



DG0637

Demo Guide

SmartFusion2 SoC FPGA CoreTSE_AHB 1000 Base-T

Loopback – Libero SoC v11.8

Contents [[hide](#)]

[1 DG0637 SmartFusion2 SoC FPGA CoreTSE](#)

[2 Revision History](#)

[3 SmartFusion2 SoC FPGA CoreTSE_AHB 1000 Base-T Loopback Demo](#)

[4 Appendix: Running the Demo Design Using Spirent Test Center](#)

[5 Documents / Resources](#)

[5.1 References](#)

DG0637 SmartFusion2 SoC FPGA CoreTSE

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all

performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Since this IP has not yet been upgraded to accommodate simulation, the information on Simulating the Design has been removed.

1.2 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Libero SoC version was updated in the software requirements and in the demo design details. For more information, see Design Requirements, page 3, and Demo Design, page 3, respectively.

1.3 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Libero SoC, FlashPro, and SoftConsole design requirements were updated. For more information, see Design Requirements, page 3.
- Throughout the document, the names of SoftConsole projects used in the demo design and all the associated figures were updated.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

SmartFusion2 SoC FPGA CoreTSE_AHB 1000 Base-T Loopback Demo

Microsemi Triple-Speed Ethernet MAC, CoreTSE_AHB is a configurable soft intellectual property (IP) core that complies with the IEEE 802.3 standard.

This demo design provides an Ethernet solution for the SmartFusion®2 SoC FPGA and implements a CoreTSE_AHB-based 1000 Base-T loopback design on the SmartFusion2 Security Evaluation Kit.

CoreTSE_AHB enables system designers to implement a broad range of Ethernet designs, from lowcost 10/100 Ethernet to higher-performance 1 gigabit ports. CoreTSE_AHB suits networking equipments such as switches, routers, and data acquisition systems.

CoreTSE is also available in a version that works with IGLOO® 2 FPGA family.

CoreTSE_AHB has the following interfaces:

- 10/100/1000 Mbps Ethernet MAC with a gigabit media independent interface (GMII) and ten bit interface (TBI) to support serial gigabit media independent interface (SGMII), 1000BASE-T, and 1000BASE-X
- GMII or TBI physical layer interface connects to Ethernet PHY

- MAC data path interface
- Advanced peripheral bus (APB) slave interface for MAC configuration registers and status counter access

CoreTSE_AHB can be configured as GMII or TBI for Ethernet network at 10/100/1000 Mbps data transfer rates (line speeds).

The CoreTSE IP is available in two different versions:

- CoreTSE_AHB: Uses AHB interface for both the transmit and receive paths. This IP works for SmartFusion2 SoC FPGA.
- CoreTSE (Non-AMBA): Uses direct access to the MAC with a streaming packet interface. This IP works for IGLOO2 FPGA and SmartFusion2 SoC FPGA.

CoreTSE and CoreTSE_AHB are identical to MSS hard Ethernet MAC in SmartFusion2 with respect to the supported features, register configuration, and register addresses. Multiple instances of the CoreTSE IP can be used to achieve Ethernet solutions in SmartFusion2 devices. The CoreTSE_AHB IP, along with MSS Ethernet MAC, can be used to support multiple Ethernet interfaces for SmartFusion2 devices. For more information about CoreTSE_AHB, see to the CoreTSE_AHB Handbook.

For more information about Ethernet applications, see the AC423: SmartFusion2/IGLOO2 Ethernet Application Note.

Note: CoreTSE_AHB requires a license for use in the Libero® SoC design suite. For license request, contact Technical Support Center through the website at www.microchip.com/support.

2.1 Design Requirements

The following table lists the design requirements for running the demo.

Table 1 • Design Requirements

Hardware Requirements	Description
-----------------------	-------------

SmartFusion2 Security Evaluation Kit: • 12 V adapter • FlashPro4 programmer	Rev D or later
Host PC or Laptop (12 GB RAM)	Windows 64-bit Operating System
Spirent Test Center (Optional)	
Software Requirements	
Libero SoC	11.8
FlashPro Programming Software	11.8
SoftConsole	v4.0
Cat Karat Packet Generator Software	Provided with design files
Wireshark Software	Provided with design files
IP Requirements	
CoreTSE_AHB	License provided on request. Contact Technical Support Center through the website at www.microchip.com/support .

2.2 Demo Design

The demo design files are available for download at: <https://www.microchip.com/en-us/application-notes/dg0637>

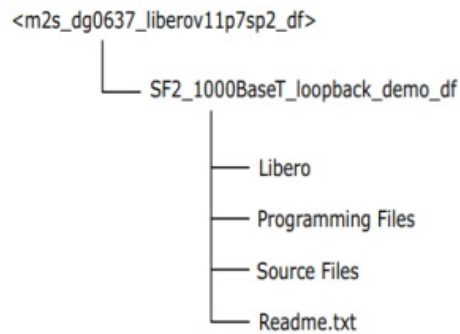
The demo design files include:

- Libero project
- Programming files
- Source files
- Readme.txt file

See the Readme.txt file for the complete directory structure.

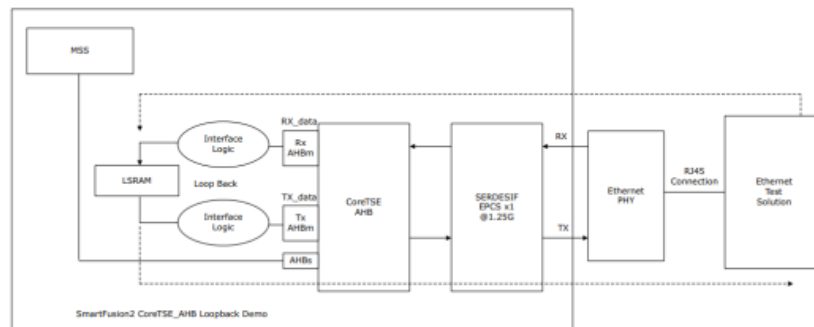
The following figure shows the top-level structure of the design files.

Figure 1 • Demo Design Files Top-Level Structure



The following figure shows the demo design block diagram.

Figure 2 • SmartFusion2 CoreTSE_AHB 1000 Base-T Loop back Demo Block Diagram



In this demo design, CoreTSE_AHB is instantiated in the FPGA fabric and connected to the on-board Ethernet PHY using high-speed serial interface (SERDES_IF).

In the previous figure, the dotted arrow in red shows the transfer of Ethernet packet from the host PC to the internal LSRAM and the dotted arrow in blue shows the retransmission of packet from LSRAM to the host.

2.2.1 Design Features

The demo design performs Ethernet loopback using CoreTSE_AHB in TBI 1000 Base-T on hardware and also in simulation.

Following are the demo design features:

- Simulation model for CoreTSE_AHB loopback design.
- CoreTSE_AHB loopback design on SmartFusion2 Security Evaluation Kit.

The following section explains the initialization and configuration of CoreTSE_AHB, SERDES_IF, and the loopback mechanism.

2.2.1.1 High-Speed Serial Interface Configuration

During the design process, CoreTSE_AHB was configured to present a Ten Bit Interface (TBI) to the SERDESIF block, which is configured for External Physical Coding SubLayer (EPCS) operation using lane 3 to create an SGMII link to the external physical-layer (PHY) device.

2.2.1.2 CoreTSE_AHB IP MAC Initialization

At power-up, firmware running on the Cortex-M3 processor will initialize control registers in CoreTSE_AHB and the external PHY device to place them in 1000 Base-T mode.

2.2.1.3 Ethernet Packet Loopback Mechanism

The following Ethernet loopback mechanism is used in this demo:

2.2.1.3.1 Ethernet Packet Reception

CoreTSE_AHB receives the Ethernet packet from the on-board Ethernet PHY through high-speed SERDES_IF.

CoreTSE_AHB receive (RX) path is connected to LSRAM through the AHB interface. The Cortex-M3 processor moves the Ethernet packet data to the LSRAM memory using DMA.

2.2.1.3.2 Ethernet Packet Transmission

To loop back the Ethernet packet, the Cortex-M3 processor reads the Ethernet packet data from LSRAM memory through AHB interface and forwards it to it on the CoreTSE_AHB transmit (TX) path. CoreTSE_AHB transmits the Ethernet packet to the on-board Ethernet PHY through high-speed SERDES.

2.2.1.4 Ethernet Test Solution

There are many ways to evaluate the CoreTSE_AHB 1000 Base-T loopback demo on the SmartFusion2 Security Evaluation board.

2.2.1.4.1 Solution 1

- The Cat Karat packet generator software installed on the host PC is used to transmit the Ethernet packet through RJ45 Ethernet copper cable.
- The Wireshark packet receiver software installed on the host PC captures the Ethernet packet (loopback) through RJ45 Ethernet copper cable.

2.2.1.4.2 Solution 2

Jumper	Pin (from)	Pin (to)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

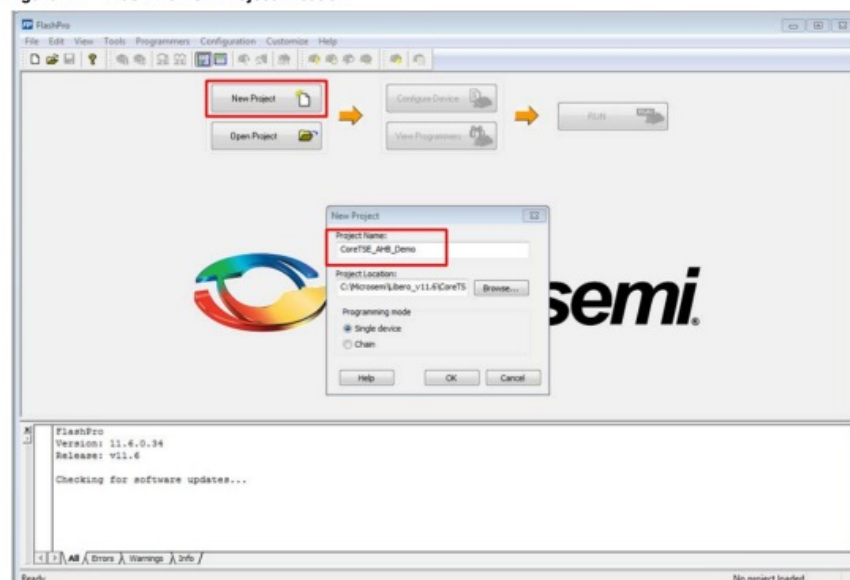
3. Connect the power supply to the J6 connector.

2.3.1 Programming the Design

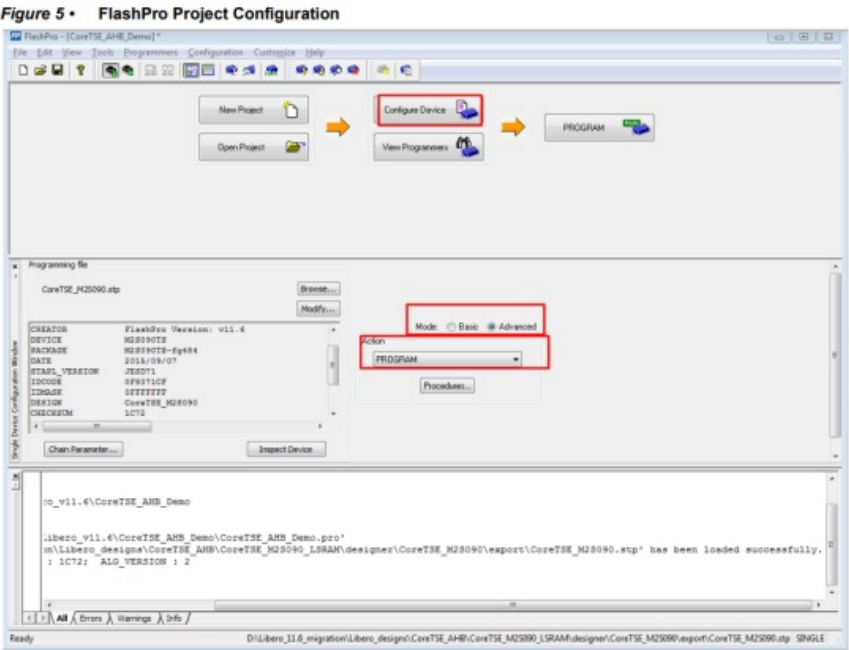
The following steps describe how to program the demo design.

1. Download the demo design from the following path: <https://www.microchip.com/en-us/application-notes/dg0637>
2. Switch ON the power supply switch, SW7.
3. Launch the FlashPro software.
4. Click New Project.
5. In the New Project window, enter the project name as CoreTSE_AHB_Demo.
6. Click Browse, and navigate to the location to save the project.
7. Select Single Device as the programming mode.
8. Click OK to save the project.

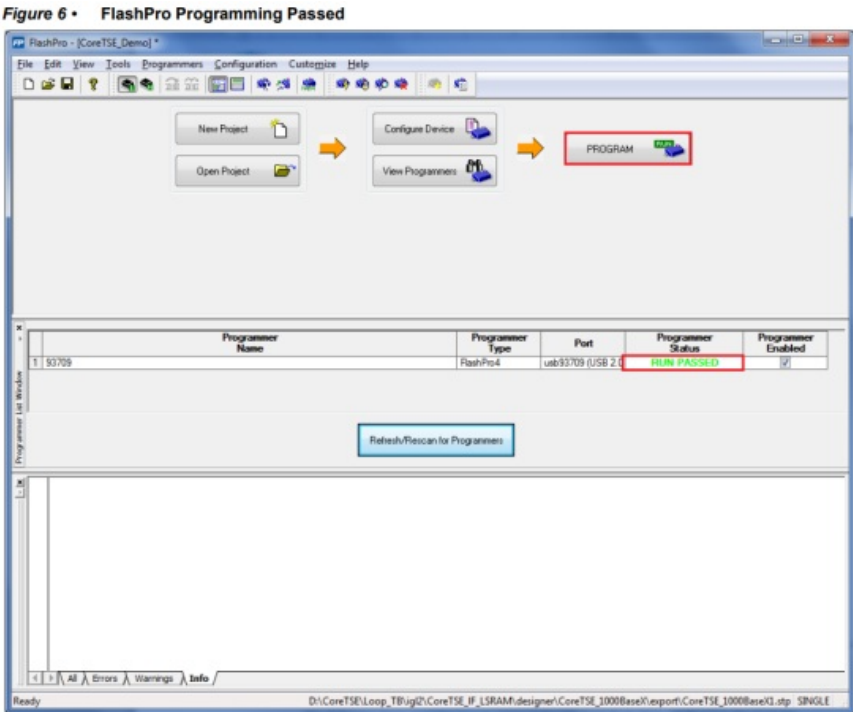
Figure 4 • FlashPro New Project Creation



9. Click Configure Device.



10. Click Browse, navigate to the location where the SF2_1000BaseT_Demo.stp file is located, and select the file. The default location is:
- <download_folder>\SF2_1000BaseT_loopback_demo_df\ProgrammingFile\
11. Select Advanced as the Mode, and select PROGRAM under Action.
12. Click PROGRAM to start programming the device. Wait until the programmer status is changed to RUN PASSED.



2.3.2 Connecting SmartFusion2 Security Evaluation Board to Host PC

The following steps describe how to connect the SmartFusion2 Security Evaluation Board to the host PC:

1. After successful programming, switch OFF the SmartFusion2 Security Evaluation Board.
2. Connect the host PC to the J13 connector on the SmartFusion2 Security Evaluation Kit using the RJ45 cable.

The following figure shows the SmartFusion2 Security Evaluation Kit board setup.

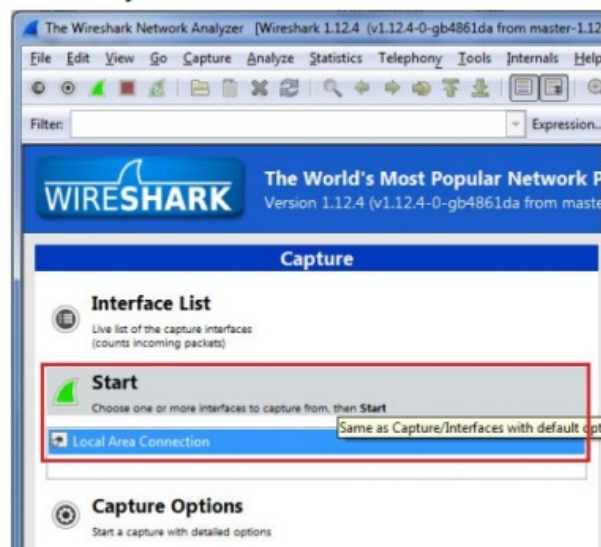
Figure 7 • SmartFusion2 Security Evaluation Kit Setup



2.3.3 Running the Demo Design with Cat Karat and Wireshark on the Hardware

1. Switch ON the power supply switch, SW7.
2. Install the Cat Karat packet software and Wireshark software on the host PC from the source files.
(<download folder>\ SF2_1000BaseT_loopback_demo_df \Source Files\)
3. On the host PC, open the Wireshark network analyzer. Select Start as shown in Figure 8, page 11.

Figure 8 • Wireshark Network Analyzer

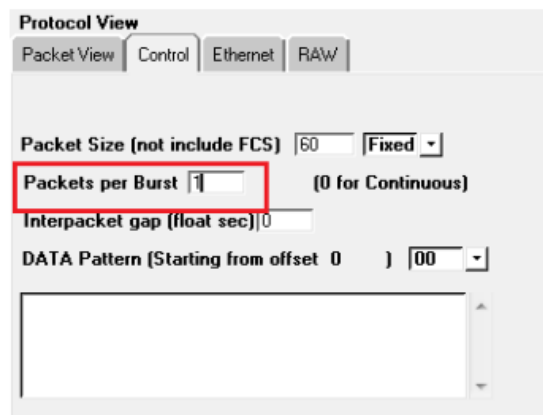


- On the host PC, open the Cat Karat software, as shown in the following figure.



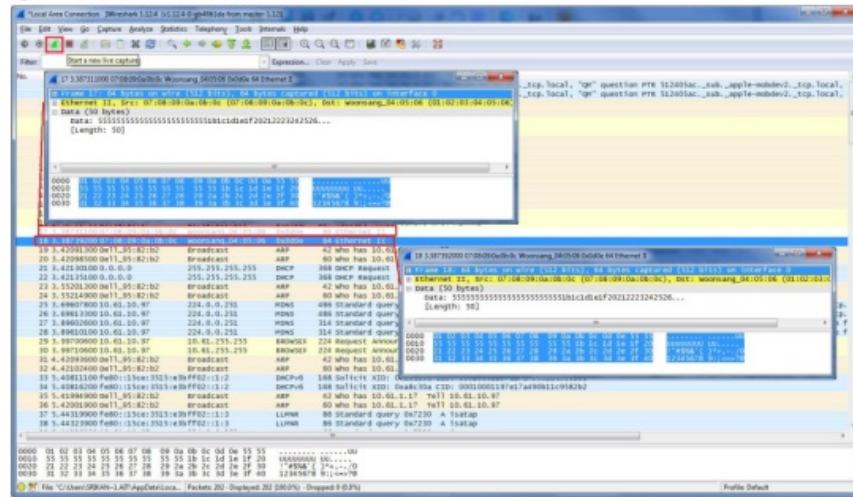
- Under Protocol View, select the Control tab and enter the value 1 for Packets per Burst, as shown in the following figure.

Figure 10 • Packet Flow Control



- Under Packet Flow, select use RAW, as shown in Figure 9, page 11.
- Under Protocol View, select the RAW tab and copy the Ethernet net packet from the source files (<download folder>\SF2_1000BaseT_loopback_demo_df\Source Files\Raw_packet.txt), as shown in Figure 9, page 11.
- Under Interfaces, select the Ethernet connection to the SmartFusion2 Evaluation board.
- Select Start Transmit from the menu, as shown in Figure 9, page 11, to transmit the packet.
- In the Wireshark software window, double-click Ethernet-II, as shown in the following figure. The transmitted and received Ethernet packets are displayed.

Figure 11 • Wireshark Software Window

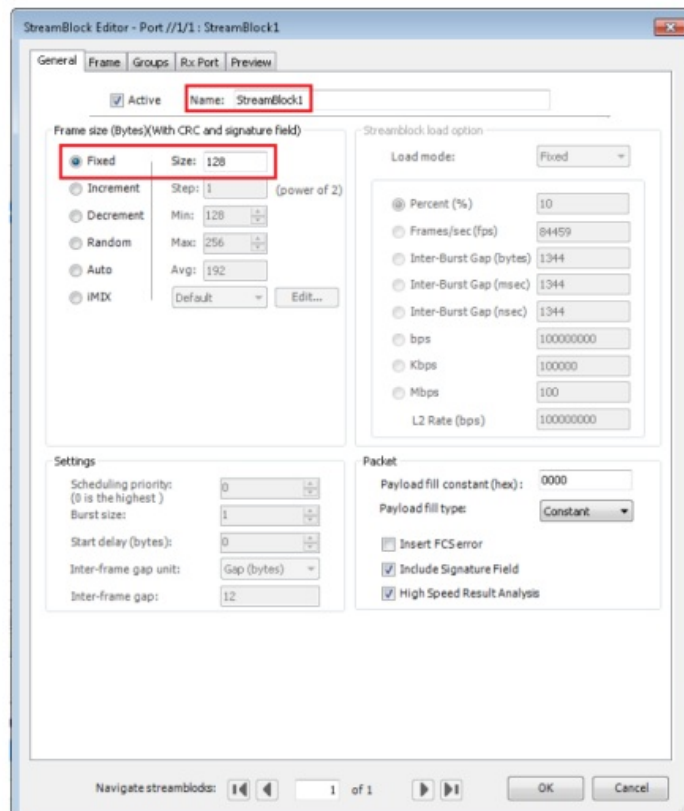


Appendix: Running the Demo Design Using Spirent Test Center

The following steps describe how to run the CoreTSE_AHB loopback demo using Spirent test center:

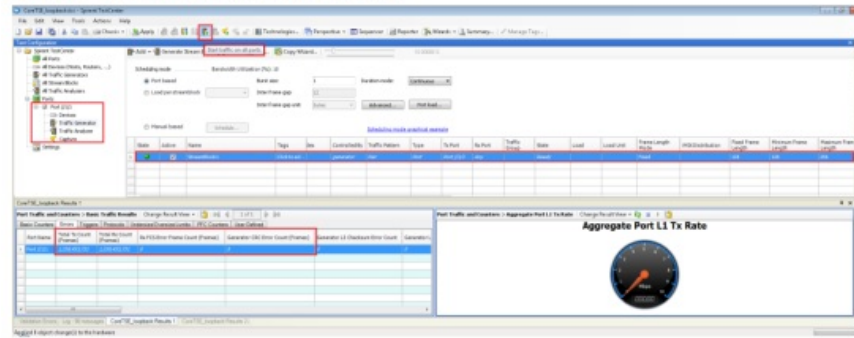
1. Connect the SmartFusion2 Security Evaluation Kit to the slot 1 Ethernet port on the Spirent test equipment using the RJ45 cable.
2. On the host PC, open the Spirent test center configurator.
3. Add port (Ethernet) in Spirent test center, as shown in the following figure.

Figure 12 • Spirent Test Center Stream Block – General Tab



4. Select Traffic Generator under Ports, add packet information in stream block editor, and click Start Traffic on all ports, as shown in the following figure.

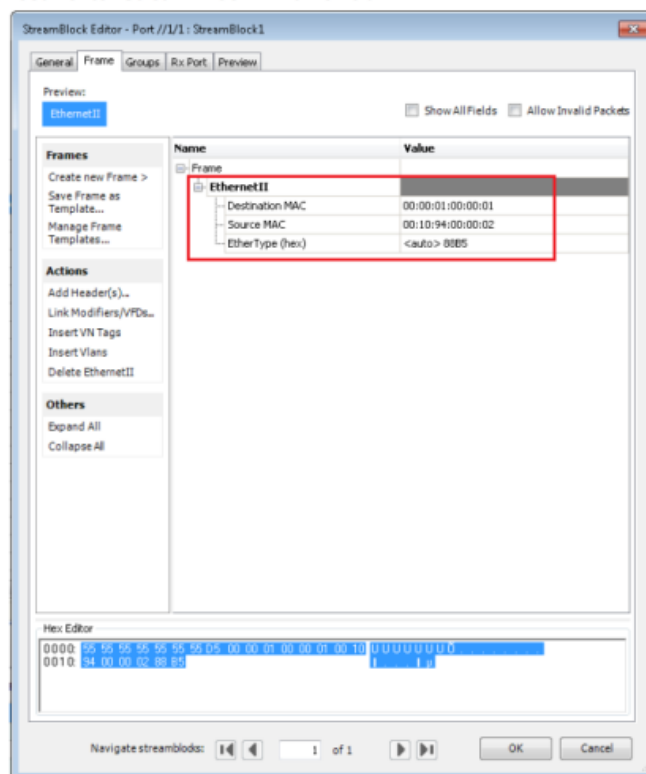
Figure 13 • Spirent Test Center –Traffic Generator



Ethernet packets are transmitted and received on port 1 through the RJ45 cable.

5. Observe the total TX, RX, RX FCS, and CRC error counts. The following figure shows the total TX, RX, RX FCS, and CRC error count information in Spirent test center. 0 indicates no loss in the packet transmission and reception.

Figure 14 • Spirent Test Center Stream Block – Frame Tab



6. Click OK to close the StreamBlock Editor.



a MICROCHIP company

Microsemi Headquarters

One Enterprise, Aliso Viejo,

CA 92656 USA

Within the USA: +1 [800-713-4113](tel:800-713-4113)

Outside the USA: +1 [949-380-6100](tel:949-380-6100)

Sales: +1 [949-380-6136](tel:949-380-6136)



Fax: +1 [949-215-4996](tel:949-215-4996)

Email: sales.support@microsemi.com

www.microsemi.com

©2023 Microsemi, a wholly owned subsidiary of Microchip Technology Inc. All rights reserved. Microsemi and the Microsemi logo are registered trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Documents / Resources

 	Microsemi DG0637 SmartFusion2 SoC FPGA CoreTSE [pdf] User Guide DG0637, DG0637 SmartFusion2 SoC FPGA CoreTSE, DG0637, SmartFusion2 SoC FPGA CoreTSE, SoC FPGA CoreTSE, CoreTSE
--	---

References

- [User Manual](#)

Microsemi

CoreTSE, DG0637, DG0637 SmartFusion2 SoC FPGA CoreTSE, Microsemi, SmartFusion2 SoC FPGA CoreTSE, SoC FPGA CoreTSE

—Previous Post

[Microsemi DG0723 Smart Fusion2 Imaging and Video Kit User Guide](#)

Leave a comment

Your email address will not be published. Required fields are marked *

Comment *

Name

Email

Website

☐ Save my name, email, and website in this browser for the next time I comment.

Post Comment

Search:

e.g. whirlpool wrf535swhz

Search

[Manuals+](#) | [Upload](#) | [Deep Search](#) | [Privacy Policy](#) | [@manuals.plus](#) | [YouTube](#)

This website is an independent publication and is neither affiliated with nor endorsed by any of the trademark owners. The "Bluetooth®" word mark and logos are registered trademarks owned by Bluetooth SIG, Inc. The "Wi-Fi®" word mark and logos are registered trademarks owned by the Wi-Fi Alliance. Any use of these marks on this website does not imply any affiliation with or endorsement.