Microsemi DG0633 IGLOO2 FPGA CoreTSE MAC 1000 Base-T Loopback Demo User Guide

Contents

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1. Revision 4.0

   The following is a summary of the changes made in this revision.

   • Updated the document for Libero SoC v2021.1.

   • Removed the references to Libero version numbers.
2. Revision 3.0

   The following is a summary of the changes in revision 3.0 of this document.

   • Libero SoC and FlashPro design requirements were updated. For more information, refer to the Design Requirements, page 3.

   • Throughout the document, all the associated figures were updated.
3. Revision 2.0

   In revision 2.0 of this document, updated the document for Libero SoC v11.7 software release.

4. Revision 1.0

   Revision 1.0 was the first publication of this document.

IGLOO2 FPGA CoreTSE MAC 1000 Base-T Loopback Demo

Microsemi Core Triple-Speed Ethernet (CoreTSE) Media Access Controller (MAC) IP is a configurable soft Intellectual Property (IP) core that complies with the IEEE 802.3 standard. This demo design provides an Ethernet solution for the IGLOO2 FPGA and implements a CoreTSE MAC -based 1000 Base-T loopback design on the IGLOO2 Evaluation Kit.

CoreTSE MAC enables system designers to implement a broad range of Ethernet designs, from low-cost 10/100 Ethernet to higher-performance 1 gigabit ports. CoreTSE MAC suits networking equipment such as switches, routers, and data acquisition systems. CoreTSE MAC is also available in a version that works with SmartFusion®2 System-on-Chip (SoC) FPGA family.

The CoreTSE MAC has the following interfaces:

- 10/100/1000 Mbps Ethernet MAC with a Gigabit Media Independent Interface (GMII) and Ten Bit Interface (TBI) to support Serial Gigabit Media Independent Interface (SGMII), 1000BASE-T, and 1000BASE-X
- GMII or TBI physical layer interface connects to Ethernet PHY
- MAC data path interface
- Advanced Peripheral Bus (APB) slave interface for MAC configuration registers and status counter access

The CoreTSE MAC can be configured as GMII or TBI for an Ethernet network at 10/100/1000 Mbps data transfer rates (line speeds).

The CoreTSE MAC is available in two different versions:

- CoreTSE_AHB: Uses the AHB interface for both the transmit and receive paths. This IP works for SmartFusion2 SoC FPGA.
- CoreTSE (Non-AMBA): Uses direct access to the MAC with a streaming packet interface. This IP works for IGLOO2 FPGA and SmartFusion2 SoC FPGA.

CoreTSE and CoreTSE_AHB are identical to MSS hard Ethernet MAC in SmartFusion2 for the supported features, register configuration, and register addresses. Multiple CoreTSE MAC IPs can be used in IGLOO2 to achieve Ethernet solutions. CoreTSE MAC can be used in SmartFusion2 devices along with MSS Ethernet MAC to support multiple Ethernet interfaces. For more information about CoreTSE MAC, refer to the CoreTSE Handbook.
For more information about Ethernet applications, refer to the AC423: SmartFusion2/IGLOO2 Ethernet Application Note.

Note: CoreTSE MAC requires license for using in Libero® System-on-Chip (SoC) design. For license request, send an email to **soc_marketing@microsemi.com**

Design Requirements

The following table lists the design requirements for running the demo.
Table 1 • Design Requirements

Table 1 • **Design Requirements**

Requirement	Version
Operating System	64 bit Windows 7 and 10
Hardware	
IGLOO2 Evaluation Kit: • 12 V adapter • FlashPro4 programmer	Rev D or later
Spirent Test Center (Optional)	
Software	
Libero SoC	**Note:** Refer to the `readme.txt` file provided in the design files for the software versions used with this reference design.
FlashPro Express	
Cat Karat Packet Generator Software	Provided with design files
Wireshark Software	Provided with design files
IP	
CoreTSE MAC	License provided on request

Note: Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

Prerequisites
Before you start:

1. Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location:
   https://www.microsemi.com/product-directory/design-resources/1750-libero-soc
2. For demo design files download link: **http://soc.microsemi.com/download/rsc/?f=m2gl_dg0633_df**

Demo Design
The demo design files include:

- Libero project
- Programming files
- Source files
- Readme.txt file

Refer to the Readme.txt file for the complete directory structure.

The following figure shows the top-level structure of the design files.
Figure 1 Demo Design Files Top-Level Structure

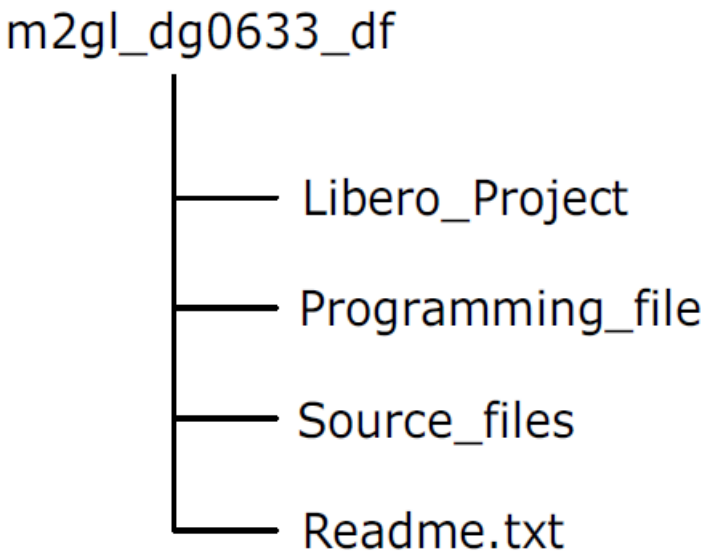
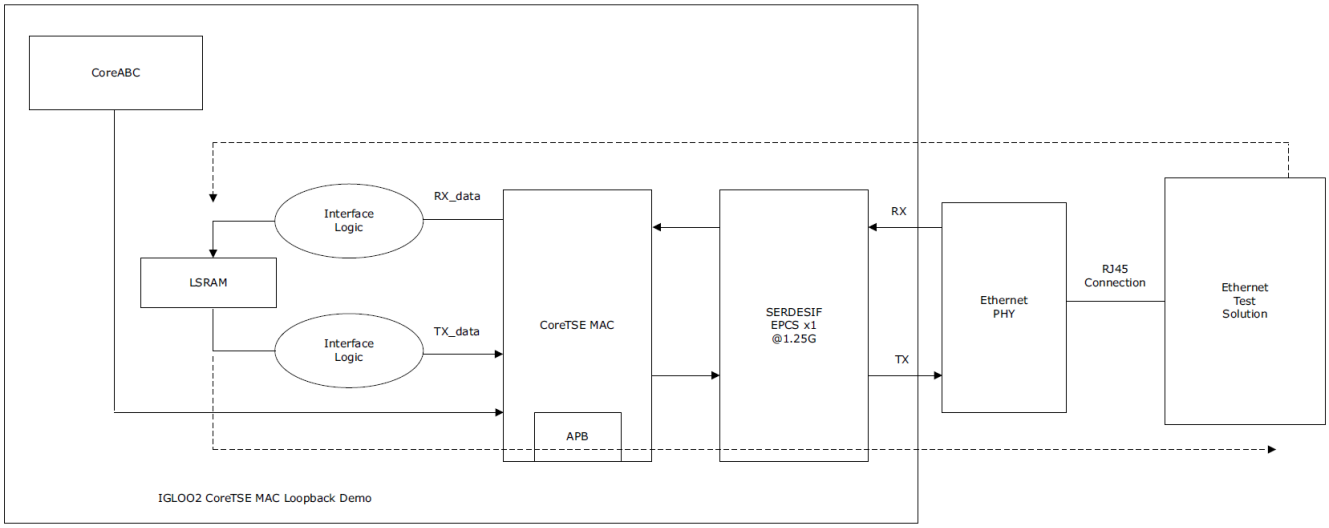


Figure 2 IGLOO2 CoreTSE MAC 1000 Base-T Loopback Demo



In this demo design, CoreTSE MAC is instantiated in the FPGA fabric and connected to the on-board Ethernet PHY using the high-speed serial interface (SERDES_IF).
In the previous figure, the dotted arrow in red shows the transfer of an Ethernet packet from the host PC to the internal LSRAM, and the dotted arrow in blue shows the retransmission of the packet from LSRAM to the host.

Demo Design Features
The demo design performs Ethernet loopback using CoreTSE MAC in TBI 1000Base-T on hardware and also in simulation.

Following are the demo design features:

- Simulation model for CoreTSE MAC loopback design.
- CoreTSE MAC loopback design on IGLOO2 Evaluation Kit.

The following section explains the initialization and configuration of CoreTSE MAC, SERDES_IF, and the loopback mechanism.

1. CoreTSE IP MAC Initialization

CoreTSE MAC is configured in TBI mode. The CoreABC soft-core is used to initialize CoreTSE MAC in 1000 Base-T and on-board Ethernet PHY.

Note: CoreABC is a Microsemi RISC processor that is implemented in logic gates. The CoreABC IP is available in the Libero SoC software IP tools catalog.

2. High-Speed Serial Interface Configuration

   The high-speed SERDES_IF is configured in the External Physical Coding Sub layer (EPCS) mode lane 3 in the Libero GUI and is connected between CoreTSE MAC and on-board Ethernet PHY.

3. Ethernet Packet Loopback

   The following Ethernet loopback mechanism is used in this demo:

   1. Ethernet Packet Reception

      The CoreTSE MAC receives the Ethernet packet from on-board Ethernet PHY through high-speed SERDES_IF.

      The CoreTSE MAC receive (RX) path is connected to LSRAM through the receive interface logic. This interface logic is implemented in Verilog RTL and is used to keep the packet on to LSRAM memory.

   2. Ethernet Packet Transmission

      To loopback, the Ethernet packet, the interface logic implemented in Verilog RTL reads the Ethernet packet data from LSRAM memory and keeps it on CoreTSE MAC transmit (TX) path. CoreTSE MAC transmits the Ethernet packet to on-board Ethernet PHY through high-speed SERDES.

4. **Ethernet Test Solution**

   There are many ways to evaluate the CoreTSE MAC 1000 Base-T loopback demo on the IGLOO2 Evaluation Board.

   1. Solution 1

      • The Cat Karat packet generator software installed on the host PC is used to transmit the Ethernet packet through RJ45 Ethernet copper cable.

      • The Wireshark packet receiver software installed on the host PC captures the Ethernet packet (loopback) through RJ45 Ethernet copper cable.

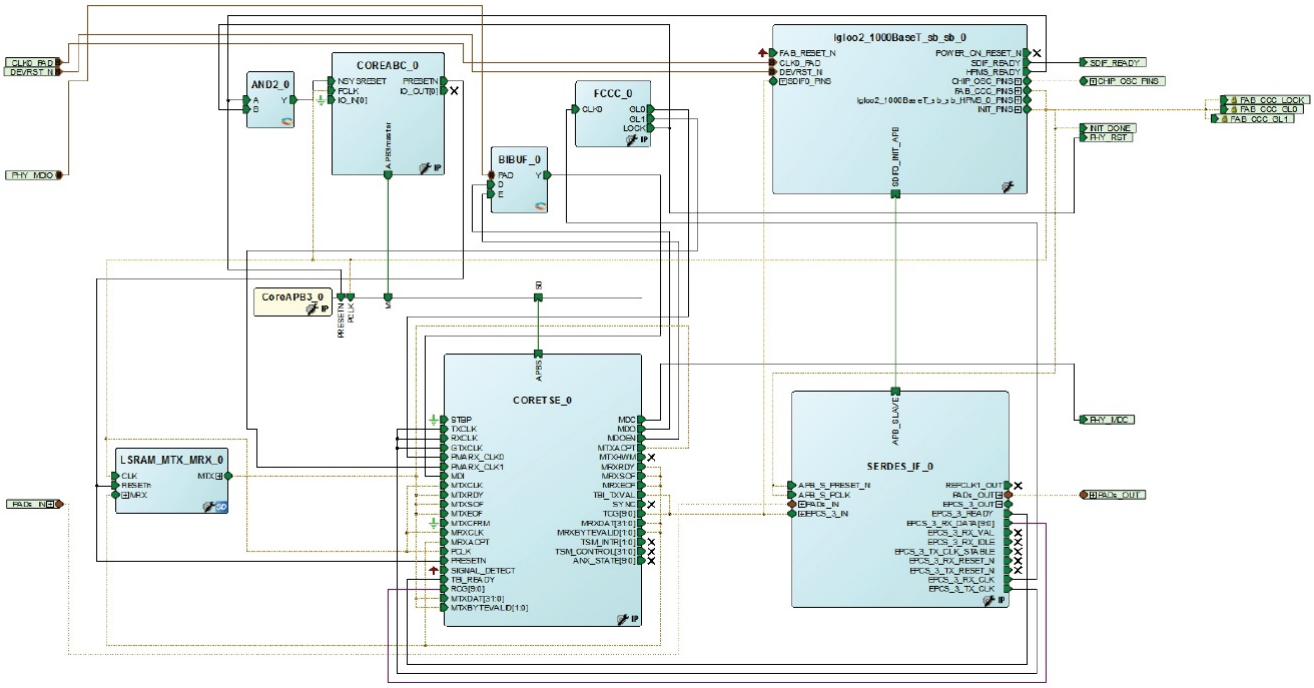
   2. Solution 2

      Spirent test center or an equivalent solution can be used to test the CoreTSE MAC loopback demo. For more information, refer to the Appendix 2: Running the Demo Design Using Spirent Test Center, page 18.

Demo Design Description

This demo design is implemented by configuring the CoreTSE MAC for the TBI mode. The following figure shows the Libero SoC hardware implementation for this demo design.

Figure 3 • **Libero SmartDesign**



Libero hardware project uses the following resources:

- CoreTSE MAC
- CoreABC to configure CoreTSE MAC and on-board Ethernet PHY
- LSRAM interface logic uses TPSRAM, receives and transmits logic implemented in Verilog RTL
- High-speed serial interface (SERDES_IF) configured for EPCS lane 3 mode
- Dedicated input pad 0 as the clock source

Simulating the Design

The testbench design is created for the CoreTSE MAC loopback demo. The testbench transmits the Ethernet packet to the CoreTSE MAC loopback demo design and receives the loopback Ethernet packet from the CoreTSE MAC loopback demo design.

Simulation

For simulation, the Ethernet packet is defined in a text file:
(m2gl_dg0633_df\Libero_Project\Simulation\CoreTSE_1000BaseT_Demo\simulation\ packetfile.txt).
The Raw Ethernet Packet frame is:
0102030405060708090a0b0c0d0e55555555555555555555555551b1c1d1e1f2021222324252627282 92
a2b2c2d2e2f303132333435363738393a3b3c3d3e3f40.
Testbench reads the Ethernet packet from the text file and puts the Ethernet packet on to the high-speed SERDES_IF of CoreTSE MAC loopback design.
The loopback packet is received by the testbench and displayed on the ModelSim transcript window.

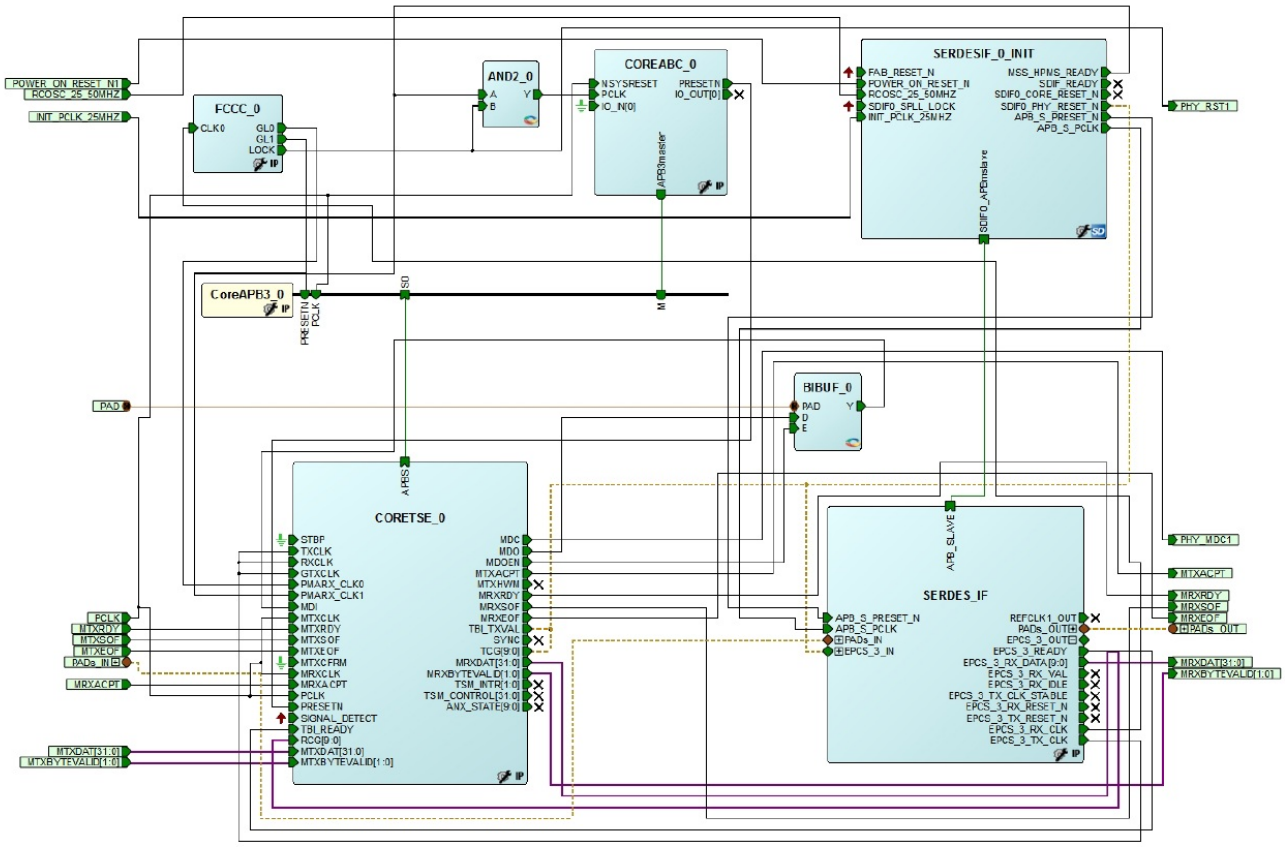
The following figure and Figure 5, page 8 show the Libero SmartDesign to simulate the CoreTSE MAC loopback demo design. The simulation testbench has the following Libero components:

- CoreTSE MAC
- High-speed SERDES_IF
- Testbench with packet transmit and packet receive logic

The testbench smart design module reads the Ethernet packet from the packetfile.txt file and sends it to the

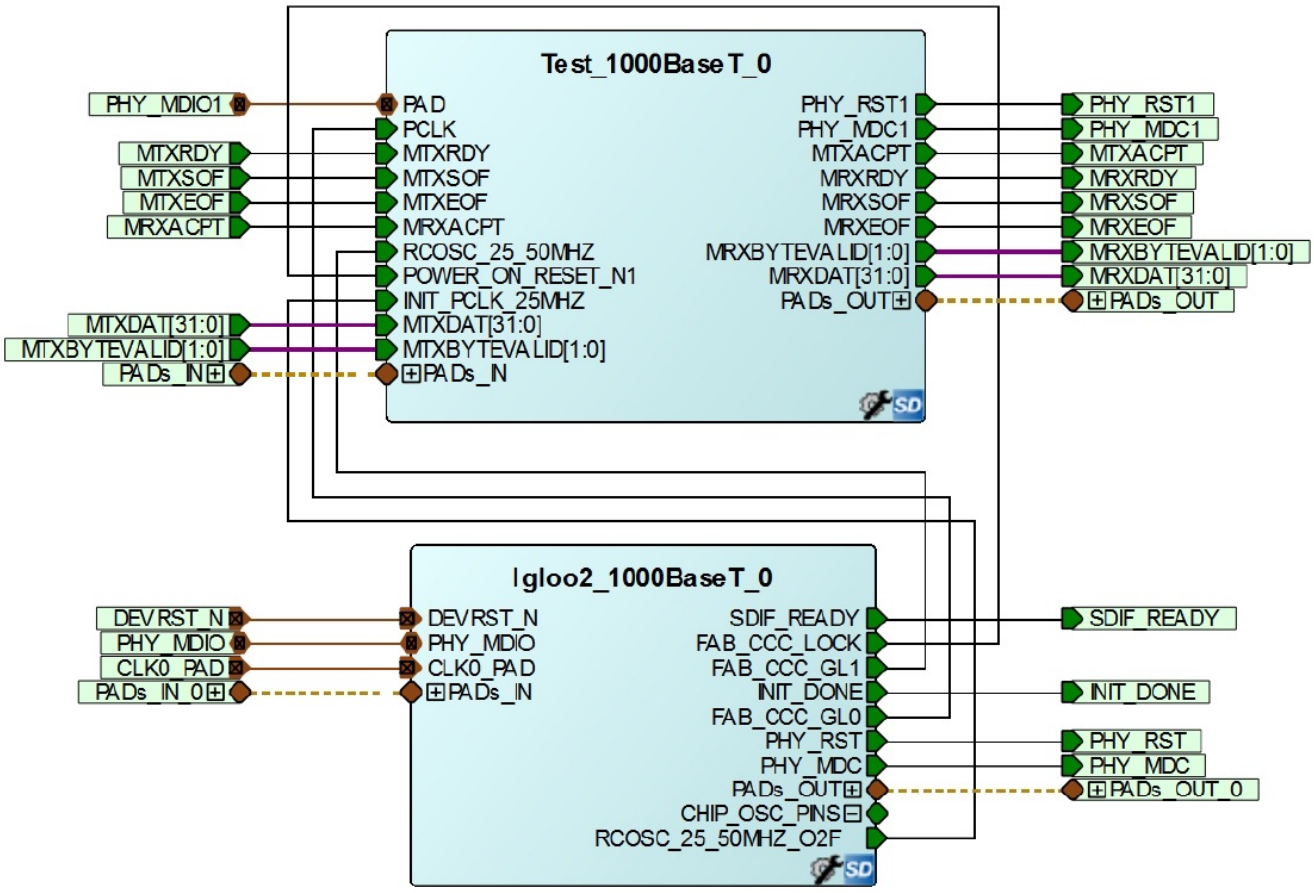
IGLOO2 CoreTSE MAC loopback design through a high-speed serial interface. The loopback Ethernet packet is received by the testbench through the high-speed serial interface. ModelSim displays the received Ethernet packet on the transcript window. This completes the Ethernet packet loopback simulation.

Figure 4 • **SmartDesign for Simulation**



The Libero SmartDesign top module contains the CoreTSE MAC loopback design and the testbench module.

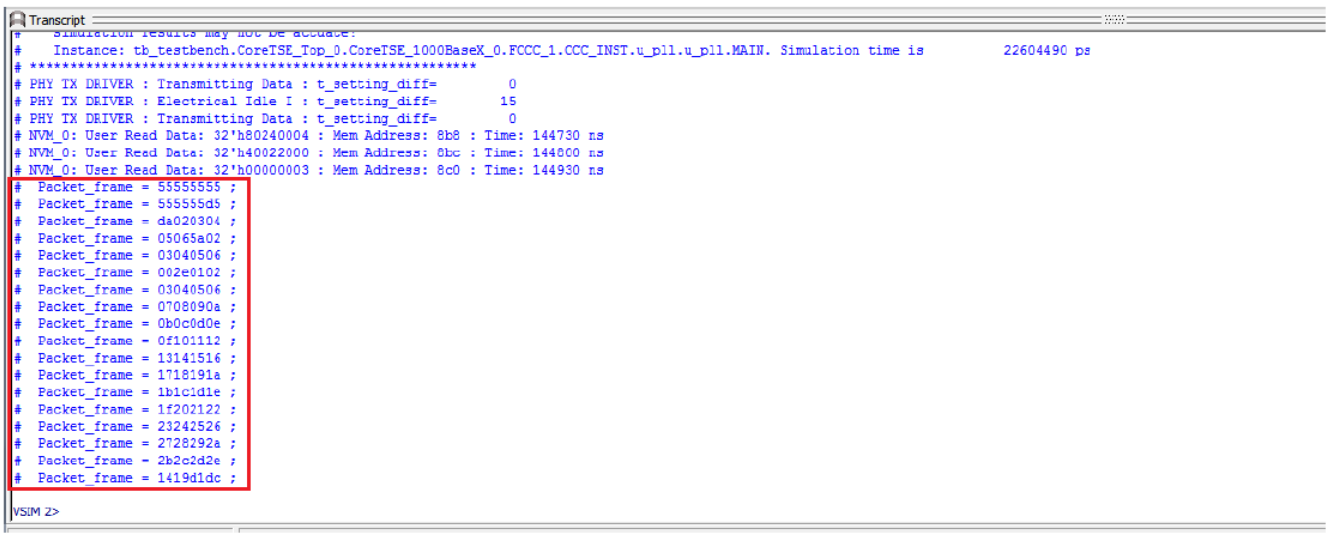
Figure 5 • **Libero SmartDesign Top Module**



The following steps describe how to simulate the demo:

1. Open the Libero project from the following design files: m2gl_dg0633_df\Libero_Project\Simulation\CoreTSE_1000BaseT_Demo\Libero_Project.prjx.
2. In the Design Flow tab, under Verify Pre-Synthesized Design, double-click Simulate. ModelSim runs the design for 180 µs. The following figure shows the received Ethernet packet information displayed on the ModelSim Transcript window.

Figure 6 • **ModelSim Transcript Messages**



The following figure and Figure 8, page 9 show the Waveform window. The highlighted portion shows the transmitted and received Ethernet packets.

Figure 7 • **Simulation Window-Transmitted Ethernet Packet**

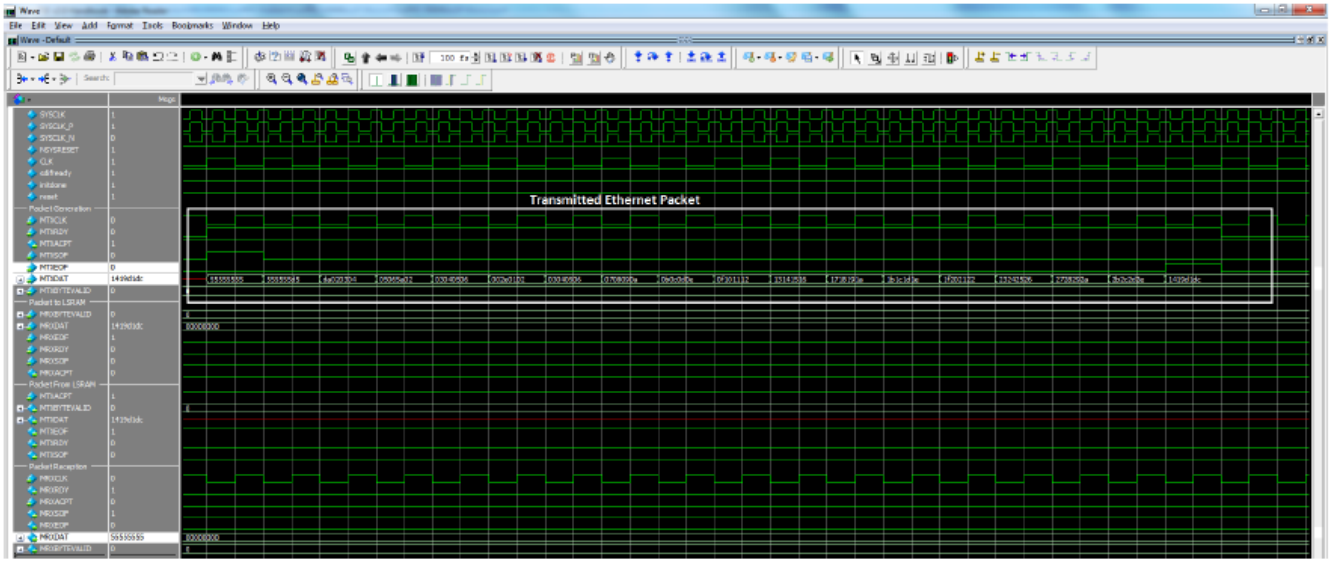
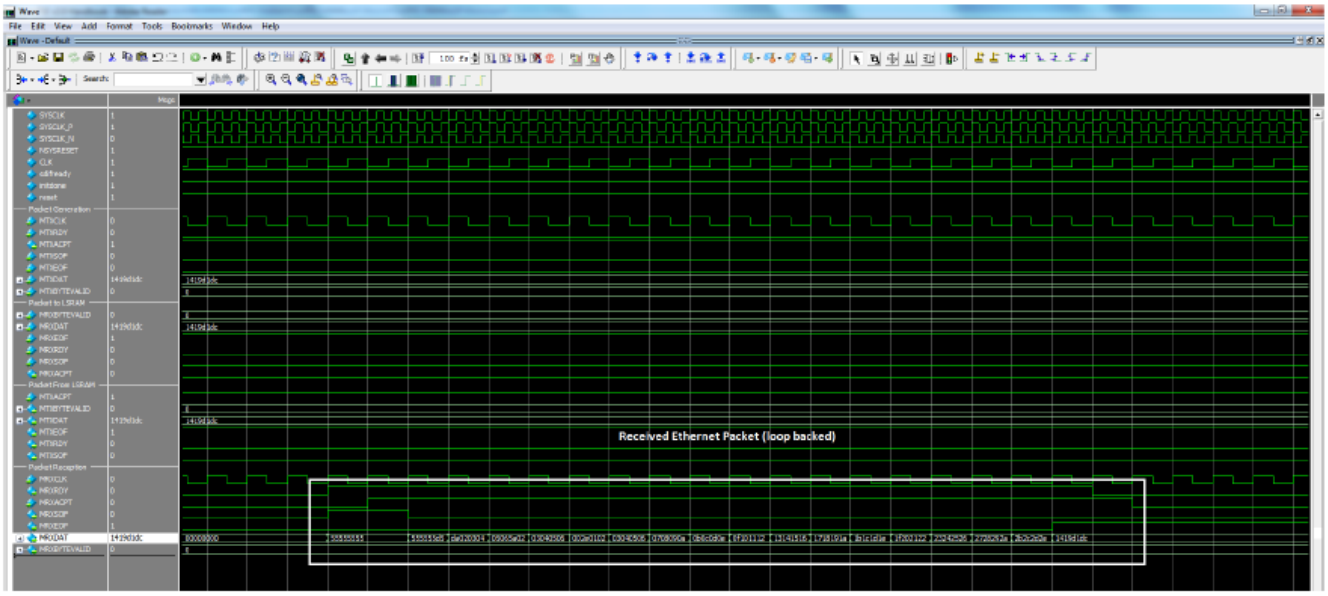


Figure 8 • **Simulation Window-Received Ethernet Packet**



Setting Up the Demo Design

The following steps describe how to setup the demo:

1. Connect the jumpers to the IGLOO2 FPGA Evaluation Kit board, as shown in the following table.
2. Connect the power supply to the J6 connector and switch ON.
3. Connect the FlashPro4 Programmer to the J5 connector on the IGLOO2 FPGA Evaluation Kit board.

Note: Ensure that the power supply switch SW7 is switched off while connecting the jumpers to the IGLOO2 FPGA Evaluation Kit.

Table 2 IGLOO2 FPGA Evaluation Kit Jumper Settings

Jumper	Pin (From)	Pin (To)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

Programming the Device

Program the IGLOO2 Evaluation Kit board with the job file provided as part of the design files using FlashPro Express software, refer to the Appendix 1: Programming the Device Using FlashPro Express, page 15.

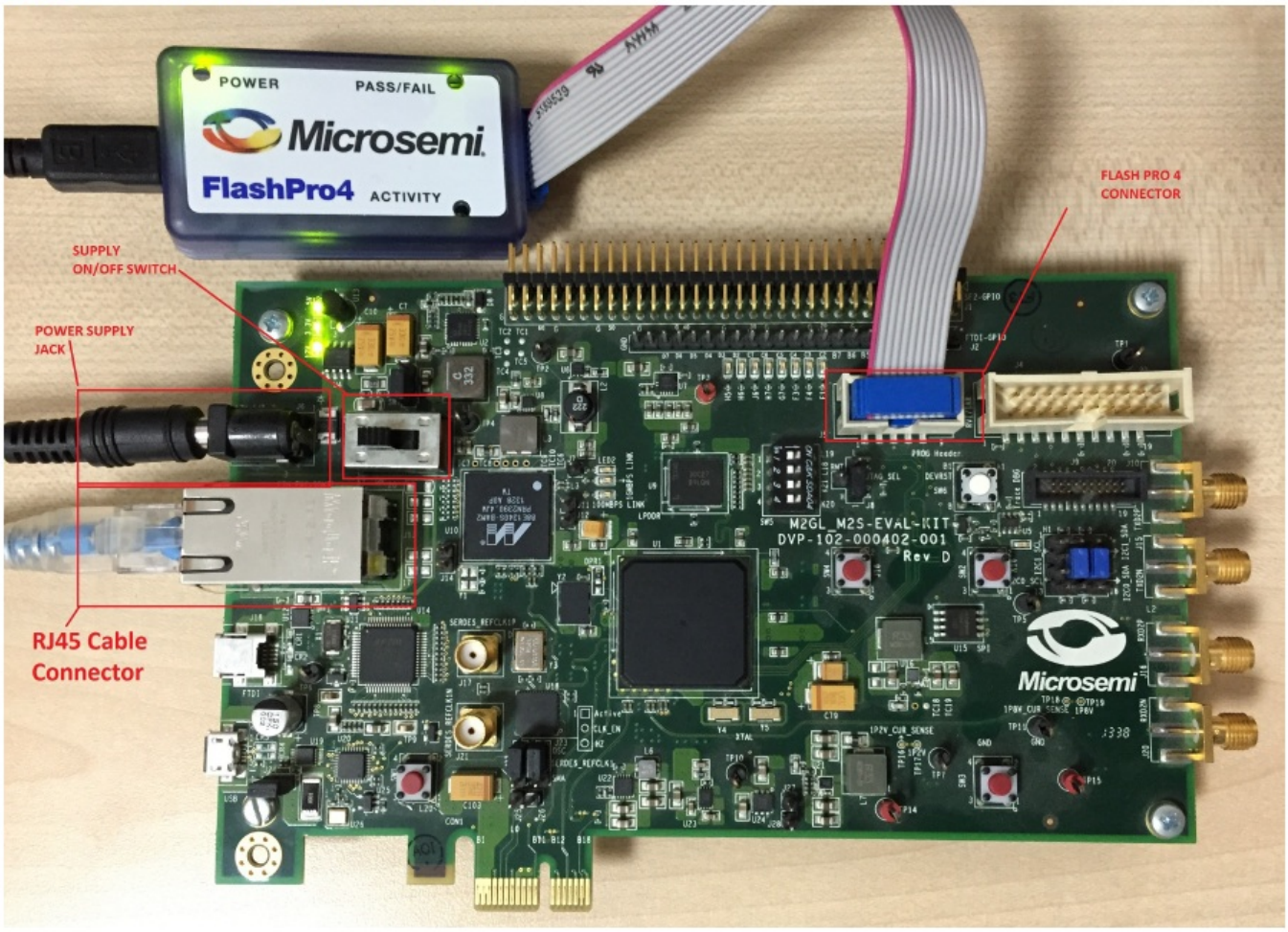
Connecting IGLOO2 Evaluation Kit Board to Host PC

The following steps describe how to connect the IGLOO2 Evaluation Kit Board to the host PC:

1. After successful programming, switch OFF the IGLOO2 Evaluation Kit Board.
2. Connect the host PC to the J13 connector on the IGLOO2 Evaluation Kit using the RJ45 cable.

The following figure shows the IGLOO2 Evaluation Kit board setup.

Figure 9 • **IGLOO2 Evaluation Kit Setup**

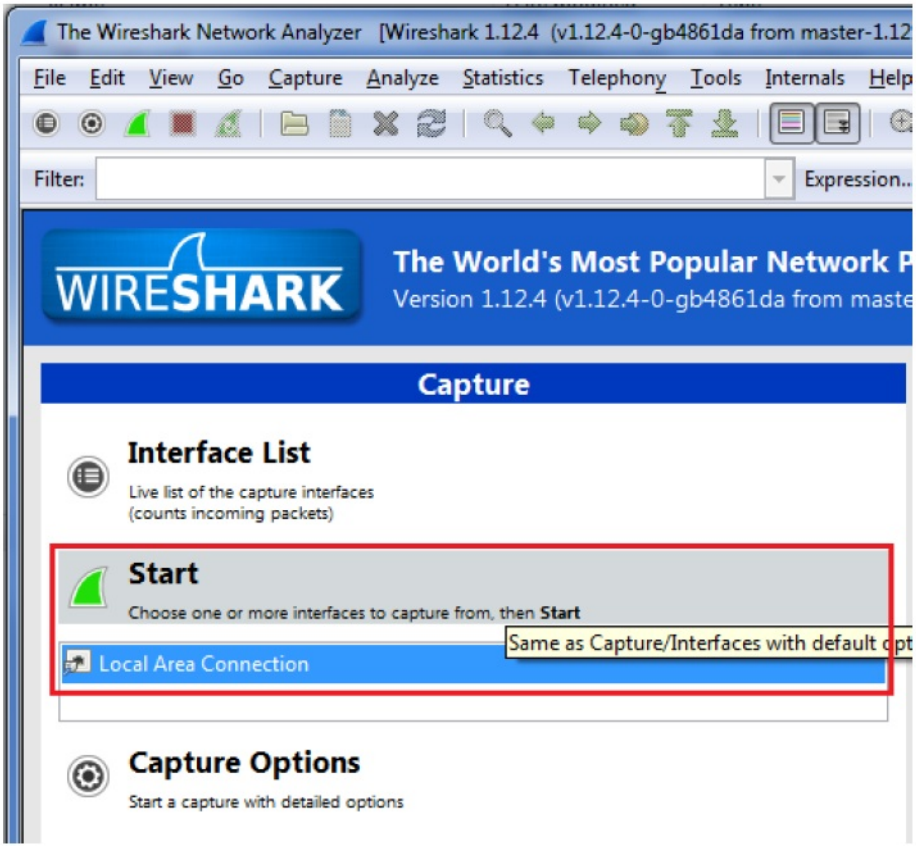


Running the Demo Design with Cat Karat and Wireshark on the Hardware

The following steps describe how to run the demo design:

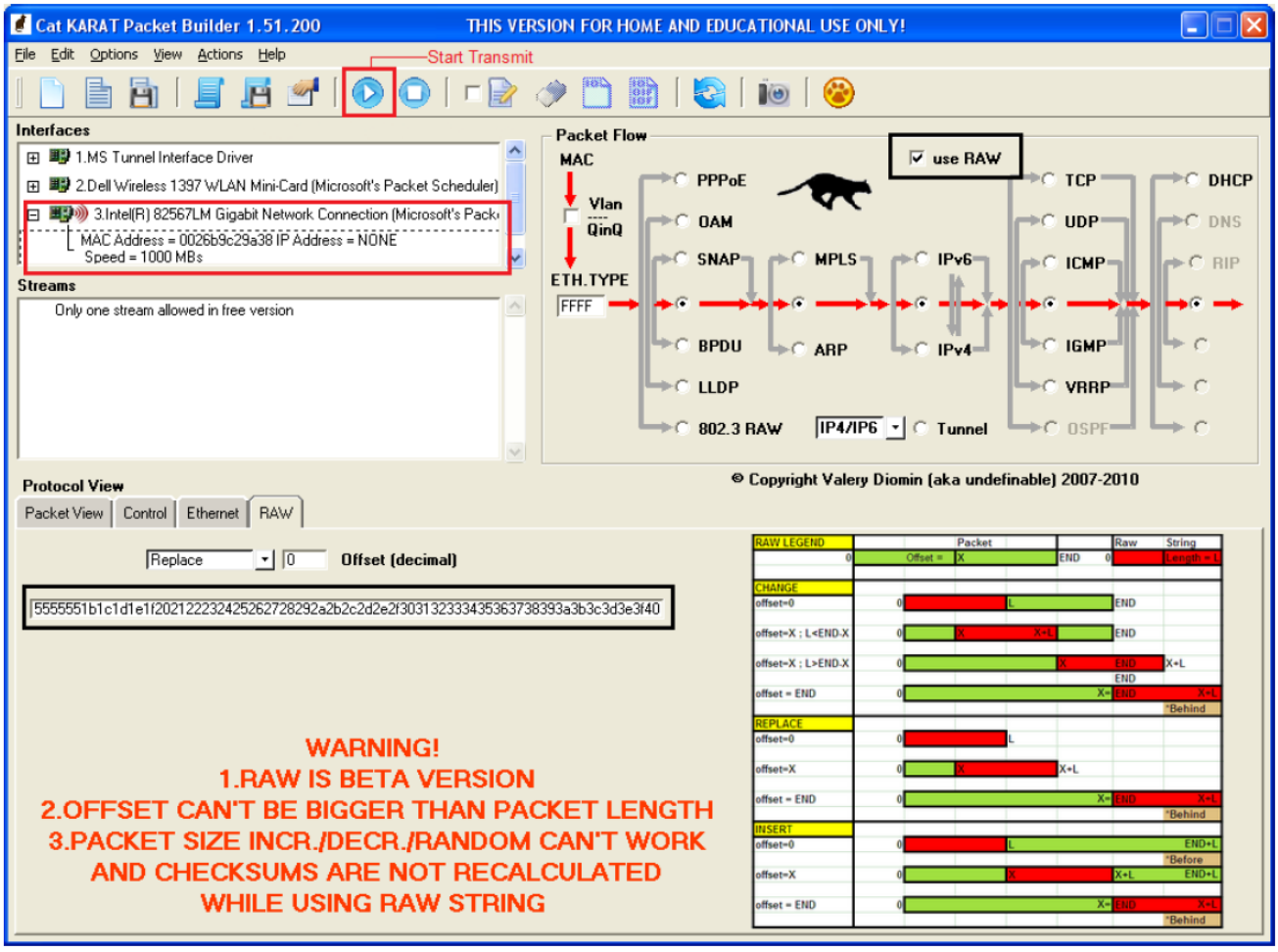
1. Switch ON the power supply switch, SW7.
2. Install the Cat Karat packet software and Wireshark software on the host PC from the source files. (m2gl_dg0633_df\Source files)
3. On the host PC, open the Wireshark network analyzer. Select Start, as shown in Figure 10, page 12.

Figure 10 • **Wireshark Network Analyzer**



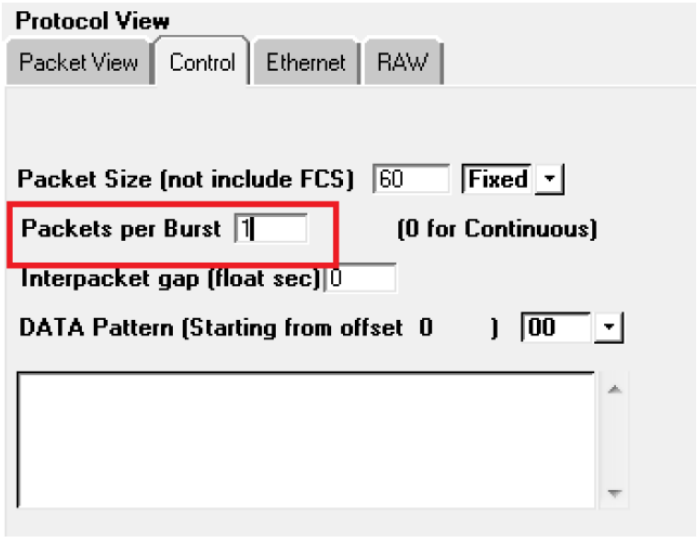
4. On the host PC, open the Cat Karat software, as shown in the following figure.

Figure 11 • **Cat Karat Packet Generate Window**



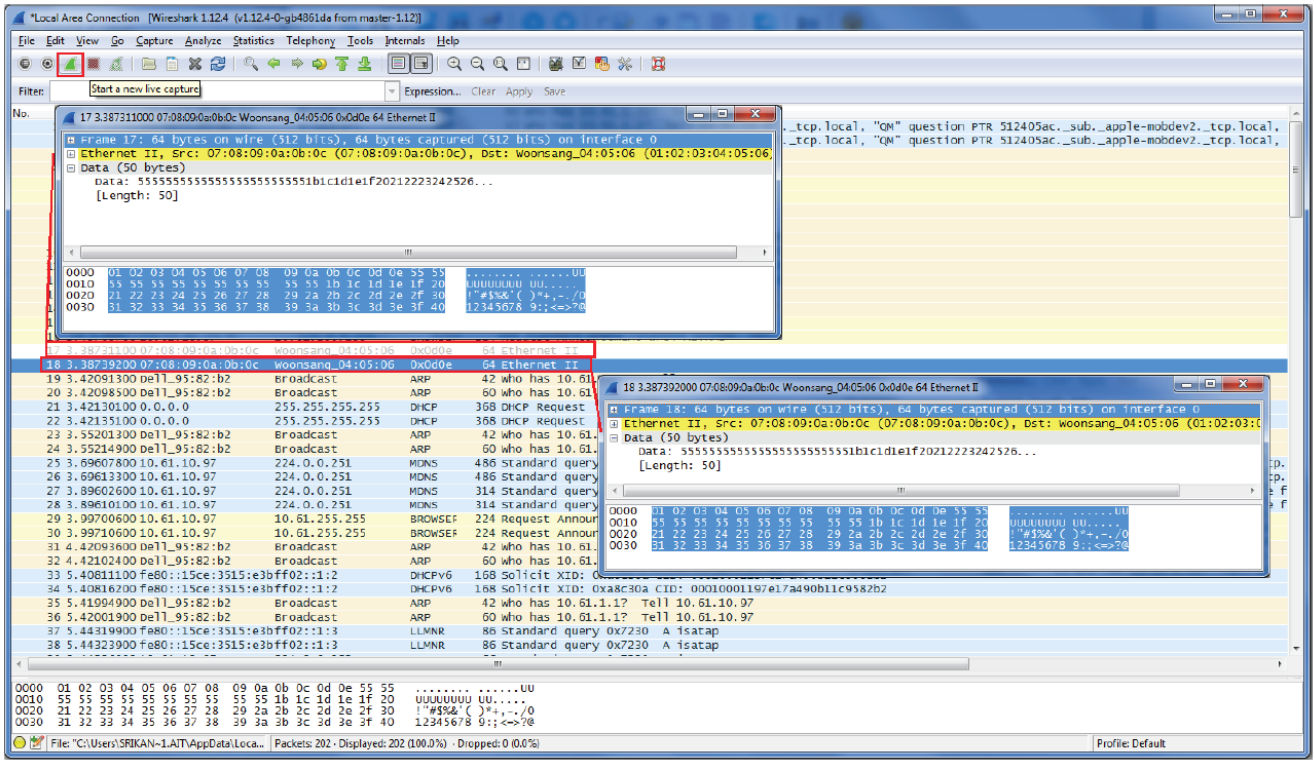
5. Under Protocol View, click Control tab and enter the value 1 for Packets per Burst, as shown in Figure 12, page 13.

Figure 12 • **Packet Flow Control**



6. Under Packet Flow, click use RAW, as shown in Figure 11, page 13.
7. Under Protocol View, select the RAW tab and copy and paste the Ethernet net packet from the source files (m2gl_dg0633_df\Source_files\Raw_frame.txt) as shown in Figure 11, page 13.
8. Under Interfaces, select the Ethernet connection to the IGLOO2 Evaluation Board.
9. Select Start Transmit from the menu, as shown in Figure 11, page 13, to transmit the packet.
10. In the Wireshark software window, double-click Ethernet-II, as shown in the following figure. The transmitted and received Ethernet packets are displayed.

Figure 13 • **Wireshark Software Window**



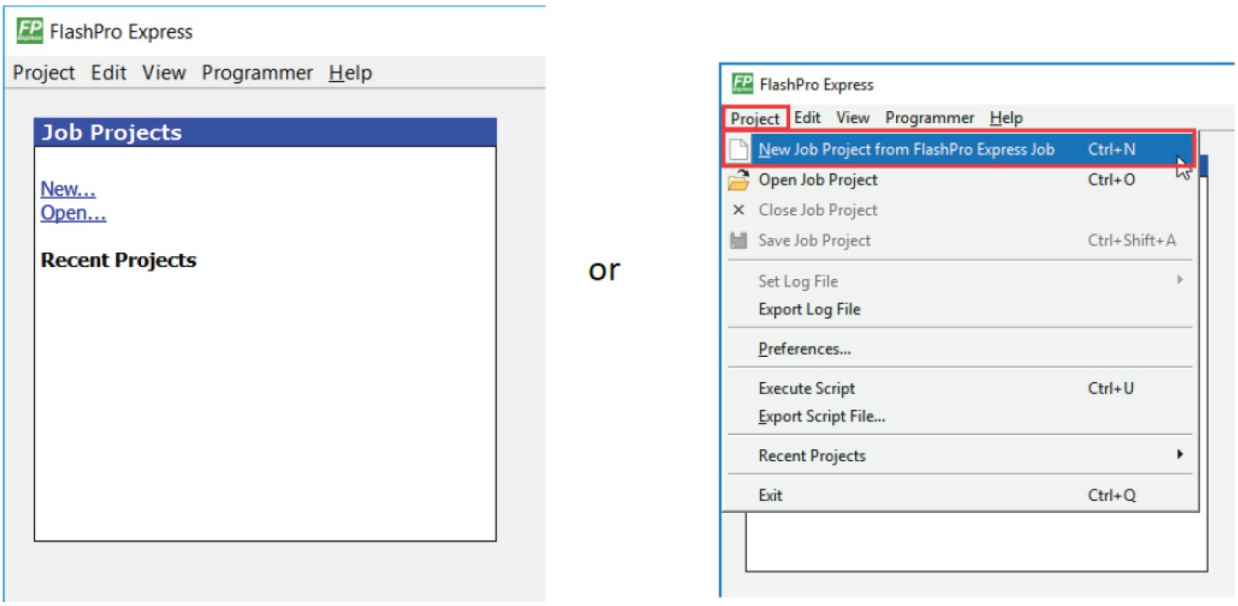
Appendix 1: Programming the Device Using FlashPro Express

This section describes how to program the IGLOO2 device with the programming job file using FlashPro Express.

To program the device, perform the following steps:

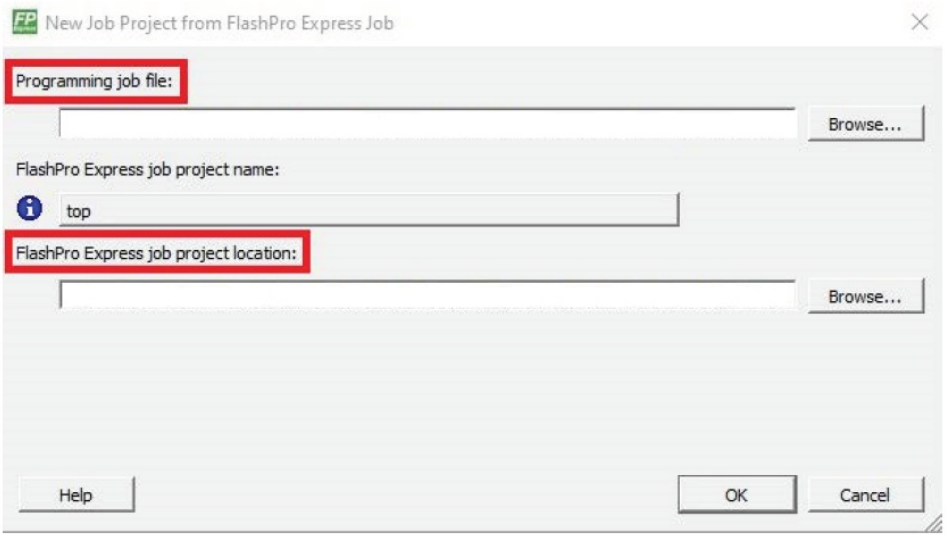
1. Ensure that the jumper settings on the board are the same as those listed in Table 2, page 10.
   Note: The power supply switch must be switched off while making the jumper connections.
2. Connect the power supply cable to the J6 connector on the board.
3. Power ON the power supply switch SW7.
4. On the host PC, launch the FlashPro Express software.
5. Click New or select New Job Project from FlashPro Express Job from Project menu to create a new job project, as shown in the following figure.

Figure 14 • **FlashPro Express Job Project**



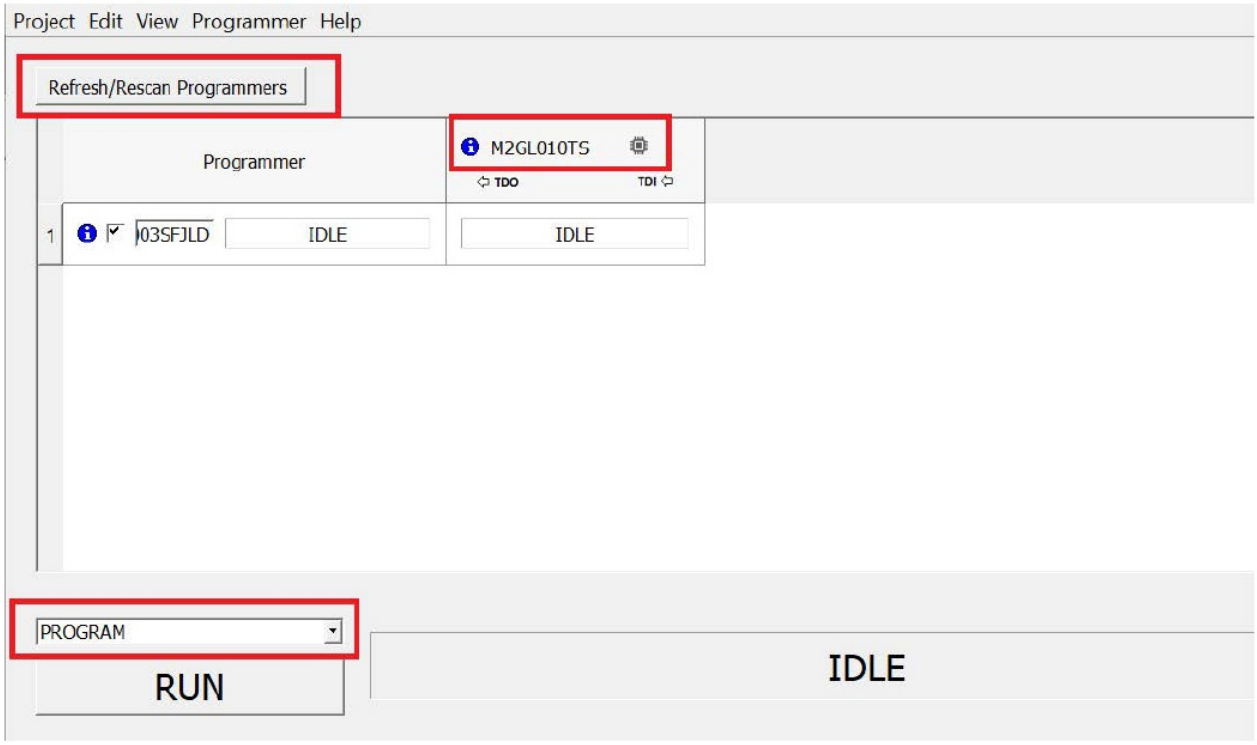
6. Enter the following in the New Job Project from FlashPro Express Job dialog box:
    - Programming job file: Click Browse, and navigate to the location where the .job file is located and select the file. The default location is:<download_folder>\m2gl_dg0633_df\Programmingfile
    - FlashPro Express job project name: Click Browse and navigate to the location where you want to save the project.

Figure 15 • **New Job Project from FlashPro Express Job**



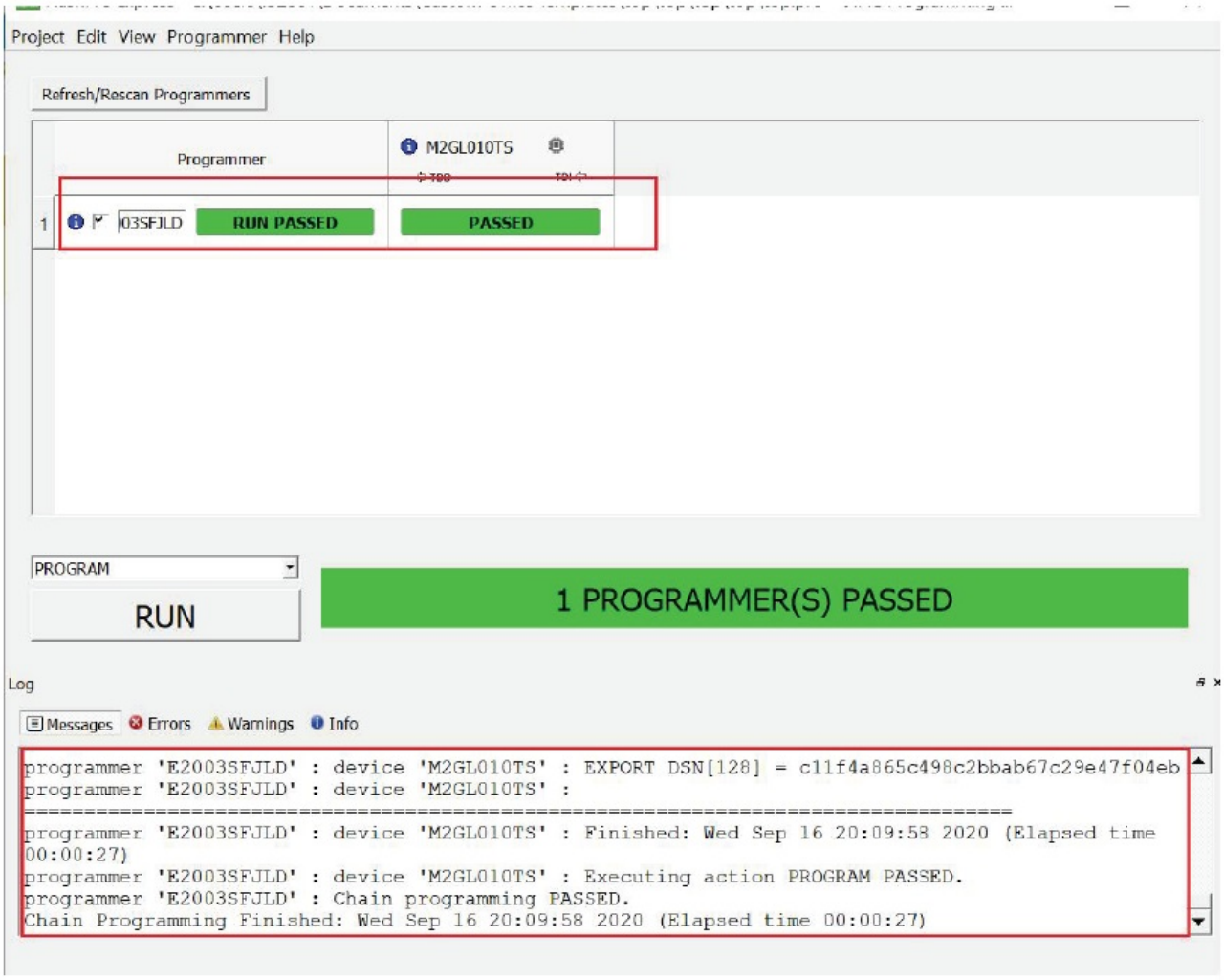
7. Click OK. The required programming file is selected and ready to be programmed in the device.
8. The FlashPro Express window appears as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click Refresh/Rescan Programmers.

Figure 16 • **Programming the Device**



9. Click RUN. When the device is programmed successfully, a RUN PASSED status is displayed as shown in the following figure.

Figure 17 • **FlashPro Express—RUN PASSED**



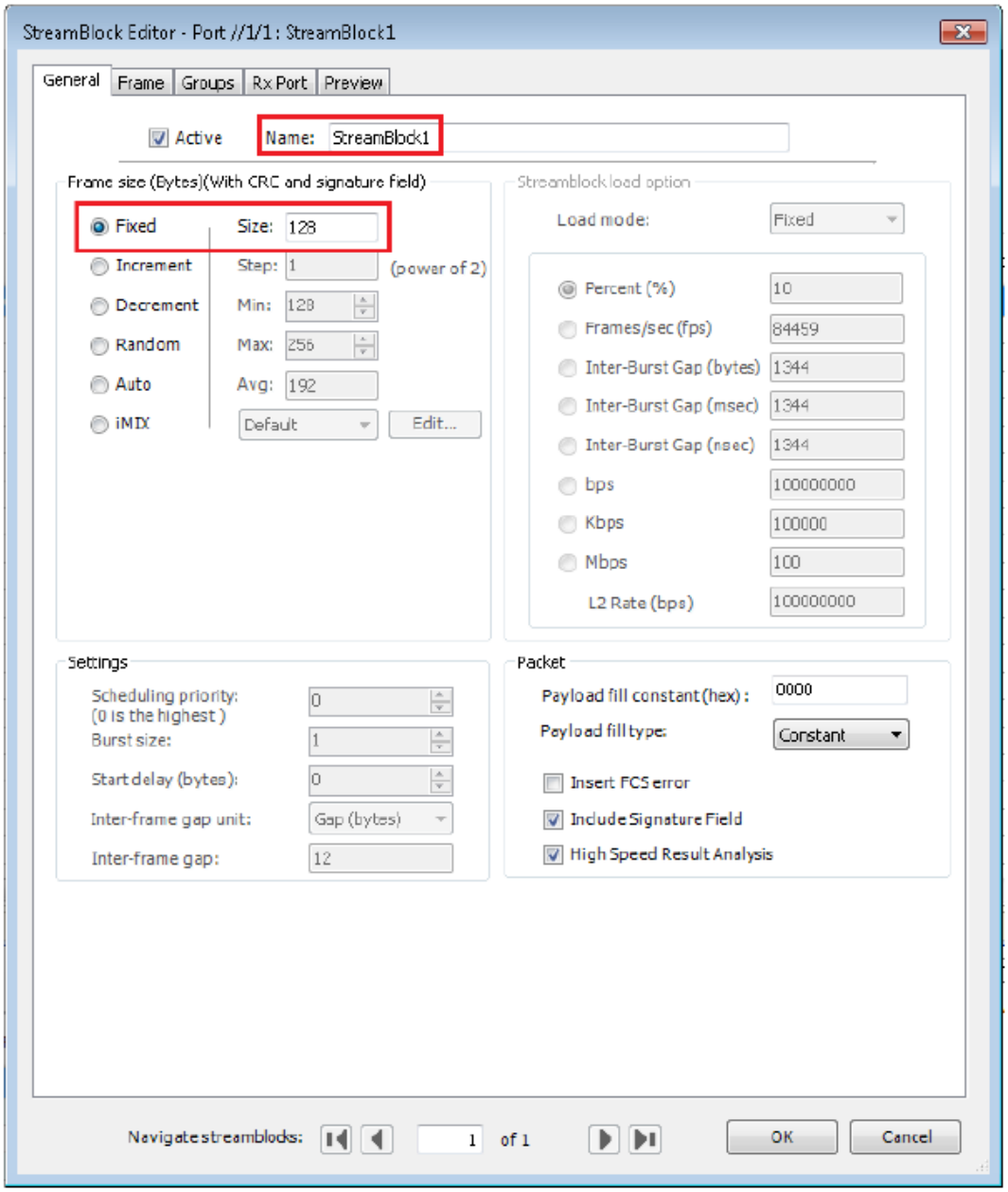
10. Close FlashPro Express or in the Project tab, click Exit.

Appendix 2: Running the Demo Design Using Spirent Test Center

The following steps describe how to run the CoreTSE MAC loopback demo using the Spirent test center:

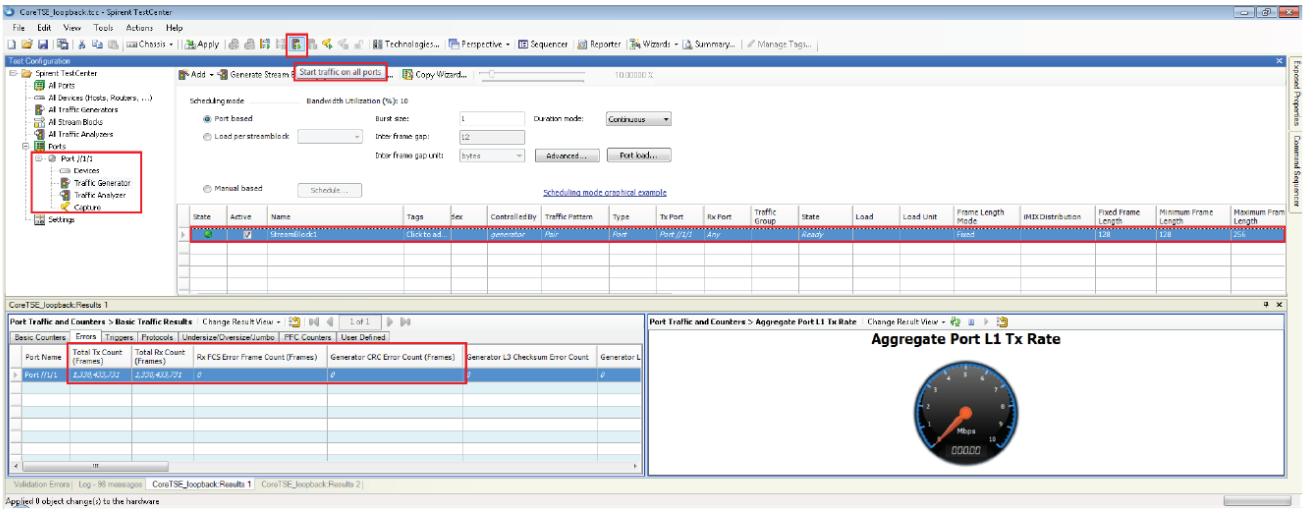
1. Connect the IGLOO2 Evaluation Kit to the slot 1 Ethernet port on the Spirent test equipment using the RJ45 cable.
2. In the host PC, open the Spirent test center configurator.
3. Add port (Ethernet) in the Spirent test center, as shown in the following figure.

Figure 18 • **Spirent Test Center Stream Block – General Tab**



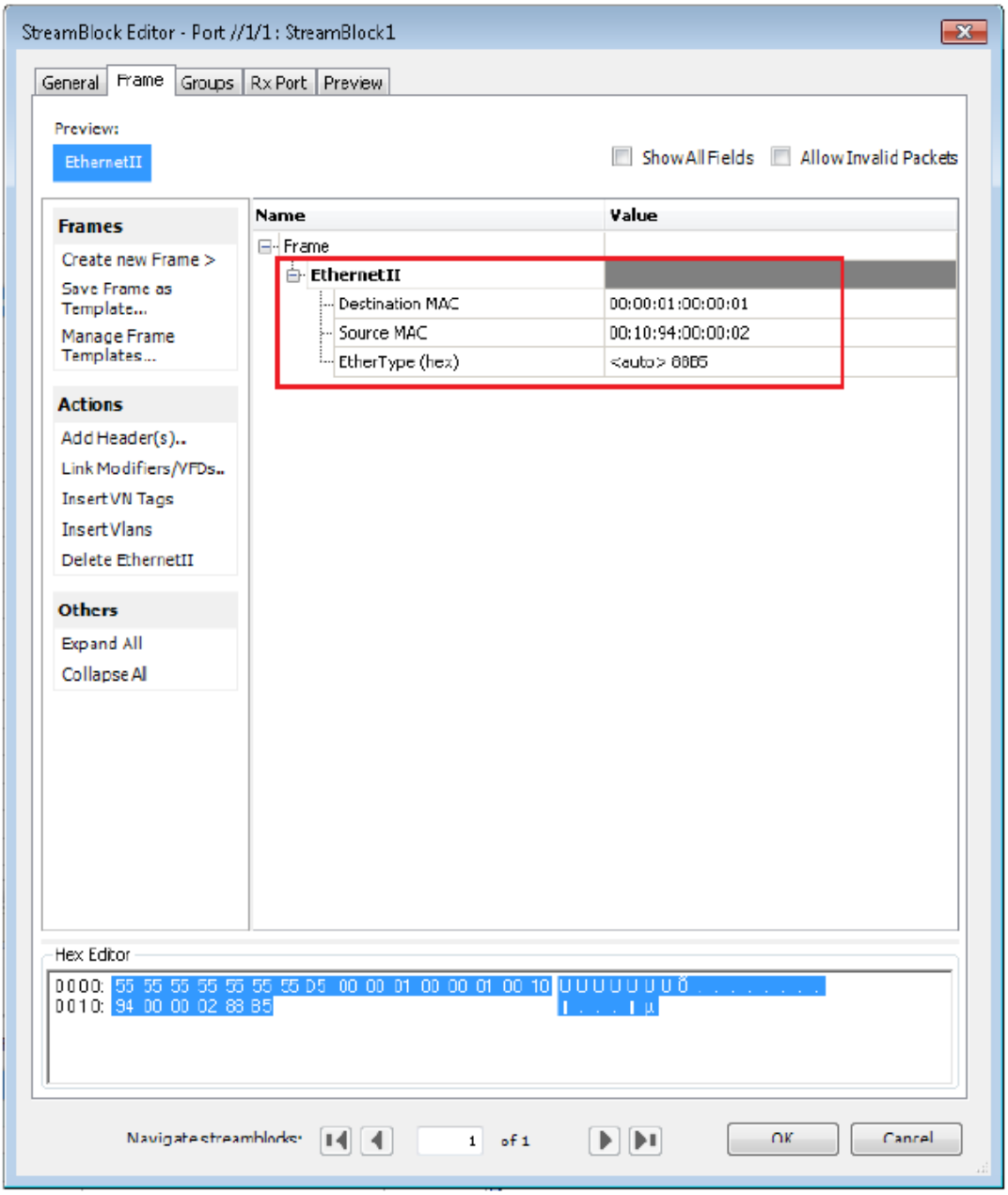
4. Click Traffic generator under Port, add packet information in the stream block editor, and click OK as shown in Figure 20, page 19.

Figure 19 • **Spirent Test Center**



5. Click Start traffic on all ports, as shown in Figure 20. Ethernet packets are transmitted and received on port1 through the RJ45 cable.
6. Observe the Total TX, RX, RX FCS, and CRC error counts. Figure 20 shows the total TX, RX, RX FCS, and CRC error count information in the Spirent test center. 0 indicates no loss in the packet transmission and reception.

Figure 20 • **Spirent Test Center Stream Block – Frame Tab**



Documents / Resources

	Microsemi DG0633 IGLOO2 FPGA CoreTSE MAC 1000 Base-T Loopback Demo [pdf] User Guide DG0633 IGLOO2 FPGA CoreTSE MAC 1000 Base-T Loopback Demo, DG0633, IGLOO2 FPGA CoreTSE MAC 1000 Base-T Loopback Demo, Base-T Loopback Demo

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