Microsemi AC264 ProASIC Plus SSO and Pin Placement User Guide

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Introduction

Ground bounce and VDD bounce have always been present in digital integrated circuits. With the advance of technology and shrinking CMOS features, the speed of designs, I/O slew rates, and the size of I/O busses have increased significantly through the past few years. As a result, Simultaneously Switching Outputs (SSOs) and their effects on signal integrity have become an important factor in any digital circuit design. In addition to SSOs, the effects of Simultaneously Switching Registers (SSRs) are discussed in this document. When SSOs and SSRs are not properly designed into a board layout or digital IC, they may lead to data corruption and system failure.

Simplified Design Rules

In order to prevent SSO-induced issues in modern digital systems, designers must compromise an elegant board layout for reliability. An elegant board layout may include practices such as placing all the inputs on one side of the chip and all the outputs on the opposite side, and placing all bus pins next to each other to make the board layout simple. In today's digital systems, utilizing modern FPGAs, such as Microsemi® system-on-chip (SoC) Products Group Pro ASICPLUS®, this may result in data corruption due to ground bounce, VDD bounce, or crosstalk. To design a reliable system for Pro ASICPLUS FPGAs, designers should follow three simple rules:

1. Identify the SSOs of the design as early in the design cycle as possible and spread them out across the entire die periphery. Avoid clusters of adjacent SSO I/So.
2. Identify sensitive (and usually asynchronous) system signals, and shield them from SSOs (specific shielding techniques are discussed later in this document).
3. When creating the chip design, stagger the timing of SSOs such that a maximum of 12 outputs switch within a 1 ns window. This may require instantiation of delay buffers to achieve a large timing spread.

Furthermore, relatively large lead inductance in PQFP and CQFP packages makes these packages more vulnerable to SSO and hence undesirable for high-speed designs or designs with more than 12 SSOs. FBGA or BGA packages are preferred in such designs since they show much better performance in the presence of SSOs. By following the above three rules, designers can create a reliable system free from the effects of SSOs. The following sections cover the effects of SSOs, specific SSO limits, and mitigation techniques for designs that do not comply with these recommendations.

Basics of the SSO Effect

The total number of SSOs for each bus is determined by identifying the outputs that are synchronous to a single

clock domain, have their clock-to-out times within 1 ns of each other, and are placed next to each other on die pads on both sides of a quiet I/O, as shown in Figure 1. The SSOs may affect the quiet I/O if the total number of SSOs on both sides of the quiet I/O exceeds the Pro ASICPLUS SSO recommendation. It is important to note that the SSO should be identified on the die pads, not the package pins, since neighboring package pins are not necessarily next to each other on the die (e.g., for BG and FG packages). This can be determined by using Multi View Navigator (MVN) in the Designer software or die/package bonding diagrams provided by Microsemi. However, when routing traces on the board, it is important to note that SSOs on neighboring package pins may affect the quiet I/O surrounded by the SSOs on the board by crosstalk or coupling.

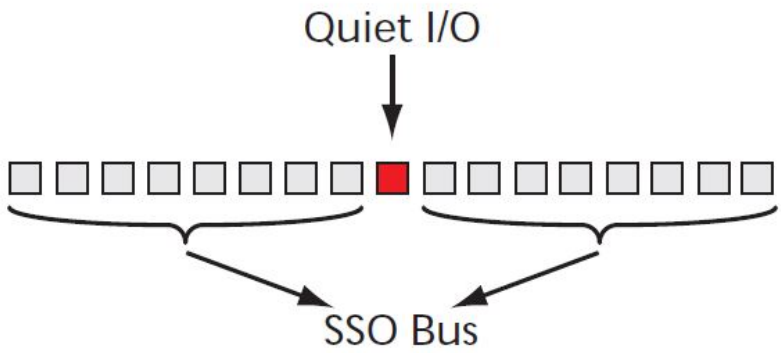

Figure 1: Basic Block Diagram of a Quiet I/O Surrounded by an SSO Bus.

SSO Effect on Power and Ground for Output

If SSOs toggle in one direction (high to low or low to high), a significant amount of current will start to flow to the ground or VDD pins within a short amount of time. The current is the sum of the output buffers' CMOS sinking or sourcing current at the same time. The quick jump in the current causes a voltage drop on the parasitic inductance between the board and die VDD and ground ($V = L \times di/dt$). For more information about the ground and VDD bounce phenomenon please refer to the Simultaneous Switching Noise and Signal Integrity application note. The local fluctuations on the VDD and ground level may cause the logic on quiet outputs that are measured with respect to the fluctuating VDD and ground to be misinterpreted in the form of unwanted glitches in the logical value. This effect is easily prevented by following design guidelines 1, 2, or 3 in "Simplified Design Rules" on page 1.

SSO Effect on Inputs for PQFP and CQFP Packages

PQFP and CQFP packages have inferior inductance and capacitance characteristics compared to BGA packages. Also, smaller die sizes have less capacitance to mitigate the effects of SSOs. On small Pro ASICPLUS devices in PQFP and CQFP packages, a large number of SSOs will generate an increased level of noise on the device's internal I/O supplies. This noise may affect the threshold levels of the input stage transistors and may result in increased fall times on signals driven from input buffers into the FPGA array. This effect is easily eliminated by following design rule 3 in "Simplified Design Rules" on page 1.

Shielding from SSO

When exposure of sensitive signals (e.g., asynchronous reset) to SSOs is inevitable, these signals need to be shielded from the SSOs to mitigate the unwanted effects. Shielding is basically separating the sensitive signals from SSOs using neighboring pins. Figure 2 shows a basic block diagram depicting a quiet output in the presence of an SSO bus with pins.

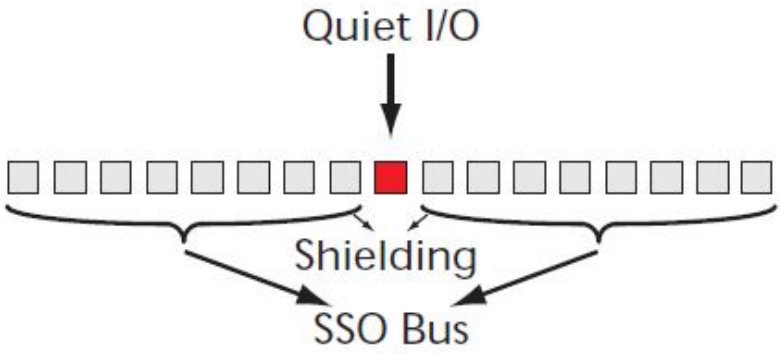

Figure 2: Shielding Scheme.

There are different shielding techniques that can be used to protect the quiet I/O from the SSO bus. Before considering these techniques, review the concepts of “Virtual Ground” and “Virtual VDD”

Virtual Ground
A virtual ground is a ground pin that is implemented by designers using regular I/O ports. To implement a virtual ground, instantiate an output buffer (with highest drive strength and slew rate) in the design. Tie the input of this output buffer to zero within the design so that the output buffer is constantly driving out to the ground level.

Virtual VDD
A virtual VDD is implemented in a similar fashion to a virtual ground. The only difference is that in the case of a virtual VDD, the input of the output buffer is internally tied to logic high.
In general, there are two shielding methods recommended by SoC Products Group: a) using GND pins or virtual grounds, and b) using any VDDP, GND, VDD, unused I/O, used (but not sensitive) I/O, or any combination of these pins.

Shielding Using GND or Virtual Ground Pins
When shielding sensitive quiet I/Os from an SSO bus, GND or virtual ground pins can be used if required. In this case, two or three GND or virtual ground pins should be placed on each side of the quiet I/O. The shielding pins should be connected externally to the board-level ground. To prevent any board-level coupling or crosstalk noise on the quiet I/Os, the shielding pins should be routed on the board alongside the SSO bus for the whole length of the SSO traces on the same board layer. These shielding traces should be connected to board ground on both ends of their length.

Shielding Using Other Pins
The type of the shielding pins is not restricted to GND or virtual grounds. The shielding pins can also be VDD, VDDP, virtual VDD, unused I/Os, or used I/Os that are not sensitive to SSO effects (e.g., outputs driving LEDs).

Basics of the SSR Effect

When a design has a very large number of SSRs, enough noise may be generated to affect the delay of output buffers. However, the amount of delay introduced is within the output timing margin when the percentage of SSRs (%SSR) is 50% or less. %SSR is calculated by multiplying the register utilization percentage (%Register) for the design on a given array size by the percentage of registers that change state on a given clock edge (%Toggle). Typical register utilization for a design will not exceed 25% (the Designer compile report provides the actual value for a design), and a typical toggle rate will not exceed 20%. Therefore a typical maximum %SSR is 5%, well within the 50% guideline. %SSR = %Register × %Toggle

SSO Data

This section provides SSO guidelines for Pro ASICPLUS devices and packages. The criteria is a glitch with maximum amplitude of 1.25 V and maximum pulse width of 2 ns. SSOs are defined as the number of Simultaneously Switching Outputs within a 1 ns window. Refer to Table 1 for more information.

Table 1: SSO Recommendations for Pro ASICPLUS Devices.

Devices	Packages	SSO Recommendations
All ProASICPLUS devices	PBGA, FBGA, CCGA, LGA, TQFP	32 SSOs around a quiet output for High Slew Rate. >40 SSOs around a quiet output for Low Slew Rate.
APA600 or larger	PQFP, CQFP	32 SSOs around a quiet output for High Slew Rate. >40 SSOs around a quiet output for Low Slew Rate.
APA450 or smaller	PQFP, CQFP	12 SSOs, independent of location and slew rate.

Mitigating SSO Effects

Mitigating SSO Effect on Outputs

Any effort to mitigate the SSO effect starts with eliminating the SSOs themselves. As described in “Basics of the SSO Effect”, the SSOs should be spread across the die pads to avoid concentration of a large SSO bus in one area of the die. If possible, the clock-to-out timing of output busses should be staggered to reduce the number of SSOs placed in vicinity of quiet outputs. The SSOs closest to the quiet output should have more than 1 ns timing separation from the other SSO bits of that bus so they act as a shield, not contributors. If placement of sensitive outputs close to the SSO bus is inevitable, these outputs should be shielded from the bus. Whenever shielding is required, it is recommended to use GND or virtual ground pins as shielding. However, it is acceptable to use other shielding pins to protect the sensitive outputs from SSOs. Segmenting SSO busses into smaller sections helps to mitigate the SSO effect. Segmentation of the SSO bus can be effected by inserting spacers among the SSO bus pins when placed on the die pads as shown in Figure 3. The spacers can be GND or virtual ground, VDD or virtual VDD, unused I/Os, or used I/Os that are not assigned to sensitive signals and do not toggle frequently or synchronously with the SSOs (e.g., signals driving LEDs).

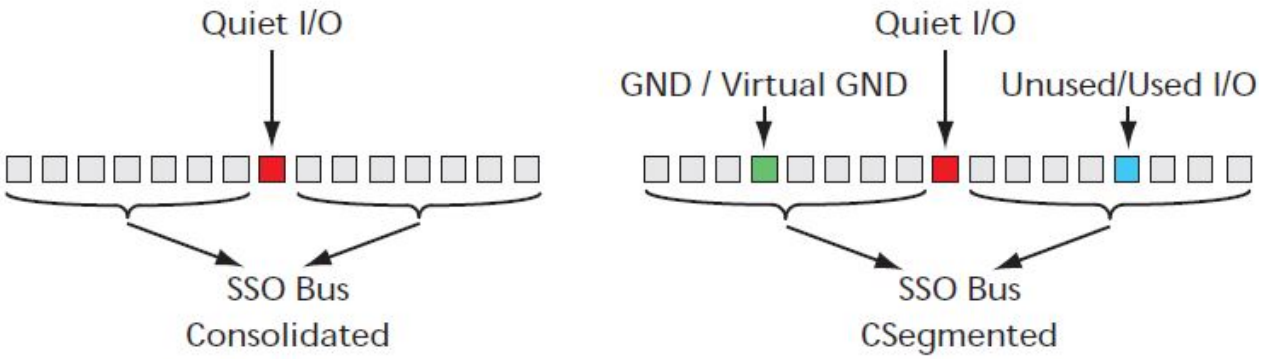

Figure 3: Example of Consolidated and Segmented SSO Bus.

Additionally, FG and BG packages show much better characteristics with respect to SSO effects than PQ or TQ packages. Therefore, for relatively high-speed design or designs that have significant numbers of wide output busses, FG or BG packages are strongly recommended. In addition to the digital design and the device package type, board-level design is a key parameter in mitigating the SSO effect. A well-designed PCB capable of providing clean voltage supplies to the FPGA is less susceptible to noise and therefore performs better in mitigating SSO effects.

Mitigating SSO Effect on Inputs

As discussed in “SSO Data”, SSOs on small APA devices (APA450 or smaller) in PQFP and CQFP packages may affect device inputs. The SSOs do not need to be adjacent to the input for this phenomenon to occur. To prevent this, it is first imperative that the PCB layout be clean, with adequate power supply decoupling. General PCB layout recommendations can be found in the Board Level Considerations application note. Second, the

number of SSOs across the device within a 1 ns window should be reduced to 12 or less. The effects of this are worse at cold temperatures, so this recommendation has been tested down to –40°C on a 50 MHz input clock.

Conclusion

As digital designs get faster and larger, SSOs and their effects become a more critical part of system signal integrity analysis. This application note provides a set of data characterizing the effect of SSOs on inputs and sensitive outputs in Pro ASICPLUS FPGAs. In the presence of SSOs, their effects should be accounted for or mitigated to ensure the functionality of the design. SSO mitigation techniques should be conducted in parallel on chip-level and board-level design, as they both play important roles in providing a clean digital system.

Related Documents

Application Notes

- **Board Level Considerations**
  www.microsemi.com/soc/documents/ALL_AC276_AN.pdf
- **Simultaneous Switching Noise and Signal Integrity**
  www.microsemi.com/soc/documents/SSN_AN.pdf

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes
Revision 1 (April 2012)	Updated links listed under sections “Mitigating SSO Effect on Inputs” and “Application N otes” (SAR 38043).

Note:
The revision number is located in the part number after the hyphen. The digits following the slash indicate the month and year of publication.

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Documents / Resources

	**Microsemi AC264 ProASIC Plus SSO and Pin Placement** [pdf] User Guide AC264 ProASIC Plus SSO and Pin Placement, AC264, ProASIC Plus SSO and Pin Placement, Plus SSO and Pin Placement, Pin Placement

References

- **Microsemi | Semiconductor & System Solutions | Power Matters**