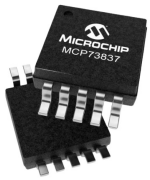
MICROCHIP
Viterbi Decoder



MICROCHIP Viterbi Decoder User Guide

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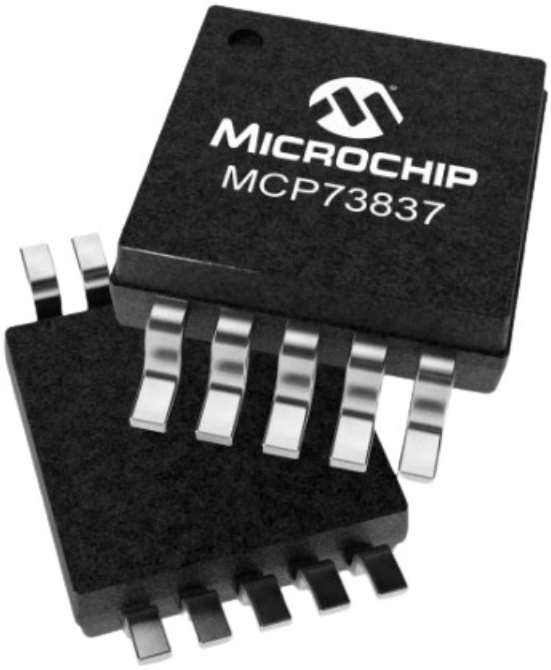


Specifications

- **Algorithm:** Viterbi Decoder
- **Input:** 3-bit or 4-bit soft or hard input
- **Decoding Method:** Maximum Likelihood
- **Implementation:** Serial and Parallel
- **Applications:** Mobile phones, satellite communications, digital television

Product Usage Instructions

The Serial Viterbi Decoder processes input bits individually in a sequential manner. Follow these steps to use the Serial Decoder:

- Provide the input bits sequentially to the decoder.
- The decoder will update path metrics and make decisions for each bit.
- Understand that the Serial Decoder may be slower but offers reduced complexity and lower resource usage.
- Use the Serial Decoder for applications prioritizing size, power consumption, and cost over speed.
- The Parallel Viterbi Decoder processes multiple bits concurrently. Here’s how to utilize the Parallel Decoder:
- Simultaneously provide multiple bits as input to the decoder for parallel processing.
- The decoder updates various path metrics in parallel, resulting in faster processing.
- Note that the Parallel Decoder offers high throughput at the expense of increased complexity and resource usage.
- Choose the Parallel Decoder for applications requiring fast processing and high throughput, such as real-time communication systems.

FAQ

Q: What are convolutional codes?

A: Convolutional codes are error-correcting codes widely used in communication systems to protect against transmission errors.

Q: How does the Viterbi Decoder work?

A: The Viterbi Decoder utilizes the Viterbi algorithm to identify the most probable sequence of transmitted bits based on the received signal, minimizing decoding errors.

Q: When should I choose a Serial Viterbi Decoder over a Parallel one?

A: Opt for a Serial Decoder when prioritizing reduced complexity, lower resource usage, and cost efficiency. It is suitable for applications where speed is not the primary concern.

Q: In what applications is the Viterbi Decoder commonly used?

A: The Viterbi Decoder is widely used in modern communication systems such as mobile phones, satellite communications, and digital television.

Introduction

The Viterbi Decoder is an algorithm used in digital communication systems to decode convolutional codes. Convolutional codes are error-correcting codes that are widely used in communication systems to protect against errors introduced during transmission.
The Viterbi Decoder identifies the most probable sequence of transmitted bits based on the received signal by using the Viterbi algorithm, a dynamic programming approach. This algorithm considers all potential code paths to calculate the most probable bit sequence based on the received signal. It then selects the path with the highest likelihood.
The Viterbi Decoder is a maximum likelihood decoder, which minimizes the probability of error in decoding the received signal and is implemented in Serial, occupying a small area, and in Parallel for higher throughput. It is widely used in modern communication systems, including mobile phones, satellite communications, and digital television. This IP accepts 3-bit or 4-bit soft or hard input.
The Viterbi algorithm can be implemented using two main approaches: Serial and Parallel. Each approach has distinct characteristics and applications, which are outlined as follows.
Serial Viterbi Decoder
Serial Viterbi Decoder processes input bits individually, sequentially updating path metrics and making decisions for each bit. However, due to its serial processing, it tends to be slower compared to its Parallel counterpart. Serial Decoder requires 69 clock cycles to generate an output due to its sequential updating of all possible state metrics, and the necessity to trace back through the trellis for each bit, resulting in extended processing time.
The advantage of using a Serial decoder lies in its typically reduced complexity and lower hardware resource usage, compared to a Parallel decoder. This makes it an advantageous option for applications in which size, power consumption, and cost are more critical than speed.
Parallel Viterbi Decoder
Parallel Viterbi Decoder is designed to concurrently process multiple bits. This is achieved by employing parallel processing methodologies to simultaneously update various path metrics. Such parallelism results in a significant reduction in the number of clock cycles needed to generate an output, which is 8 clock cycles.
The speed of the Parallel Decoder comes at the cost of increased complexity and resource usage, requiring more hardware to implement the parallel processing elements, which can increase the size and power consumption of the decoder. For applications requiring high throughput and fast processing, such as real-time communication systems, the Parallel Viterbi Decoder is often preferred.
In summary, the decision between using a Serial and Parallel Viterbi Decoder depends on the specific requirements of the application. In applications that require minimal power, cost, and speed, a Serial decoder is typically appropriate. However, for applications demanding high speed and high throughput, where performance is

critical, a Parallel decoder is the preferred option, even though it is more complex and requires more resources.

Summary
The following table lists a summary of the Viterbi Decoder IP characteristics.
Table 1. Viterbi Decoder Characteristics

Core Version	This document applies to Viterbi Decoder v1.1.
Supported Device Families	• PolarFire® SoC • PolarFire
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Licensing	The Viterbi Decoder encrypted RTL is freely available with any Libero license. **Encrypted RTL:** A complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout are performed with Libero software.

Features
Viterbi Decoder IP has the following features:

- Supports soft input widths of 3-bit or 4-bit
- Supports Serial and Parallel architecture
- Supports user-defined traceback lengths, and the default value is 20
- Supports unipolar and bipolar data types
- Supports code rate of 1/2
- Supports constraint length which is 7

Installation Instructions

The IP core must be installed to the IP Catalog of Libero® SoC software automatically through the IP Catalog update function in the Libero SoC software, or it is manually downloaded from the catalog. Once the IP core is installed in Libero SoC software IP Catalog, it is configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Device Utilization and Performance (Ask a Question)
The resource utilization for Viterbi Decoder is measured using the Synopsys Synplify Pro tool, and the results are summarized in the following table.
Table 2. Device and Resource Utilization

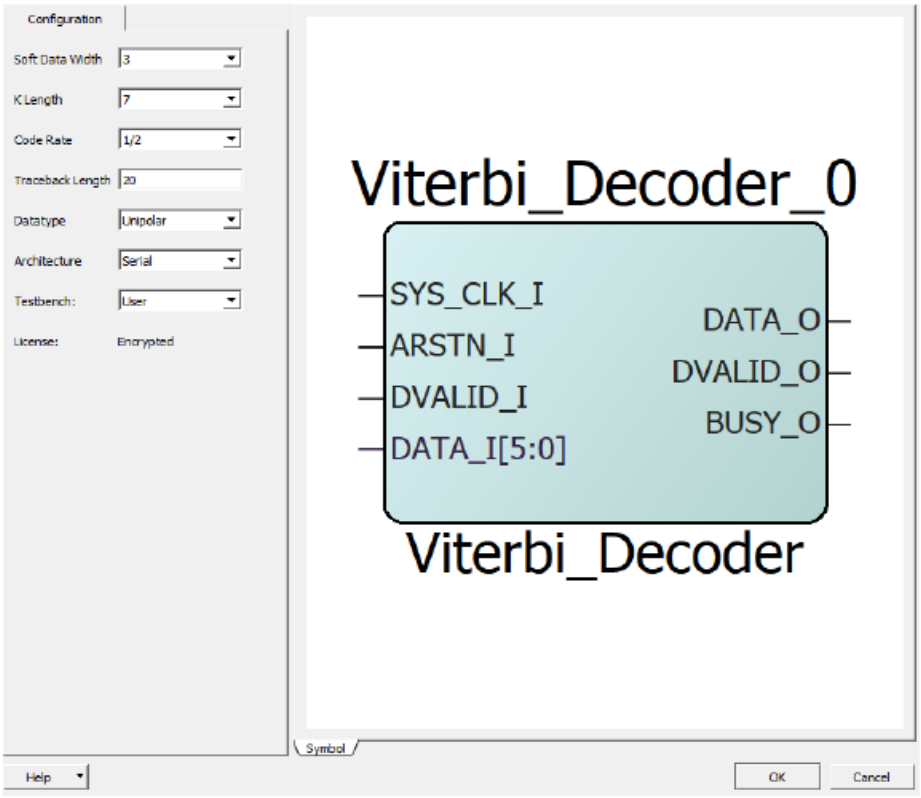
Device Details		Data Type	Architecture	Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device			LUTs	DFF		LSRAM	uSRAM		
PolarFire® SoC	MPFS250T	Unipolar	Serial	416	354	200	3	0	0	0
		Bipolar	Serial	416	354	200	3	0	0	0
		Unipolar	Parallel	13784	4642	200	0	0	0	0
		Bipolar	Parallel	13768	4642	200	0	0	0	1
PolarFire	MPF300T	Unipolar	Serial	416	354	200	3	0	0	0
		Bipolar	Serial	416	354	200	3	0	0	0
		Unipolar	Parallel	13784	4642	200	0	0	0	0
		Bipolar	Parallel	13768	4642	200	0	0	0	1

Important: The design is implemented using Viterbi Decoder by configuring the following GUI parameters:

- Soft Data Width = 4
- K Length = 7
- Code Rate = ½
- Traceback Length = 20

Viterbi Decoder IP Configurator

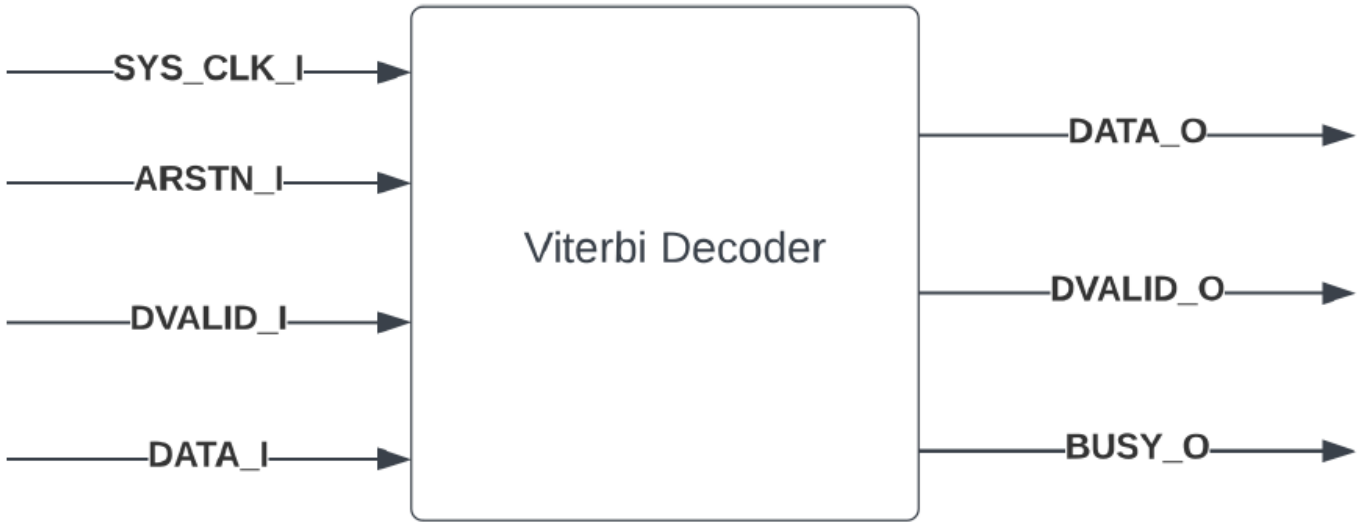
Viterbi Decoder IP Configurator (**Ask a Question**)
This section provides an overview of the Viterbi Decoder Configurator interface and its various components.
The Viterbi Decoder Configurator provides a graphical interface to configure parameters and settings for a Viterbi Decoder IP core. It allows the user to select parameters such as Soft Data Width, K Length, Code Rate, Traceback Length, Datatype, Architecture, Testbench, and License. The key configurations are described in Table 3-1.
The following figure provides a detailed view of the Viterbi Decoder Configurator interface.
Figure 1-1. Viterbi Decoder IP Configurator



The interface also includes OK and Cancel buttons for confirming or discarding the configurations made.

Functional Description

The following figure shows the hardware implementation of the Viterbi Decoder.
Figure 2-1. Hardware Implementation of Viterbi Decoder



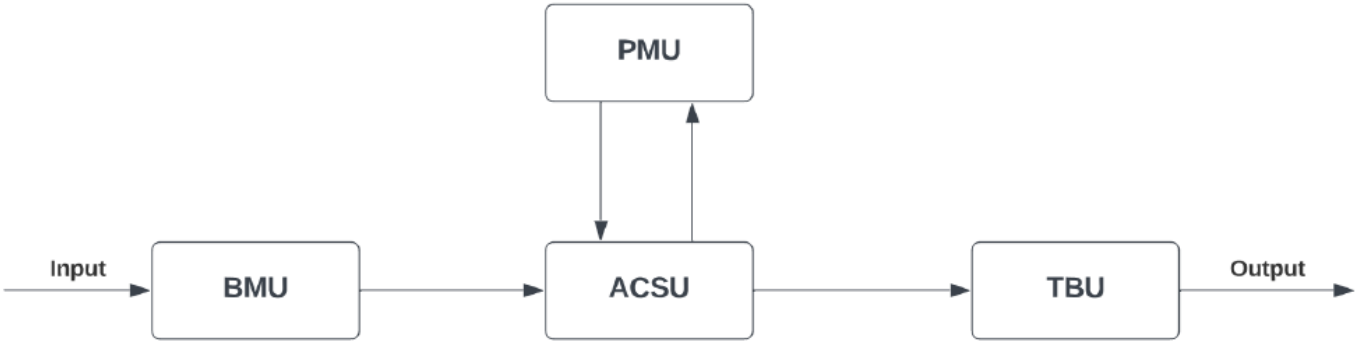
This module works on DVALID_I. When DVALID_I is asserted, the respective data is taken as input, and the process starts. This IP has a history buffer and based on that selection, IP takes the selected buffer number of DVALID_Is + Some clock cycles to generate the first output. By default, the history buffer is 20. The latency between the input and output of the Parallel Viterbi Decoder is 20 DVALID_Is + 14 Clock Cycles. The latency between the input and output of the Serial Viterbi Decoder is 20 DVALID_Is + 72 Clock Cycles.

Architecture (**Ask a Question**)
Viterbi Decoder retrieves the data initially given to the Convolutional Encoder by finding the best path through all possible encoder states. For a constraint length of 7, there are 64 states. The architecture consists of the following

major blocks:

- Branch Metric Unit (BMU)
- Path Metric Unit (PMU)
- Trace Back Unit (TBU)
- Add Compare Select Unit (ACSU)

The following figure shows the Viterbi Decoder architecture.
Figure 2-2. Viterbi Decoder Architecture



The Viterbi Decoder consists of three internal blocks which are explained as follows:

1. **Branch Metric Unit (BMU):** The BMU calculates the discrepancy between the received signal and all potential transmitted signals, using metrics such as Hamming distance for binary data or Euclidean distance for advanced modulation schemes. This calculation assesses the similarity between the received and possible transmitted signals. The BMU processes these metrics for each received symbol or bit and forwards the results to the Path Metric Unit.
2. **Path Metric Unit (PMU):** The PMU which is also known as the Add-Compare-Select (ACS) unit, updates path metrics by processing branch metrics from the BMU. It keeps track of the best path's cumulative metric for each state in the trellis diagram (a graphical representation of the possible state transitions). The PMU adds the new branch metric to the current path metric for each state, compares all paths leading to that state, and selects the one with the lowest metric, indicating the most probable path. This selection process is carried out at each stage of the trellis, resulting in a collection of the most likely paths, known as survivor paths, for each state.
3. **Traceback Unit (TBU):** The TBU is responsible for identifying the most probable sequence of states, following the processing of received symbols by the PMU. It accomplishes this by retracing the trellis from the final state with the lowest path metric. The TBU initiates from the end of the trellis structure and traces back through the survivor paths using pointers or references, to determine the most probable transmitted sequence. The length of the traceback is determined by the constraint length of the convolutional code, impacting both the decoding latency and complexity. Upon completing the traceback process, the decoded data is presented as output, usually with the appended tail bits removed, which were initially included to clear the convolutional encoder.

The Viterbi Decoder uses these three units to accurately decode the received signal into the original transmitted data, by correcting any errors that may have occurred during the transmission.
Renowned for its efficiency, the Viterbi algorithm is the standard method for decoding convolutional codes within communication systems.
Two data formats are available for soft coding: unipolar and bipolar. The following table lists the values and corresponding descriptions for 3-bit soft input.

Table 2-1. 3-bit Soft Inputs

Description	Unipolar	Bipolar
Strongest 0	000	100
Relatively strong 0	001	101
Relatively weak 0	010	110
Weakest 0	011	111
Weakest 1	100	000
Relatively weak 1	101	001
Relatively strong 1	110	010
Strongest 1	111	100

The following table lists the standard convolution code.
Table 2-2. Standard Convolution Code

Constraint Length	Output Rate = 2	
	Binary	Octal
7	1111001	171
	1011011	133

Viterbi Decoder Parameters and Interface Signals (Ask a Question)
This section discusses the parameters in the Viterbi Decoder GUI configurator and I/O signals.

Configuration Settings (Ask a Question)
The following table lists the configuration parameters used in the hardware implementation of Viterbi Decoder. These are generic parameters and vary as per the requirement of the application.
Table 3-1. Configuration Parameters

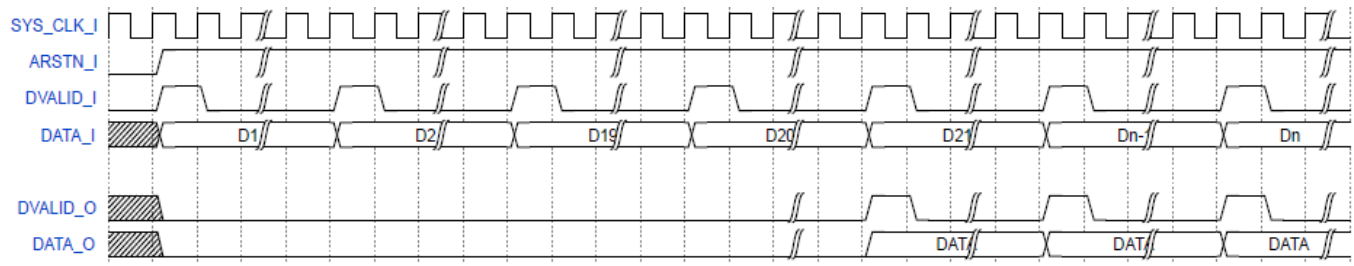
Parameter Name	Description	Value
Soft Data Width	Specifies the number of bits used to represent the soft input data width	User selectable which supports 3 and 4 bits
K Length	K is the constraint length of the convolutional code	Fixed to 7
Code Rate	Indicates the ratio of input bits to output bits	1/2
Traceback Length	Determines the depth of the trellis used in the Viterbi algorithm	User-defined value and by default, is 20
Data Type	Allows users to select the input data type	User-selectable and supports the following options: • Unipolar • Bipolar
Architecture	Specifies the type of implementation architecture	Supports the following implementation types: • Parallel • Serial

Inputs and Outputs Signals (Ask a Question)
The following table lists the input and output ports of the Viterbi Decoder IP.
Table 3-2. Input and Output Ports

Signal Name	Direction	Width	Description
SYS_CLK_I	Input	1	Input clock signal
ARSTN_I	Input	1	Input reset signal (Asynchronous active-low reset)
DATA_I	Input	6	Data input signal (MSB 3-bit IDATA, LSB 3-bit QDATA)
DVALID_I	Input	1	Data valid input signal
DATA_O	Output	1	Viterbi Decoder data output
DVALID_O	Output	1	Data valid output signal

Timing Diagrams

This section discusses the timing diagrams of the Viterbi Decoder.
The following figure shows the timing diagram of Viterbi Decoder which applies to both Serial and Parallel mode configuration.
Figure 4-1. Timing Diagram



- Serial Viterbi Decoder requires a minimum of 69 clock cycles (Throughput) to generate the output.
- To calculate the latency of the Serial Viterbi Decoder, use the following equation:
- Number of history buffer times DVALIDs + 72 clock cycles
- For Example, If the History Buffer length is set to 20, then
- Latency = 20 Valids + 72 Clock Cycles
- Parallel Viterbi Decoder requires a minimum of 8 clock cycles (Throughput) to generate the output.
- To calculate the latency of the Parallel Viterbi Decoder, use the following equation:
- Number of history buffer times DVALIDs + 14 clock cycles
- For Example, If the History Buffer length is set to 20, then
- Latency = 20 Valids + 14 Clock Cycles

Important: The timing diagram for Serial and Parallel Viterbi decoder is identical, with the exception of the number of clock cycles required for each decoder.

Testbench Simulation

A sample testbench is provided to check the functionality of the Viterbi Decoder. To simulate the core using the testbench, perform the following steps:

1. Open the Libero® SoC application, click Catalog > View > Windows > Catalog, and then expand Solutions-Wireless. Double-click Viterbi_Decoder, and then click OK. The documentation associated with IP is listed under Documentation.
   Important: If you do not see the Catalog tab, navigate to the View Windows menu, and then click Catalog to make it visible.
2. Configure the IP as per the requirement, as shown in Figure 1-1.
3. The FEC encoder must be configured to test the Viterbi Decoder. Open the Catalog and configure the FEC Encoder IP.
4. Navigate to Stimulus Hierarchy tab, and click Build Hierarchy.
5. On the Stimulus Hierarchy tab, right-click testbench (vit_decoder_tb(vit_decoder_tb.v [work])), and then click Simulate Pre-Synth Design > Open Interactively.

Important: If you do not see the Stimulus Hierarchy tab, navigate to View > Windows menu and click Stimulus Hierarchy to make it visible.
The ModelSim® tool opens with the testbench, as shown in the following figure.
Figure 5-1. ModelSim Tool Simulation Window

Figure 5-1. ModelSim Tool Simulation Window

Important

- If the simulation is interrupted due to the run-time limit specified in the.do file, use the run -all command to complete the simulation.
- After running the simulation, the testbench generates two files (fec_input.txt, vit_output.txt) and you can compare the two files for a successful simulation.

Revision History (Ask a Question)
The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 6-1. Revision History

Revision	Date	Description
B	06/2024	The following is the list of changes made in revision B of the document: • Updated the content of Introduction section • Added Table 2 in Device Utilization and Performance section • Added 1. Viterbi Decoder IP Configurator section • Added the content about the internal blocks, updated Table 2-1 and added Table 2-2 in 2.1. Architecture section • Updated Table 3-1 in 3.1. Configuration Settings section • Added Figure 4-1 and a Note in 4. Timing Diagrams section • Updated Figure 5-1 in 5. Testbench Simulation section
A	05/2023	Initial release

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