MICROCHIP V43 Resolver Interface User Guide

MICROCHIP V43 Resolver Interface
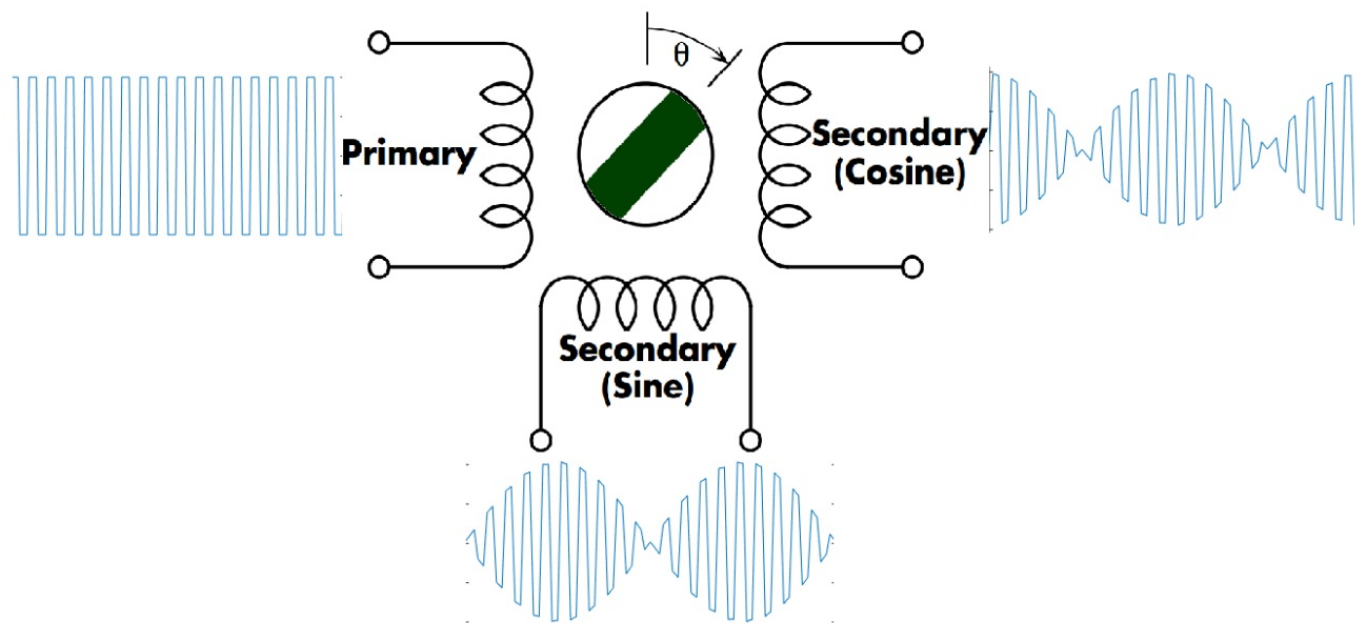
Contents

Introduction (Ask a Question)

A resolver is a position sensor or transducer which measures the absolute angular position of the rotating shaft to which it is attached.

The operating principle of a resolver is similar to the operating principle of a synchro. Resolvers are typically built like small motors with a rotor (attached to the shaft whose position is to be measured) and a stator (stationary part) which takes the excitation signals and produces the output signals. A resolver typically consists of a primary winding, also called excitation winding and two secondary windings called cosine and sine windings. The secondary windings are geometrically placed such that winding signals are cosine and sine function of rotor angle.

The following figure shows the signals generated by resolver.

Figure 1. Signal Generation in Resolver

Summary (Ask a Question)

Core Version	This document applies to Resolver Interface v4.3.
Supported Device Families	- PolarFire® SoC - PolarFire - RTG4™ - IGLOO® 2 - SmartFusion® 2
Supported Tool F low	Requires Libero® SoC v11.8 or later releases.
Licensing	Complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. Resolver interface is licensed with encrypted RTL that must be purchased separately. For more information, see Resolver Interface.

Features (Ask a Question)

Resolver Interface has the following key features:

- Provides a high-frequency signal for excitation
- Demodulates sine and cosine winding inputs
- Computes angle and speed

Implementation of IP Core in Libero® Design Suite (Ask a Question)

IP core must be installed to the IP Catalog of the Libero SoC software. This is installed automatically through the IP Catalog update function in the Libero SoC software, or the IP core can be manually downloaded from the catalog.
Once the IP core is installed in the Libero SoC software IP Catalog, the core can be configured, generated, and instantiated within the Smart Design tool for inclusion in the Libero project list.

Device Utilization and Performance (Ask a Question)

The following table lists the device utilization used for Resolver interface.

Table 1. Resolver Interface Utilization

| Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T	1815	909	200	0	0	2	0
PolarFire	MPF300T	1815	909	200	0	0	2	0
SmartFusion® 2	M2S150	1832	914	175	0	0	2	0

Important:

1. The data in this table is captured using typical synthesis and layout settings. CDR reference clocksource was set to Dedicated with other configurator values unchanged.
2. Clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers.

Functional Description (Ask a Question)

The following figure shows the block diagram of Resolver interface.

Figure 1-1. System-Level Block Diagram of Resolver Interface
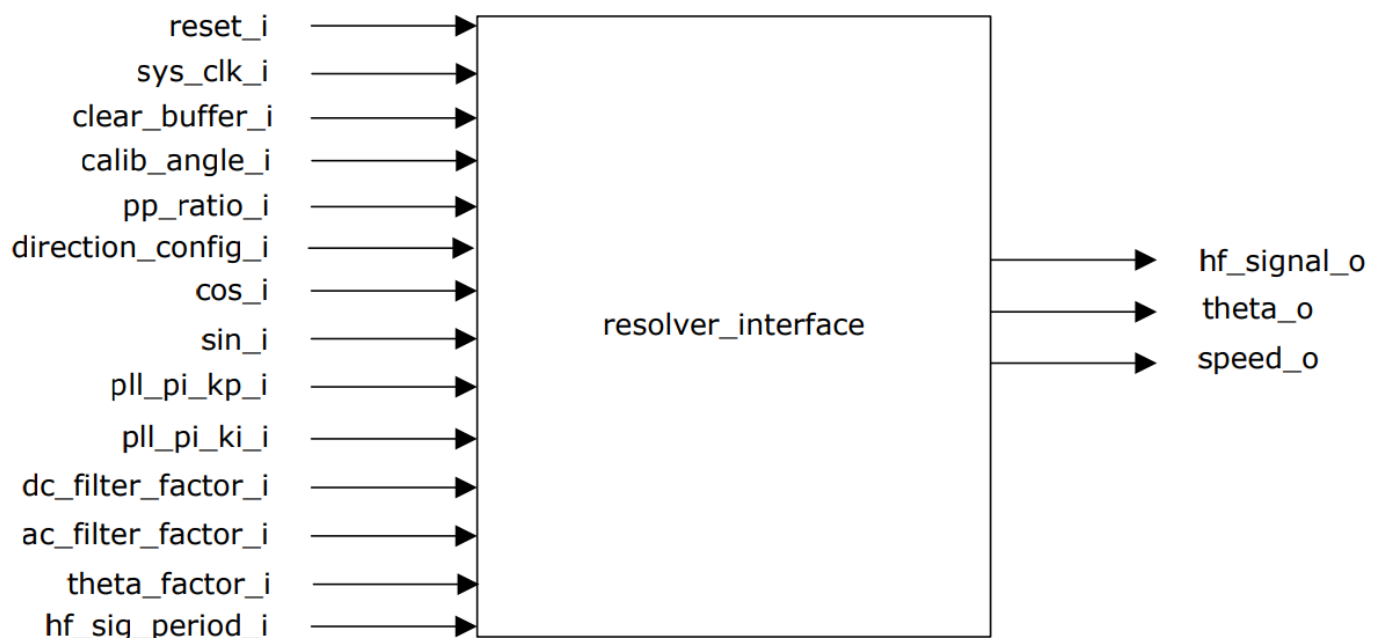
The resolver interface IP generates a square wave that is fed to the primary winding of the resolver. The frequency of the square wave can be configured through hf_sig_period_i input. The cos_i and sin_i signals from the secondary windings are demodulated and filtered to get effective cosine and sine signals. A Phase-Locked Loop (PLL) is used to extract angle and speed from cosine and sine signals.

The PLL uses a PI controller whose gains pll_pi_kp_i and pll_pi_ki_i can be tuned to get required response time. A higher value for gains results in quick response to angle and speed changes but can also induce noise in angle

and speed outputs.

In motor control application, the resolver zero position must be aligned with motor magnetic zero position. To achieve this, a calib_angle_i signal is used. During calibration process, the signal goes high and the motor is forced to align its rotor to magnetic zero position. The angle output is reset to zero during this period and is taken as reference for measuring absolute angle. A motor and resolver can have multiple pole pairs in which the motor control algorithm needs multiple theta transitions (3600) for one mechanical rotation of the rotor. This feature can be configured through the pp_ratio_i port, listed in Table 2-2.

The theta_factor constant is calculated by using the following equation. The calculated speed can be scaled to per unit using theta_factor_i.

EQ1

$$theta\_factor = \frac{18.12 \ * \ Rated \ Motor \ Speed(RPM)}{System \ Clock \ (MHz)}$$

The hf_sig_period input determines the frequency of square wave injected into resolver primary, calculated by using the following equation.

EQ2

$$hf\_sig\_period\_i = \frac{f_{sys\_clk}}{hf\_freq \times 2}$$

where,
hf_freq = Frequency of the square wave injected into resolver primary fsys_clk = Frequency of the system clock provided at sys_clk_i input

Resolver Interface Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the Resolver interface GUI configurator and I/O signals.

Configuration of GUI Parameters (Ask a Question)

The following table lists the description of the configuration parameter used in the hardware implementation of Resolver interface. These are generic parameters and can be varied as per the requirement of the application.

Table 2-1. Configuration Parameters

Signal Name	Description
g_NO_MCYCLE_PATH	The number of clock delays required before the multiplication product ready signal is asserted.

Input and Output Signals (Ask a Question)

The following table lists the input and output ports of Resolver interface.

Table 2-2. Inputs and Outputs of Resolver Interface

Signal Name	Direction	Description
reset_i	Input	Active low asynchronous reset signal to design
sys_clk_i	Input	System clock
clear_buffer_i	Input	When set to 1, internal speed filter buffer is cleared When set to 0, buffer is normally operated
calib_angle_i	Input	The IP enters calibration state when this signal goes high. The angle offset between the resolver zero and the motor magnetic zero is calculated in this state.
direction_config_i	Input	Specifies the direction of motor rotation
pp_ratio_i	Input	The ratio of number of motor poles to number of resolver poles expressed as exponent of 2. Example for motor poles 16, resolver poles 2, pp_ratio_i = 3; For motor poles 8, resolver poles 2, pp_ratio_i= 2; For motor poles 4, resolver poles 4, pp_ratio_i = 0.
cos_i	Input	Cosine winding input (from ADC)
sin_i	Input	Sine winding input (from ADC)
pll_pi_kp_i	Input	Proportional gain of PI controller used for PLL
pll_pi_ki_i	Input	Integral gain of PI controller used for PLL
dc_filter_factor	Input	Filter time constant of high-pass filter used to eliminate DC value from Sine and Cosine signals
ac_filter_factor	Input	Filter time constant of low-pass filter used to eliminate modulation wave frequency component for Sine and Cosine signals
theta_factor_i	Input	Theta factor constant, as calculated from **EQ1**
hf_sig_period_i	Input	Half the value of the high frequency square wave time period, as calculated from **EQ2**
hf_signal_o	Output	Square wave signal used to drive primary winding of resolver
theta_o	Output	Angle output of resolver; equivalent to motor electrical angle
speed_o	Output	Speed output of resolver IP

Timing Diagrams (Ask a Question)

This section discusses Resolver interface timing diagram.
The following figure shows the timing diagram of Resolver interface.

Figure 3-1. Resolver Interface Timing Diagram
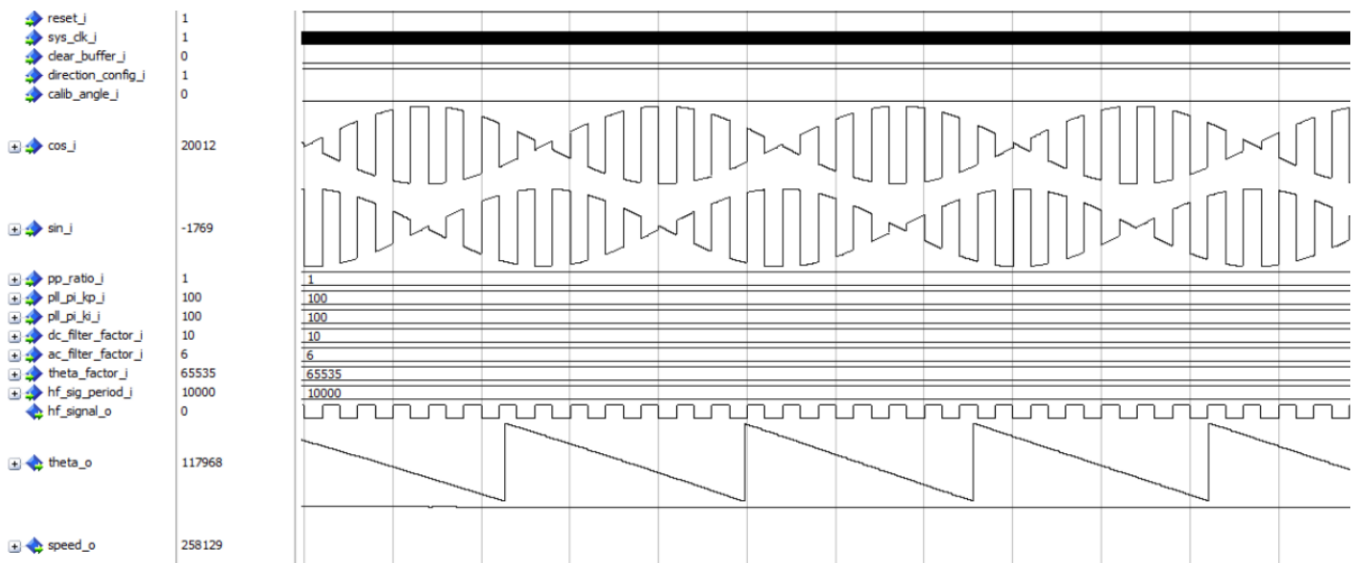
Testbench (Ask a Question)

A unified testbench is used to verify and test Resolver interface called as user testbench. Testbench is provided to check the functionality of the Resolver interface IP.
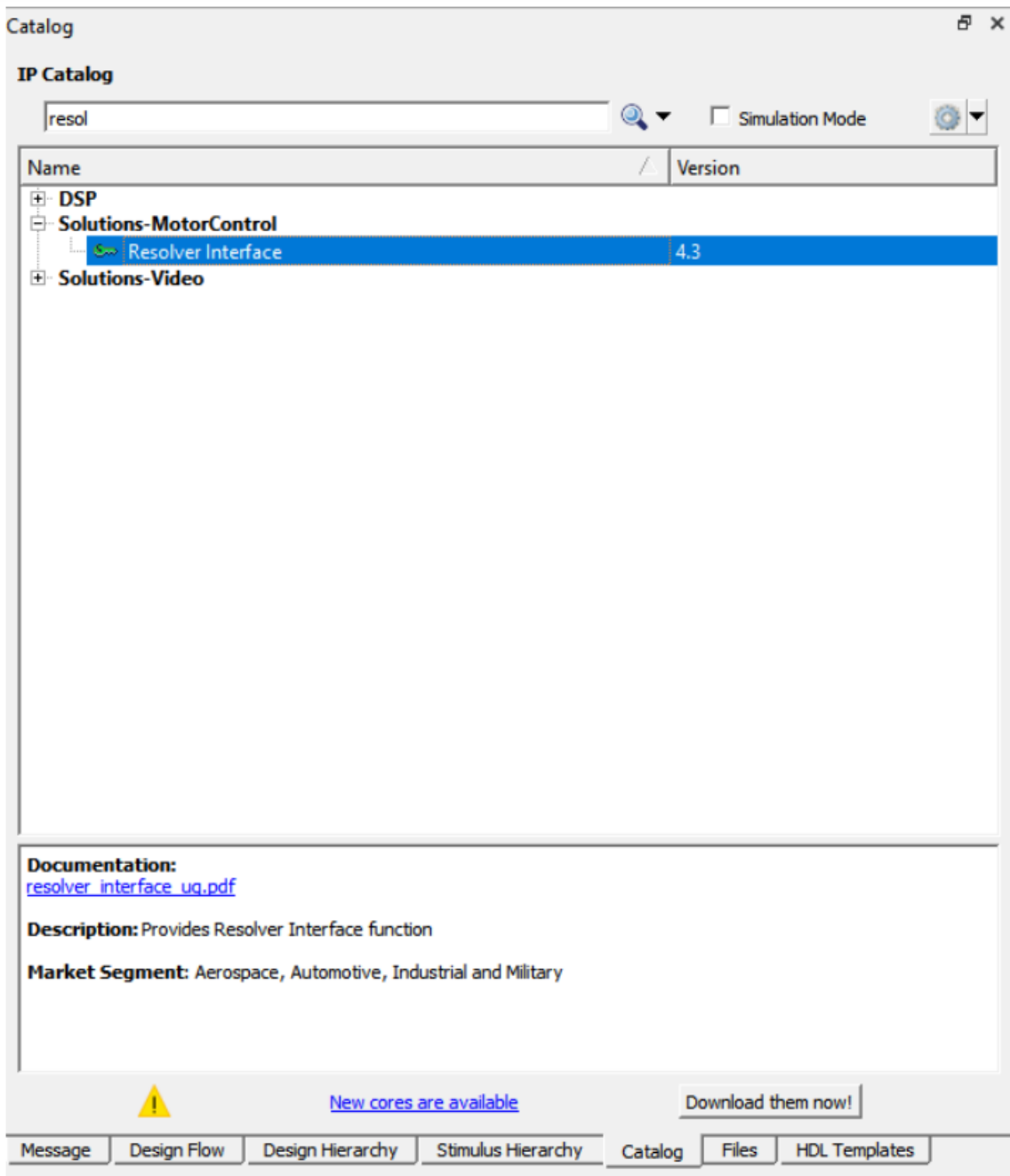
Simulation (Ask a Question)

The following steps describe how to simulate the core using the testbench:

1. Open Libero SoC Catalog tab, expand Solutions-Motor Control, double click Resolver Interface, and then click OK. The documentation associated with the IP are listed under Documentation.

   Important: If you do not see the Catalog tab, navigate to View > Windows menu and click Catalog to make it visible.

   **Figure 4-1. Resolver Interface IP Core in Libero SoC Catalog**

Catalog

IP Catalog

resol

☐ Simulation Mode

Name	/	Version
⊞ **DSP**		
⊟ **Solutions-MotorControl**		
⟜ Resolver Interface		4.3
⊞ **Solutions-Video**		

Documentation:
resolver_interface_ug.pdf

Description: Provides Resolver Interface function

Market Segment: Aerospace, Automotive, Industrial and Military

⚠ New cores are available   Download them now!

Message | Design Flow | Design Hierarchy | Stimulus Hierarchy | Catalog | Files | HDL Templates

2. On the Stimulus Hierarchy tab, select the testbench (resolver_interface_tb.v), right click and then click Simulate Pre-Synth Design > Open Interactively.

→ **Important:** If you do not see the Stimulus Hierarchy tab, navigate to View > Windows menu and click Stimulus Hierarchy to make it visible.

Figure 4-2. Simulating Pre-Synthesis Design
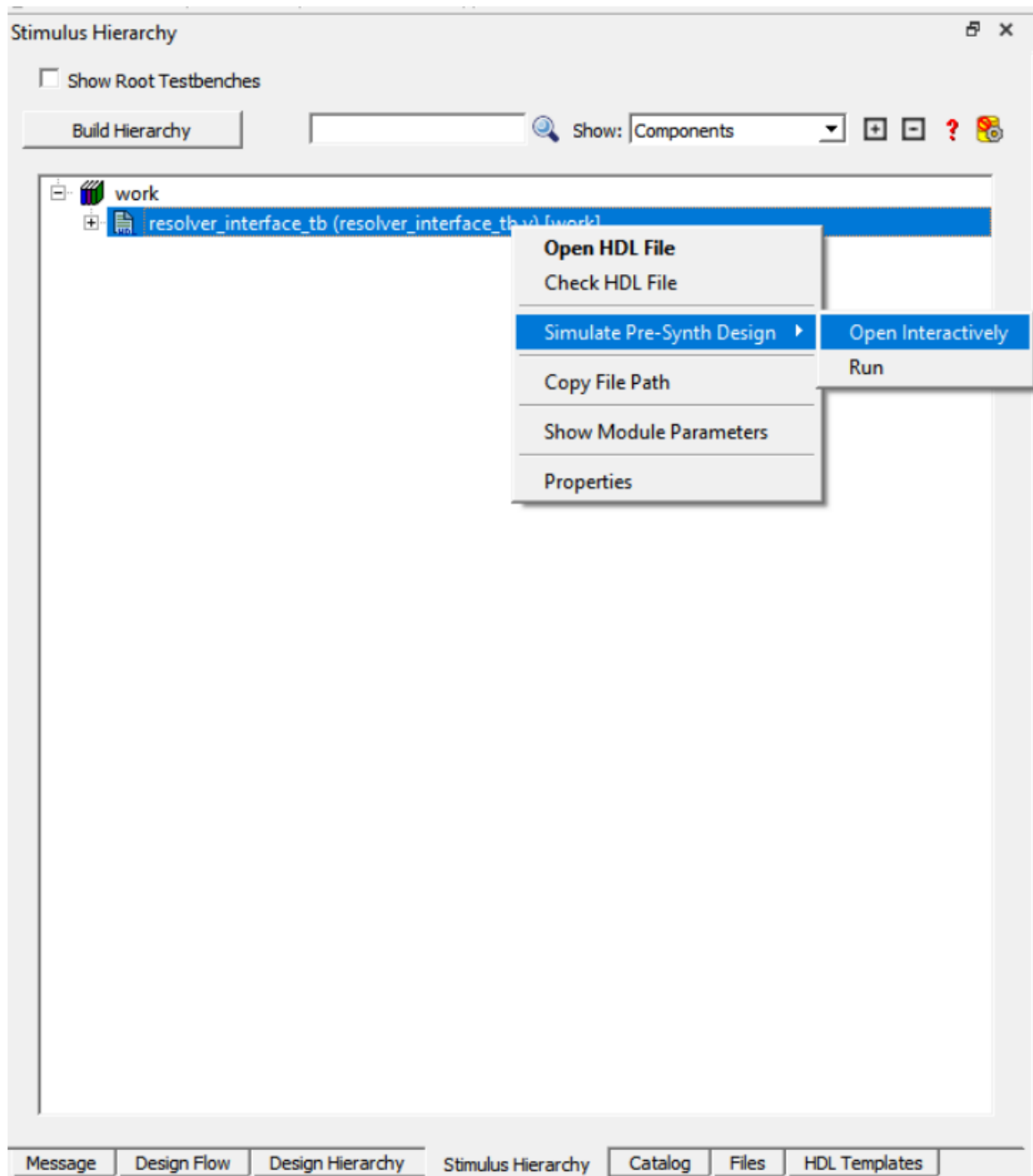
ModelSim opens with the testbench file, as shown in the following figure.

Figure 4-3. ModelSim Simulation Window
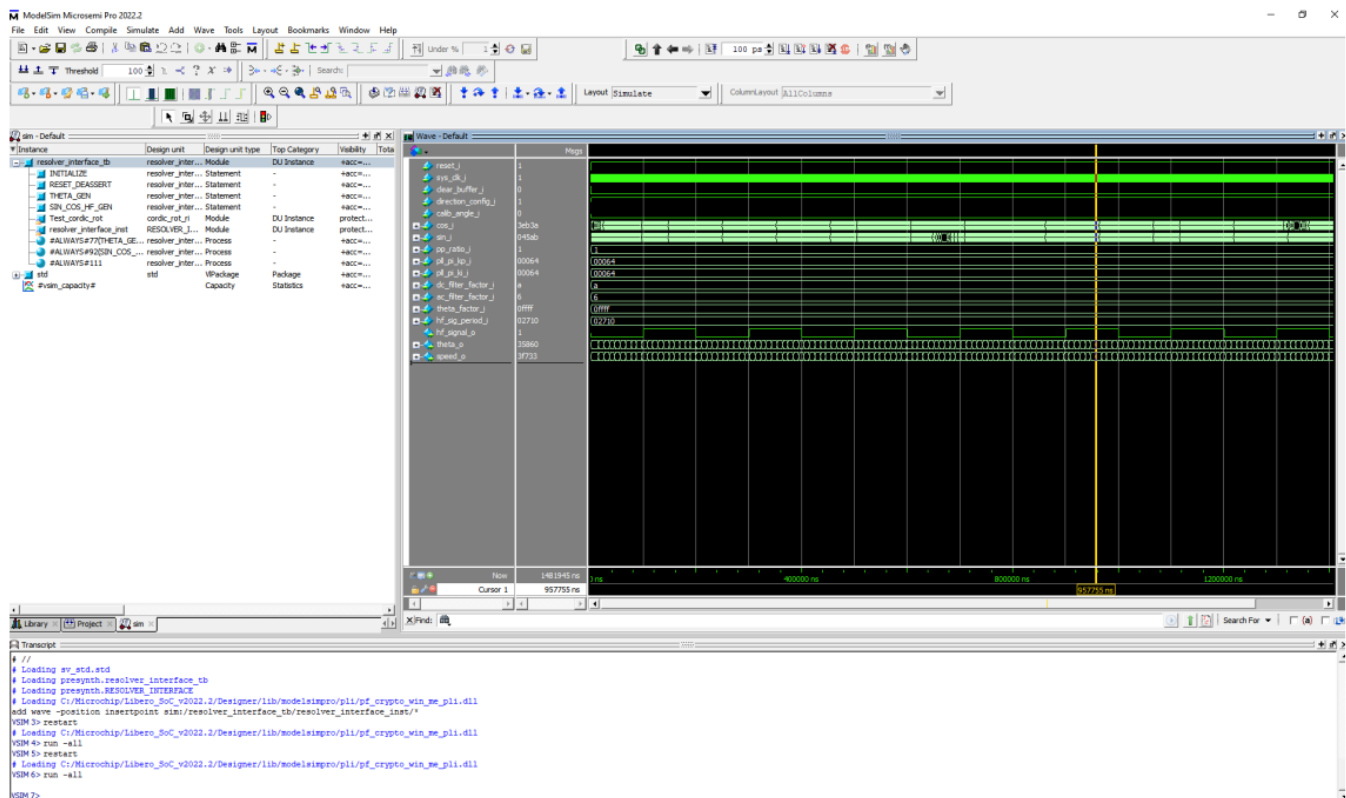
Important: **If** the simulation is interrupted due to the runtime limit specified in the .do file, use the run -all command to complete the simulation.

Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	03/2023	The following list of changes is made in revision A of the document: • Migrated the document to the Microchip template. • Updated the document number to DS50003511 from 50200735. • Added **3. Timing Diagrams**. • Added **4. Testbench**.
4.0	—	The following is a summary of the changes made in revision 4.0 of this document • **Figure 1-1** is updated to add the input port: direction_config_i. • **Table 2-2** is updated to add new signal name: direction_config_i and its description. Also , updated description for the signal name: pp_ratio_i.
3.0	—	The following is a summary of the changes made in revision 3.0 of this document • **Figure 1-1** is updated to add the input ports, clear_buffer_i and pp_ratio_i. • Added new signal names, clear_buffer_i, pp_ratio_i and their descriptions. • The configuration parameter g_PP_RATIO was deleted. • The count value of the resource, "Sequential elements" is changed from 960 to 980. • The equation to calculate theta_factor constant is edited in Hardware Implementation.
2.0	01/2017	The following is a summary of the changes made in revision 2.0 of this document. • Key features were added. • Supported family information was added. • Information on scaling the calculated speed using the theta factor was added. • The description for the calib_angle_i input signal was updated. • The PP_RATIO configuration parameter was added.
1.0	11/2016	Revision 1.0 was the first publication of this document.

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V43 Resolver Interface, V43, Resolver Interface, Interface

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