MICROCHIP v4.2 Speed ID IQ PI Controller User Guide

Contents

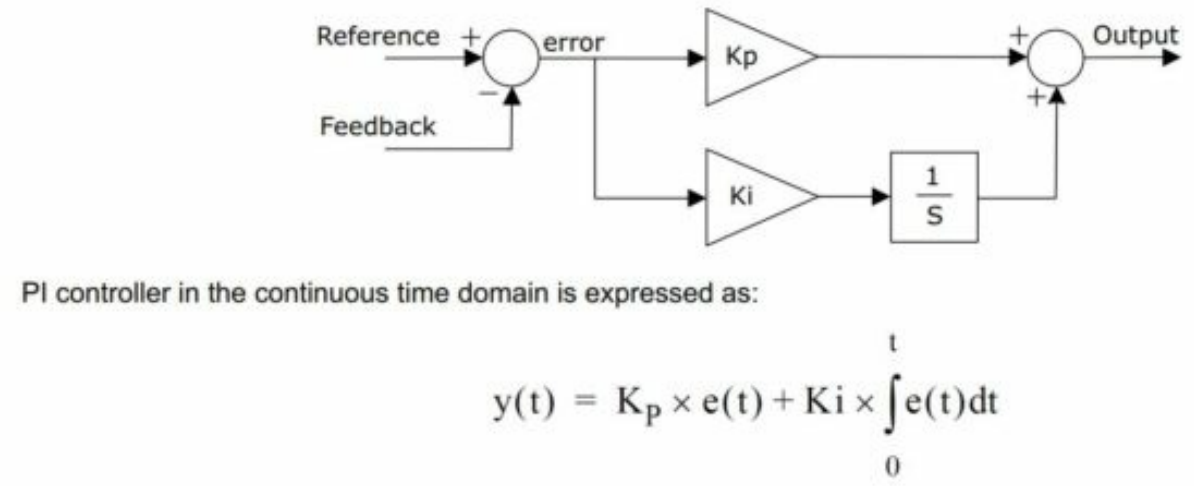
Introduction

(Ask a Question)

The PI controller is a widely used closed-loop controller for controlling a first-order system. The basic functionality of a PI controller is to make the feedback measurement to track the reference input. PI controller performs this action controls its output until the error between the reference and feedback signals becomes zero.

There are two components that contribute to the output: the proportional term and the integral term, as shown in the following figure. The proportional term depends only on the instantaneous value of the error signal, whereas the integral term depends on the present and previous values of an error.

Figure 1. PI Controller in Continuous Domain

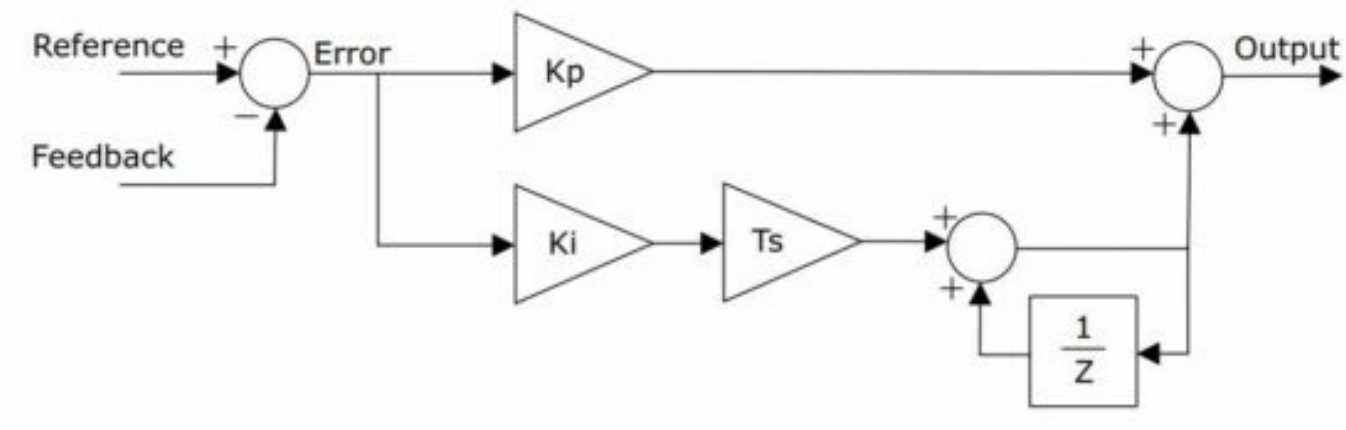


PI controller in the continuous time domain is expressed as:

$$y(t) = K_p \times e(t) + Ki \times \int_0^t e(t)dt$$

Where,
y (t) = PI controller output
e (t) = reference (t) – feedback (t) is the error between reference and feedback
To implement the PI controller in the digital domain, it has to be discretized. The discretized form of the PI controller based on zero order hold method is shown in the following figure.

Figure 2. PI Controller based on Zero Order Hold Method



$$P(n) = K_p \times e(n)$$

$$I(n) = K_i \times T_s \times e(n) + I(n-1)$$

$$Y(n) = P(n) \times I(n)$$

Summary

Core Version	This document applies to Speed ID IQ PI Controller v4.2.
Supported Device Families	• PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v11.8 or later releases.
Licensing	The complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. The Speed ID IQ PI Controller is licensed with the encrypted RTL that must be purchased separately. For more information, see Speed ID IQ PI Controller.

Features (Ask a Question)
The Speed ID IQ PI Controller has the following key features:

- Computes d-axis current, q-axis current, and motor speed
- PI controller algorithm runs for one parameter at a time
- Automatic anti-windup and initialization functions are included

Implementation of IP Core in Libero Design Suite (Ask a Question)
IP core must be installed to the IP Catalog of the Libero SoC software. This is done automatically through the IP Catalog update function in the Libero SoC software, or the IP core can be manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, the core can be configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero project list.

Device Utilization and Performance

(Ask a Question)

The following table lists the device utilization used for Speed ID IQ PI Controller.
Table 1. Speed ID IQ PI Controller Utilization

Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T	627	411	120	0	0	1	0

.....continued

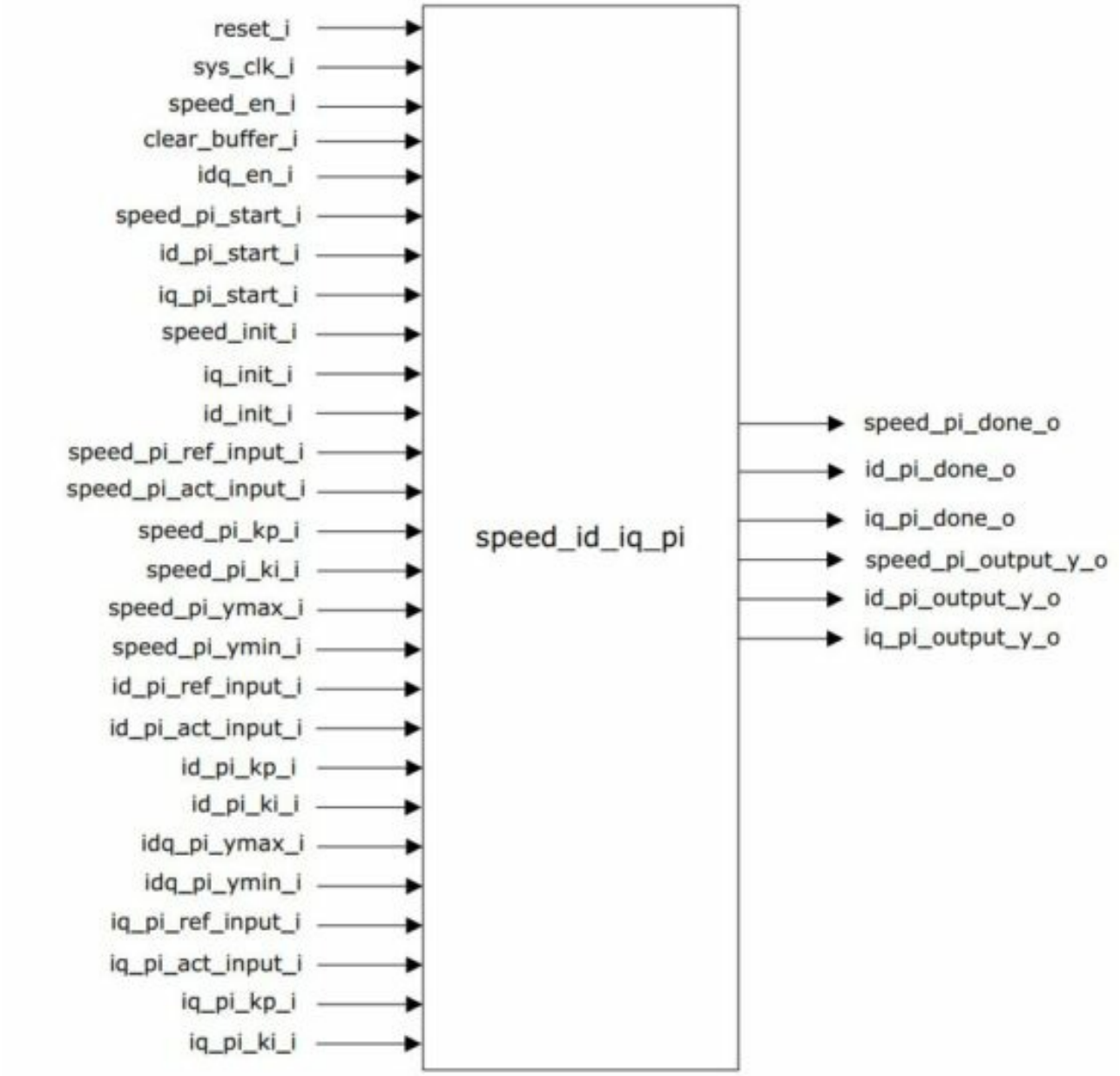
Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire	MPF300T	627	411	120	0	0	1	0
SmartFusion® 2	M2S150	631	411	120	0	0	1	0

Important:

1. The data in the preceding table is captured using typical synthesis and layout settings. The CDR reference clock source is set to Dedicated with other configurator values unchanged.
2. Clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers.

1. Functional Description (Ask a Question)

This section describes the implementation details of the Speed ID IQ PI Controller.
The following figure shows the system-level block diagram of the Speed ID IQ PI Controller.
Figure 1-1. System-Level Block Diagram of Speed ID IQ PI Controller



Note: The Speed ID IQ PI controller executes a PI controller algorithm for three quantities—d-axis current, q-axis current, and motor speed. The block is designed to minimize hardware resource utilization. The block allows the PI controller algorithm to be run for one parameter at a time.

1.1 Anti-Windup and Initialization (Ask a Question)

The PI controller has minimum and maximum limits of output to keep the output within practical values. If a non-zero error signal persists for a long time, the integral component of the controller keeps increasing and might reach a value limited by its bit width. This phenomenon is called integrator windup and must be avoided to have a proper dynamic response. The PI controller IP has an automatic anti-windup function, which limits the integrator as soon as the PI controller reaches saturation.

In certain applications, such as motor control, it is important to initialize the PI controller to a proper value before enabling it. Initializing the PI controller to a good value avoids jerky operations. The IP block has an enable input to enable or disable the PI controller. If disabled, the output is equal to the unit input, and when this option is enabled,
the output is the PI computed value.

1.2 Time Sharing of PI Controller (Ask a Question)

In the Field Oriented Control (FOC) algorithm, there are three PI controllers for Speed, d-axis current ID, and q-axis current Iq. The input of one PI controller depends on the output of the other PI controller, and so they are executed sequentially. At any instant, there is only one instance of the PI controller in operation. As a result,

instead of using three separate PI controllers, a single PI controller is time shared for Speed, Id, and Iq for optimum usage of resources.

The Speed_Id_Iq_PI module allows sharing of the PI controller through the start and done signals for each of Speed, Id, and Iq. The tuning parameters Kp, Ki, and minimum and maximum limits of each instance of a controller can be configured independently through corresponding inputs.

2. Speed ID IQ PI Controller Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the Speed ID IQ PI Controller GUI configurator and I/O signals.

2.1 Configuration Settings (Ask a Question)

The following table lists the description of the configuration parameters used in the hardware implementation of Speed ID IQ PI Controller. These are generic parameters and can be varied as per the requirement of the application.

Table 2-1. Configuration Parameter

Signal Name	Description
g_NO_MCYCLE_PATH	The number of clock delays required before the multiplication product ready signal is asserted.

2.2 Input and Output Signals (Ask a Question)

The following table lists the input and output ports of Speed ID IQ PI Controller.

Table 2-2. Inputs and Outputs of Speed ID IQ PI Controller

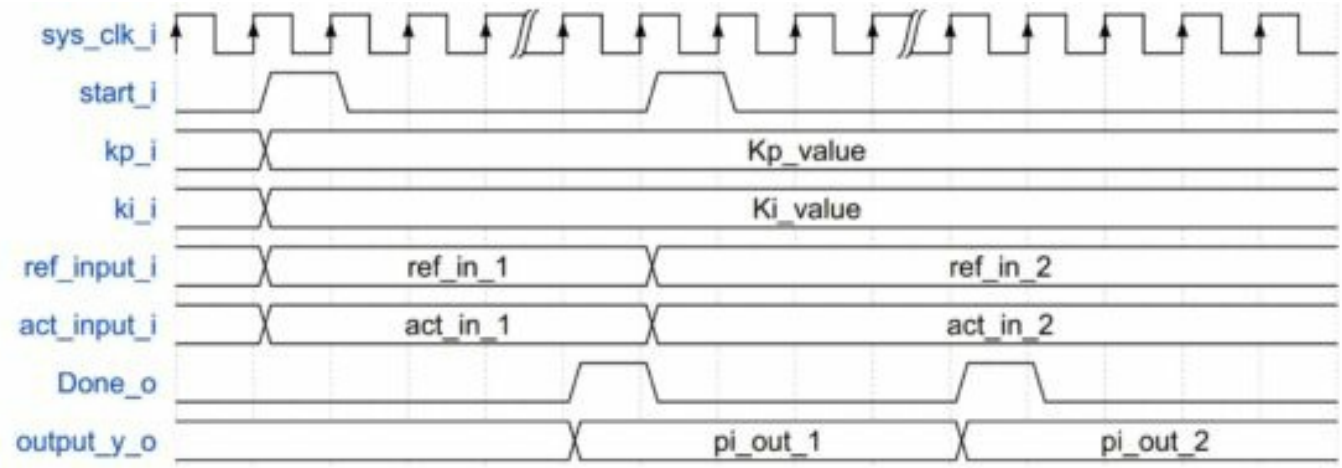
Signal Name	Direction	Description
reset_i	Input	Active low synchronous reset signal.
sys_clk_i	Input	System clock.
speed_en_i	Input	Enable signal for speed PI. When set to 1, normal PI controller operation occurs. When set to 0 (zero), PI controller output is fixed to the value available at the speed_init_i input.
clear_buffer_i	Input	Clears internal buffers when the motor stops.
idq_en_i	Input	Enable signal for Id and Iq PI: Whens et to 1, normal PI controller operation occurs When set to 0 (zero), PI controller output is fixed to the value available at the id_init_i and iq_init_i inputs respectively.
speed_pi_start_i	Input	Start signal for speed PI.
idpi_start_i	Input	Start signal for Id PI.
iqpi_start_i	Input	Starts ignal for Iq PI.
speed_init_i	Input	Initialization value for speed PI.
iq_init_i	Input	Initialization value for iq PI.
id_init_i	Input	Initialization value for id PI.
speed_pi_ref_input_i	Input	Speed PI reference input.
speed_pi_act_input_i	Input	Speed PI feedback measurement input.
speed_pi_kp_i	Input	Proportional gain (Kp) for Speed PI.
speed_pi_ki_i	Input	Integral gain (Ki) for Speed PI.
speed_pi_ymax_i	Input	Saturation limit (upper threshold) of speed PI controller.

Signal Name	Direction	Description
speed_pi_ymin_i	Input	Saturation limit (lower threshold) of speed PI controller.
id_pi_ref_input_i	Input	Id PI Reference input.
id_pi_act_input_i	Input	Id PI feedback measurement input.
id_pi_kp_i	Input	Proportional gain (Kp) for Id PI.
id_pi_ki_i	Input	Integral gain (Ki) for Id PI.
idq_pi_ymax_i	Input	Saturation limit (upper threshold) of current PI controller.
idq_pi_ymin_i	Input	Saturation limit (lower threshold) of current PI controller.
iq_pi_ref_input_i	Input	Iq PI Reference input.
iq_pi_act_input_i	Input	Iq PI feedback measurement input.
iq_pi_kp_i	Input	Proportional gain (Kp) for Iq PI.
iq_pi_ki_i	Input	Integral gain (Ki) for Iq PI.
idq_pi_ymax_i	Input	Saturation limit (upper threshold) of current PI controller.
idq_pi_ymin_i	Input	Saturation limit (lower threshold) of current PI controller.
speed_pi_done_o	Output	Indicates Speed PI computation is complete. High for one system clock cycle.
id_pi_done_o	Output	Indicates Id PI computation is complete. High for one system clock cycle.
iq_pi_done_o	Output	Indicates Iq PI computation is complete. High for one system clock cycle.
speed_pi_output_y_o	Output	Speed PI computation output.
id_pi_output_y_o	Output	Id PI computation output.
iq_pi_output_y_o	Output	Iq PI computation output.

3. Timing Diagrams (Ask a Question)

This section discusses Speed ID IQ PI Controller timing diagrams.
The following figure shows the timing diagram of Speed ID IQ PI Controller.

Figure 3-1. Speed ID IQ PI Controller Timing Diagram



4. Testbench

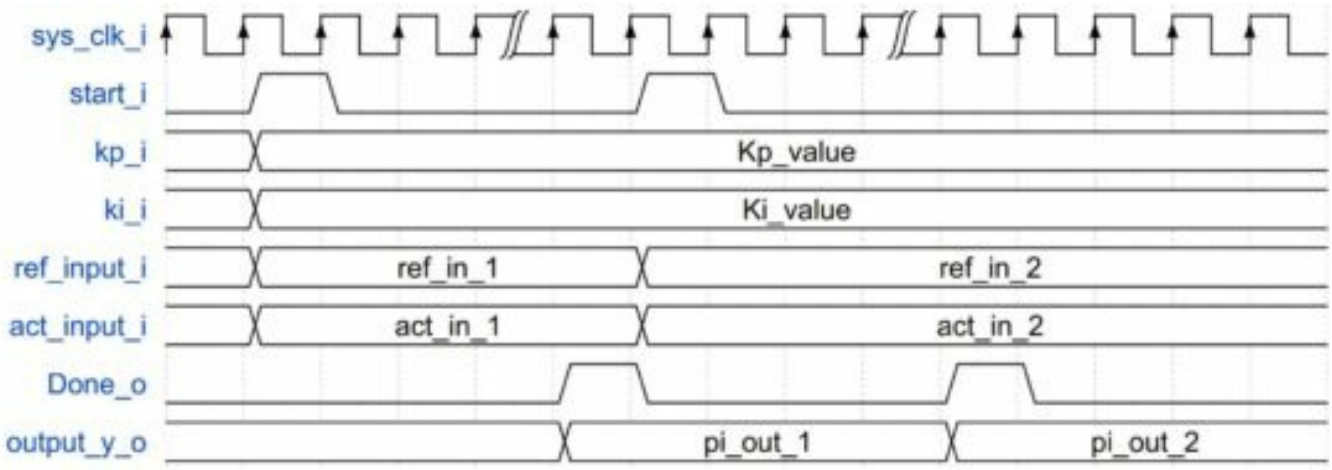
(Ask a Question)
A unified testbench is used to verify and test Speed ID IQ PI Controller called as user testbench. Testbench is provided to check the functionality of the Speed ID IQ PI Controller IP.

4.1 Simulation (Ask a Question)

The following steps describe how to simulate the core using the testbench:
1. Go to Libero SoC Catalog tab, expand Solutions-MotorControl, double click Speed ID IQ PI Controller, and then click OK. The documentation associated with the IP are listed under Documentation.

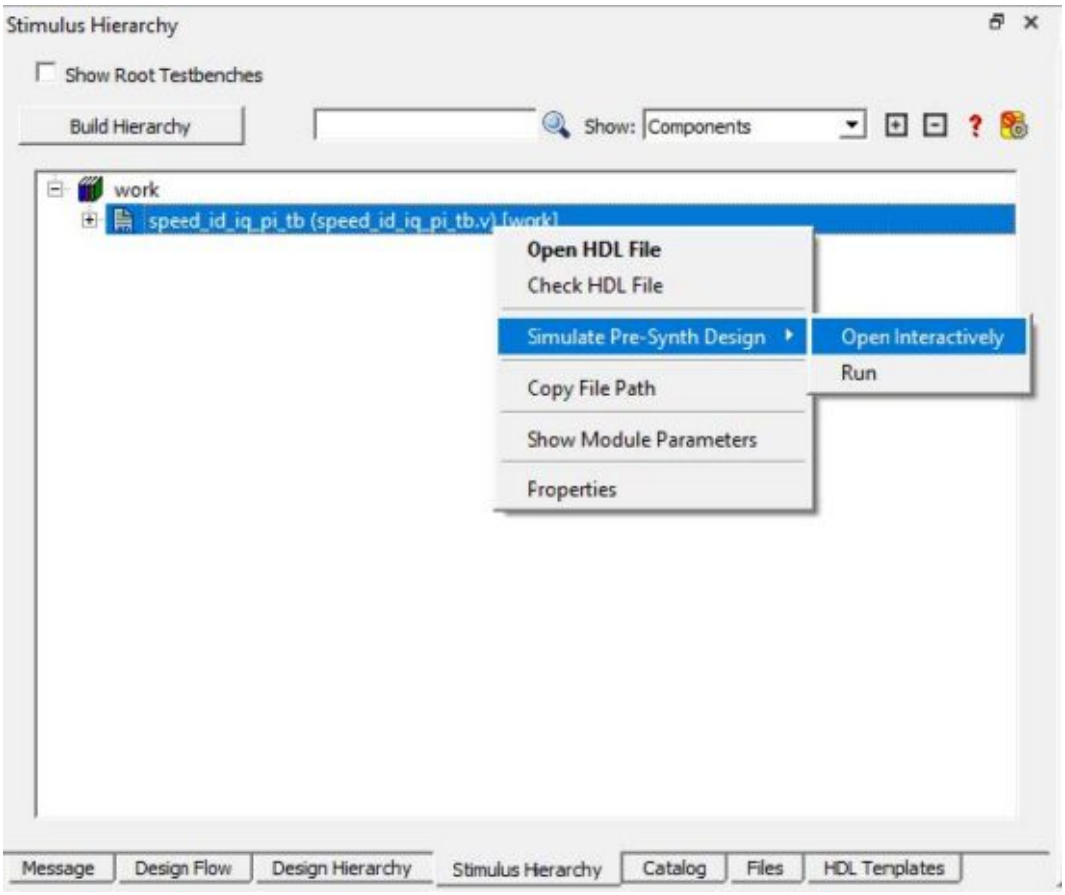
Important: If you do not see the Catalog tab, navigate to View > Windows menu and click Catalog to make it visible.

Figure 4-1. Speed ID IQ PI Controller IP Core in Libero SoC Catalog



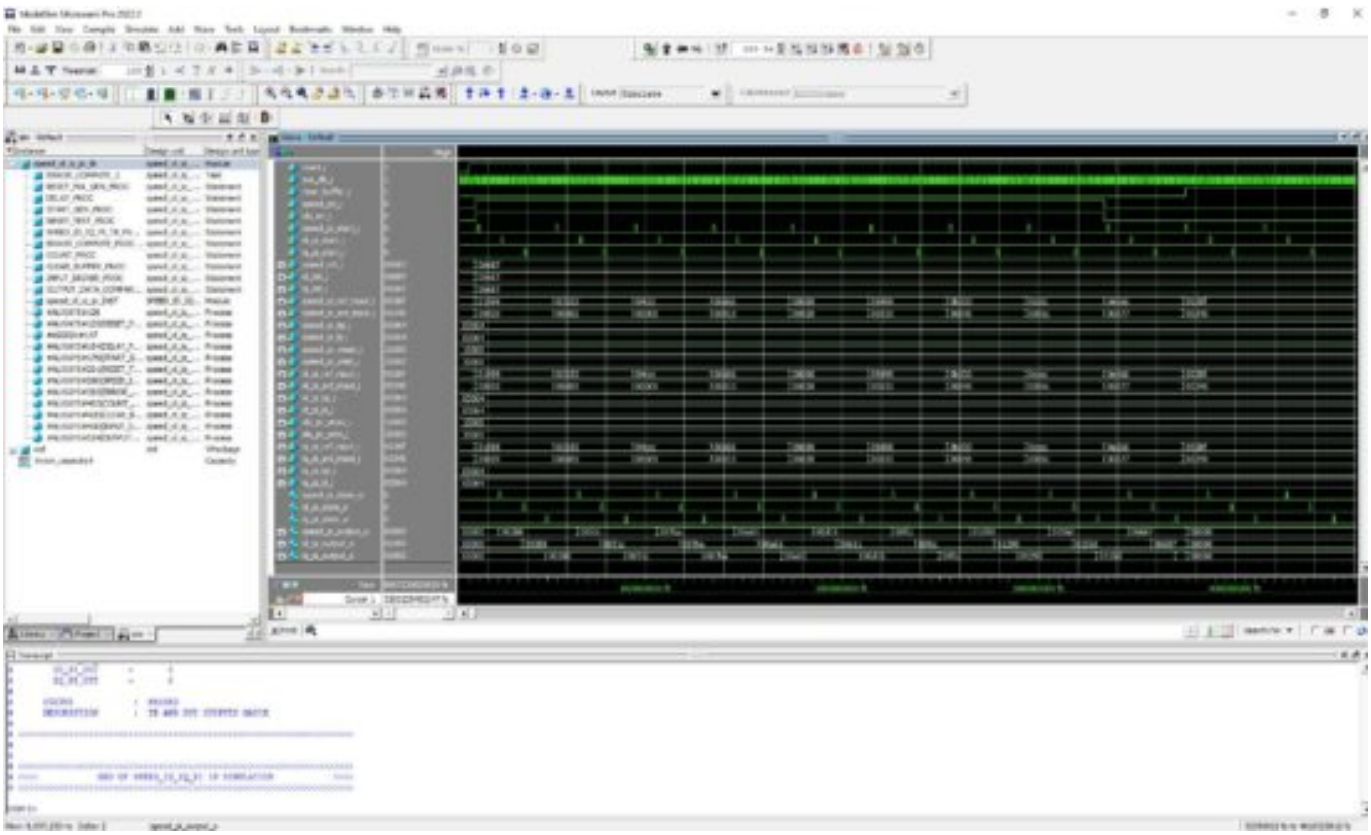
2. On the Stimulus Hierarchy tab, select the testbench (speed_id_iq_pi_controller_tb.v), right click and then click Simulate Pre-Synth Design > Open Interactively.
Important: If you do not see the Stimulus Hierarchy tab, navigate to View > Windows menu and click Stimulus Hierarchy to make it visible.

Figure 4-2. Simulating Pre-Synthesis Design



ModelSim opens with the testbench file, as shown in the following figure.

Figure 4-3. ModelSim Simulation Window



Important: If simulation is interrupted due to the runtime limit specified in the .do file, use the run -all command to complete the simulation.

5. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	03/2023	The following is the list of changes in revision A of the document: • Migrated the document to the Microchip template. • Updated the document number to DS50003507A from 50200612. • Added 3. Timing Diagrams. • Added 4. Testbench.
3.0	—	The following is the list of changes in revision 3.0 of the document: • Added the IP version to the document title. • Removed g_STD_IO_WIDTH configuration parameter from sections Configuration Parameter
2.0	—	Updated Configuration Parameters section.
1.0	—	Revision 1.0 was the first publication of this document.

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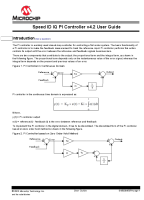	MICROCHIP v4.2 Speed ID IQ PI Controller [pdf] User Guide v4.2 Speed ID IQ PI Controller, v4.2, Speed ID IQ PI Controller, IQ PI Controller, PI Controller, Controller

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