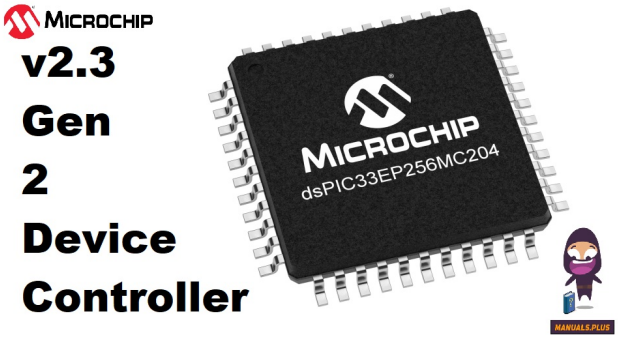
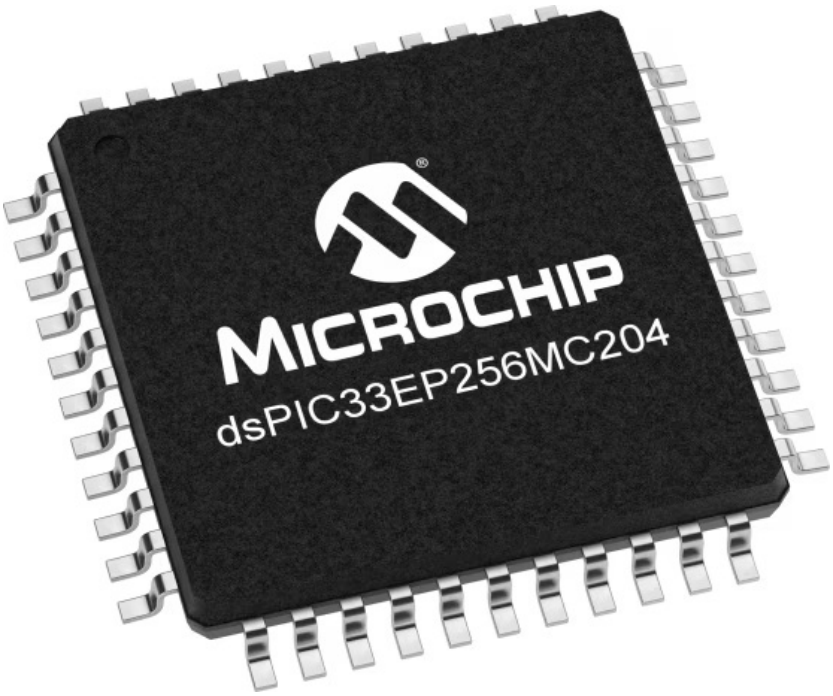


MICROCHIP v2.3 Gen 2 Device Controller User Guide

Contents

MICROCHIP v2.3 Gen 2 Device Controller



Introduction

[Ask a Question]

This CoreRxIODBitAlign generic training IP is used in the IO gearing block in the Rx path for Bit Alignment independent of the data or protocol being used. The CoreRxIODBitAlign allows you to adjust the delay in the data path relative to the clock path.

CoreRxIODBitAlign Summary

Core Version	This document applies to CoreRxIODBitAlign v2.3
Supported Device Families	CoreRxIODBitAlign supports the following families: • PolarFire® SoC • PolarFire **Note:** For additional information, visit the **product page**
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases
Supported Interfaces	—
Licensing	CoreRxIODBitAlign does not require a license
Installation Instructions	CoreRxIODBitAlign must be installed to the IP Catalog of Libero SoC software automatically, through the IP Catalog update function in Libero SoC software, or it is manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, it is configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.
Device Utilization and Performance	A summary of utilization and performance information for CoreRxIODBitAlign is listed in 8. Device Utilization and Performance

CoreRxIODBitAlign Change Log Information

This section provides a comprehensive overview of the newly incorporated features, beginning with the most recent release. For more information about the problems resolved, see the 7. Resolved Issues section.

CoreRxIODBitAlign v2.3	**What's New**	• Updated for MIPI-based training mechanism
CoreRxIODBitAlign v2.2	**What's New**	• Added Left and Right EYE Tap delays information in the top module

Features

Ask a Question

CoreRxIODBitAlign has the following features:

- Supports Bit Alignment with different Eye Widths 1–7
- Supports different Fabric Double Data Rate (DDR) Modes 2/4/3p5/5
- Supports Skip and Restart/Hold mechanism
- Supports Mobile Industry Processor Interface (MIPI) training through LP signaling Start of Frame
- Supports 256 Tap Delays for Bit Alignment

Functional Description

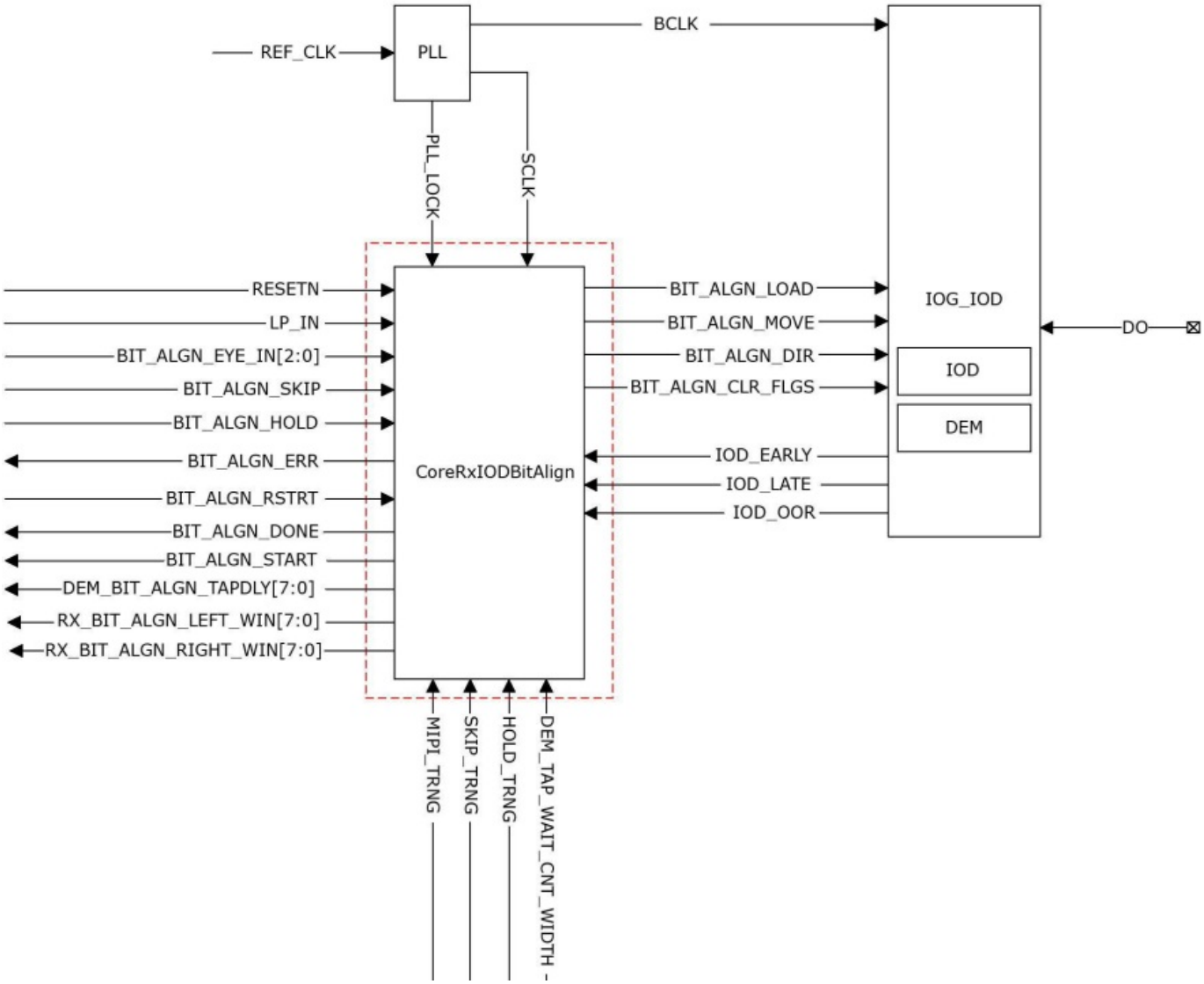
Ask a Question

CoreRxIODBitAlign with Rx IOD Interface

Ask a Question

The following figure shows a high-level block diagram of the CoreRxIODBitAlign.

Figure 2-1. CoreRxIODBitAlign Block Diagram



- The description refers to the CoreRxIODBitAlign supporting PolarFire® and PolarFire SoC devices.
- CoreRxIODBitAlign performs training and is also responsible for interfacing IO Digital (IOD) devices and IO Gearing (IOG) to support as a dynamic source with adjusting delays to capture the data correctly.
- The complete training mechanism flow is explained in the 5. Timing Diagrams section.
- CoreRxIODBitAlign dynamically supports adding or removing delay from the data path relative to the clock path. Here RX_DDRX_DYN Interface provides controls to the CoreRxIODBitAlign to perform the clock-to-data margin training by adding tap delays in an upward direction. CoreRxIODBitAlign, in turn for later review (of each tap delay increment), stores the feedback status flags from RX_DDRX_DYN Interface.
- The CoreRxIODBitAlign continues the training for every tap increment until the RX_DDRX_DYN Interface reaches the out-of-range condition.
- Finally, the CoreRxIODBitAlign sweeps the complete feedback status flags. This step optimizes and calculates the bit alignment of the data to be 90 degrees centered from the clock edges.

- The final calculated tap delays are loaded in the RX_DDRX_DYN Interface to complete the bit alignment training.
- The features supported by this CoreRxIODBitAlign are listed in detail as follows.

Dynamic Re-training Mechanism

Ask a Question

- CoreRxIODBitAlign continuously monitors the Feedback Status flags (IOD_EARLY/IOD_LATE) and checks if the flags are toggling.
- The IP firstly adjusts the previously calculated taps by +/- 4 taps in an upward or downward direction. Even then, if the flags toggle, the IP re-triggers the training again.

Figure 2-2. Re-training Mechanism Timing Diagram

Hold Mechanism (Ask a Question)

- This feature is used when the training needs to be on Hold state. The BIT_ALGN_HOLD is active-high level based input and must be asserted to hold and de-asserted to continue the training.
- The HOLD_TRNG parameter must be set to 1 in the configurator to enable this feature. This parameter is set to 0 by default.

Restart Mechanism (Ask a Question)

- This feature is used to restart the training. To restart the training, the BIT_ALGN_RSTRT input must be asserted for one clock pulse Serial Clock (SCLK).
- This initiates the soft reset of the IP, which resets BIT_ALGN_DONE to 0 and BIT_ALGN_START to 1.

Skip Mechanism (Ask a Question)

- This feature is used when the training is not required, and the complete training can be bypassed. The BIT_ALGN_SKIP is active-high level based input and must be asserted to skip the complete training.
- The SKIP_TRNG parameter must be set to 1 in the configurator to enable this feature. This parameter is set to 0 by default.

MIPI-based Training Mechanism (Ask a Question)

- The MIPI_TRNG parameter must be set to 1 in the configurator to enable this feature. If set, then the LP_IN input port is added to the CoreRxIODBitAlign.
- The IP detects the falling edge of the LP_IN input port, which indicates the valid start of the frame to start the training.

CoreRxIODBitAlign Parameters and Interface Signals

Ask a Question

Configuration GUI Parameters (Ask a Question)

There are no configuration parameters for this core release.

Ports (Ask a Question)

The following table lists the input and output signals used in the design of CoreRxIODBitAlign.

Table 3-1. Input and Output Signals

Signal	Direction	Port width (bits)	Description
Clocks and Reset			
SILK	Input	1	Fabric clock
PLL_LOCK	Input	1	PLL Lock
RESET	Input	1	Active-Low asynchronous reset
Data bus and Control			
IOD_EARLY	Input	1	Data eye monitor early flag
IOD_LATE	Input	1	Data eye monitor late flag
IOD_ OOR	Input	1	Data eye monitor out-of-range flag for delay line
BIT_ALGN_EYE_IN	Input	3	The user sets the data eye monitor width
BIT_ALGN_RSTRT	Input	1	Bit Align Training restart (Pulse-based assertion) 1— Restart Training 0— No Restart Training
BIT_ALGN_CLR_FLGS	Output	1	Clear Early or Late flags
BIT_ALGN_LOAD	Output	1	Load default
BIT_ALGN_DIR	Output	1	Delay line up or down direction 1— Up (increment 1 tap) 0— Down (decrement 1 tap)
BIT_ALGN_MOVE	Output	1	Increment the delay on the move pulse
BIT_ALIGN_SKIP	Input	1	Bit Align training skip (Level based assertion) 1— Skip the training and valid only when the SKIP_TRNG parameter is set to 1 0— Training must proceed as normal
BIT_ALIGN_HOLD	Input	1	Bit Align training hold (Level based assertion) 1— Hold the training and valid only when the HOLD_TRNG parameter is set to 1 0— Training must proceed as normal
BIT_ALIGN_ERR	Output	1	Bit Align training error (Level-based assertion) 1— Error 0— No Error
BIT_ALGN_START	Output	1	Bit Align training start (Level-based assertion) 1— Started 0— Not started
BIT_ALGN_DONE	Output	1	Bit Align training done (Level based assertion) 1— Completed 0— Not completed

Signal	Direction	Port width (bits)	Description
LP_IN	Input	1	MIPI-based frame training (Level based assertion) 1— Active-Low signal must assert low to indicate the start of frame and must deassert only at the end of the frame. 0— Training must proceed as normal and this signal must be tied low internally.
DEM_BIT_ALGN_TAPDLY	Output	8	Calculated TAP delays and valid once BIT_ALGN_DONE is set high by the IP.
RX_BIT_ALIGN_LEFT_WIN	Output	8	Left Data Eye monitor value **Note:** The values are valid only when the output BIT_ALGN_DONE is set to 1 and the output BIT_ALGN_START is set to 0. If the parameter SKIP_TRNG is set then it returns 0.
RX_BIT_ALIGN_RGHT_WIN	Output	8	Right Data Eye monitor value **Note:** The values are valid only when the output BIT_ALGN_DONE is set to 1 and the output BIT_ALGN_START is set to 0. If the parameter SKIP_TRNG is set then it returns 0.

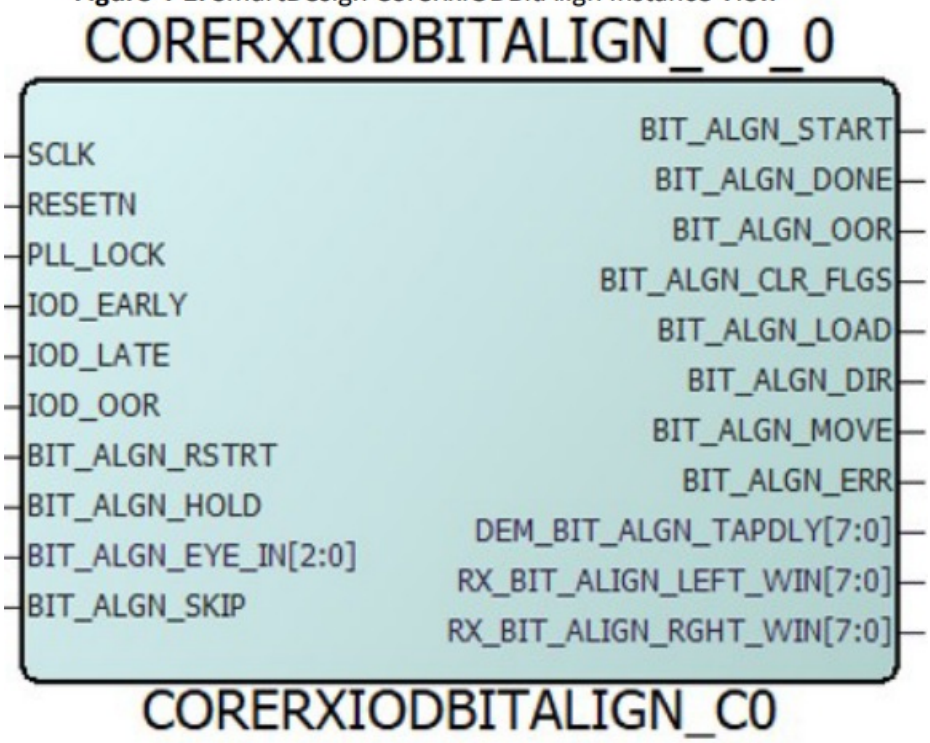
Implementing CoreRxIODBitAlign in Libero Design Suite

Ask a Question

SmartDesign (Ask a Question)

- CoreRxIODBitAlign is pre-installed in the SmartDesign IP deployment design environment. The following figure shows an example of instantiated CoreRxIODBitAlign.
- The core is configured using the configuration window in the SmartDesign, as shown in Figure 4-2.
- For more information on using the SmartDesign to instantiate and generate cores, see SmartDesign User Guide.

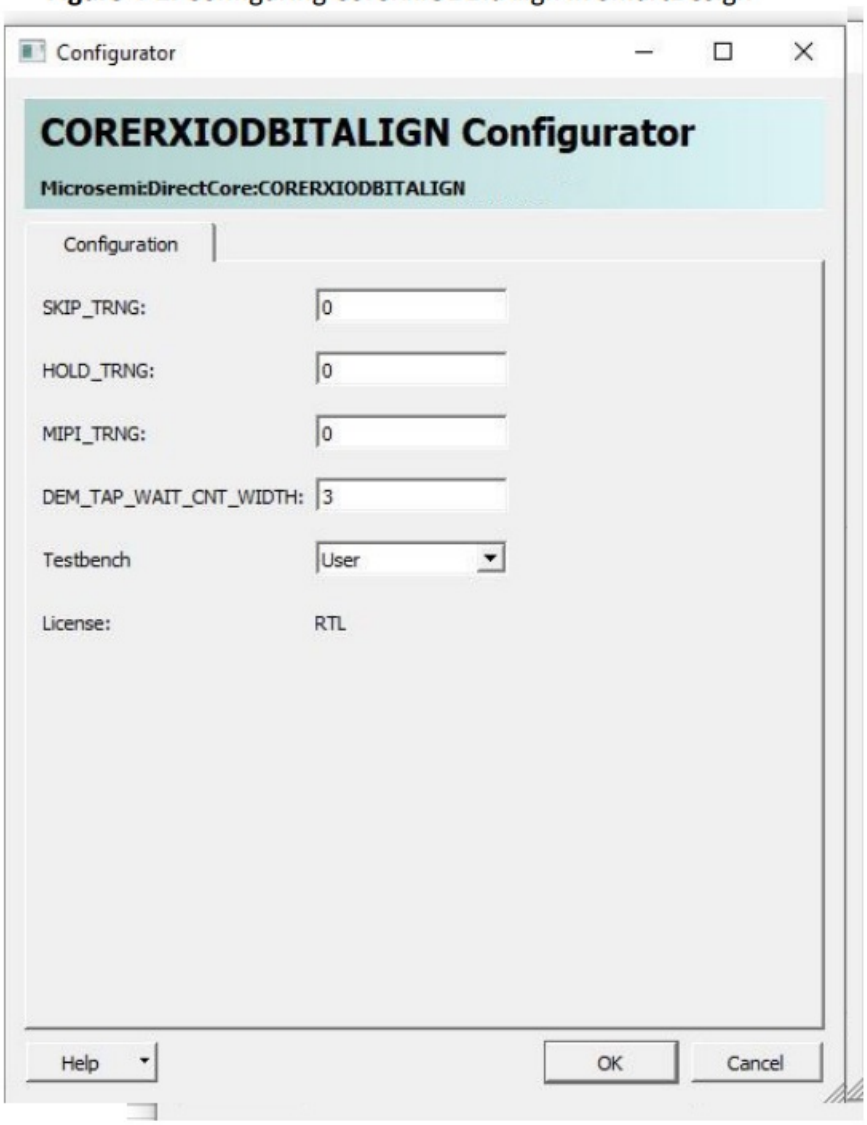
Figure 4-1. SmartDesign CoreRxIODBitAlign Instance View



Configuring CoreRxIODBitAlign in SmartDesign (Ask a Question)

- The core is configured using the configuration GUI within SmartDesign as shown in the following figure.

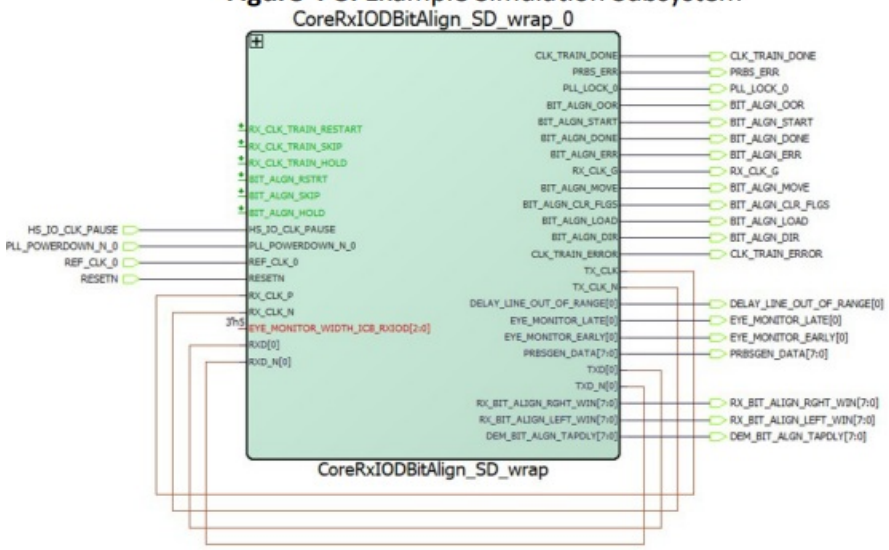
Figure 4-2. Configuring CoreRxIODBitAlign in SmartDesign



Simulation Flows (Ask a Question)

- The user testbench for CoreRxIODBitAlign is included in all the releases.
- To run simulations, perform the following step: select the User Testbench flow in the SmartDesign, and then click Save and Generate on the Generate pane.
- The User testbench is selected through the core testbench Configuration GUI. When SmartDesign generates the Libero® SoC project, it installs the user testbench files.
- To run the user testbench, set the design root to the CoreRxIODBitAlign instantiation in the Libero SoC design hierarchy pane, and then click Simulation in the Libero SoC Design Flow window.
- This invokes ModelSim® and automatically runs the simulation.
- The following figure shows an example of a simulation subsystem. It uses the IOG_IOD component DDRX4 and DDTX4 in loopback mode with the CoreRxIODBitAlign for simulation.
- Here, the PRBS data generated is transmitted by DDTX4 serially to DDRX4 and finally, the PRBS checker is used to check the data integrity after the training is completed.

Figure 4-3. Example Simulation Subsystem



Synthesis in Libero SoC (Ask a Question)

- To run synthesis with the configuration selected in the configuration GUI, set the design root appropriately. Under Implement Design, in the Design Flow tab, right-click on Synthesize and click Run.

Place and Route in Libero SoC (Ask a Question)

- After setting the design root appropriately and run Synthesis. Under Implement Design in the Design Flow tab, right-click on Place and Route, and click Run.

System Integration (Ask a Question)

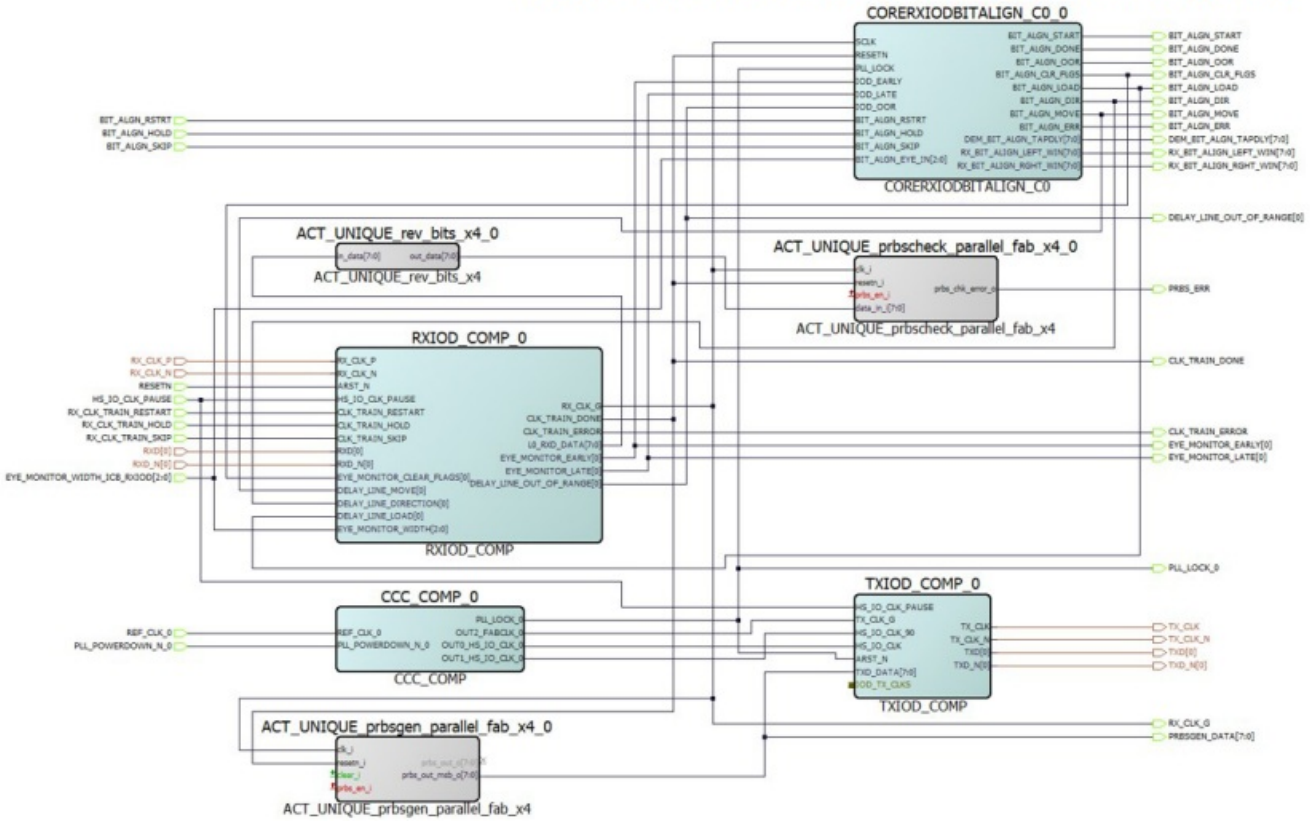
- This section hints to ease the integration of CoreRxIODBitAlign.
- The Rx/Tx IOG used supports numerous input and output modes. These data and clock rates may be slower and in some cases faster, based on final silicon characterization.
- The following table lists the data and clock rate.

Table 4-1. Data and Clock Rate

IOG Mode	Direction	Gear Ratio	Max IO Data Rate Expected	IO Clock Rate	Core Clock Rate	Data Type
DDRX4	Input	8:1	1600 Mbps	800 MHz	200 MHz	DDR

The following figure shows an example of CoreRXIODBitAlign subsystem integration.

Figure 4-4. CoreRxIODBitAlign System Integration



- The preceding subsystem uses IOG_IOD component DDRX4 and DDTX4 in Loopback mode with the CoreRxIODBitAlign for simulation. Here, the PRBS data generated is transmitted by IOG_IOD_DDRTX4_0, serially to IOG_IOD_DDRX4_PF_0.
- The CoreRxIODBitAlign does the training (BIT_ALIGN_START set to 1, BIT_ALIGN_DONE set to 0) with the component IOG_IOD_DDRX4_PF_0, and finally, once training is done (BIT_ALIGN_START set to 0, BIT_ALIGN_DONE set to 1) the PRBS checker is used to check the data integrity.

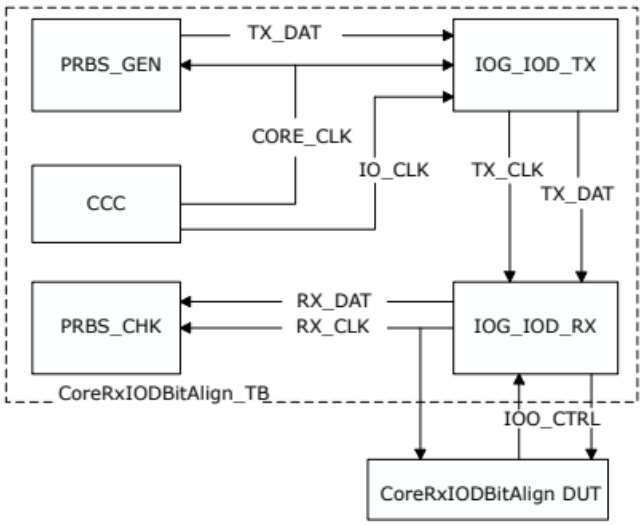
Testbench (Ask a Question)

- A unified testbench is used to verify and test CoreRxIODBitAlign called a user testbench.

User Testbench (Ask a Question)

- The user testbench is included with the releases of CoreRxIODBitAlign which verifies a few features of the CoreRxIODBitAlign. The following figure shows the CoreRxIODBitAlign user testbench.

igure 4-5. CoreRxIODBitAlign User Testbench



EXAMPLE Subsystem for DDRX4 Mode CCC-Clock Conditioning Circuit CORE_CLk/RX_CLK-125MHz IO_CLK/TX_CLK – MHz

- As shown in the preceding figure, the user testbench consists of a Microchip DirectCore CoreRxIODBitAlign DUT, PRBS_GEN, PRBS_CHK, CCC, IOG_IOD_TX, and IOG_IOD_RX to verify in Loopback mode.
- The Clock Conditioning Circuit (CCC) drives the CORE_CLK and IO_CLK when the clock is stable.
- PRBS_GEN drives the parallel data to IOG_IOD_TX, and then IOG_ID_RX receives the serial data in parallel.
- The CoreRxIODBitAlign DUT performs the training with IOD_CTRL signals. Once the training is completed, the PRBS_CHK block is enabled to check the data from the IOG_IOD_RX block for data integrity.
- **Important:** The user testbench supports only the fixed configuration.

Timing Diagrams

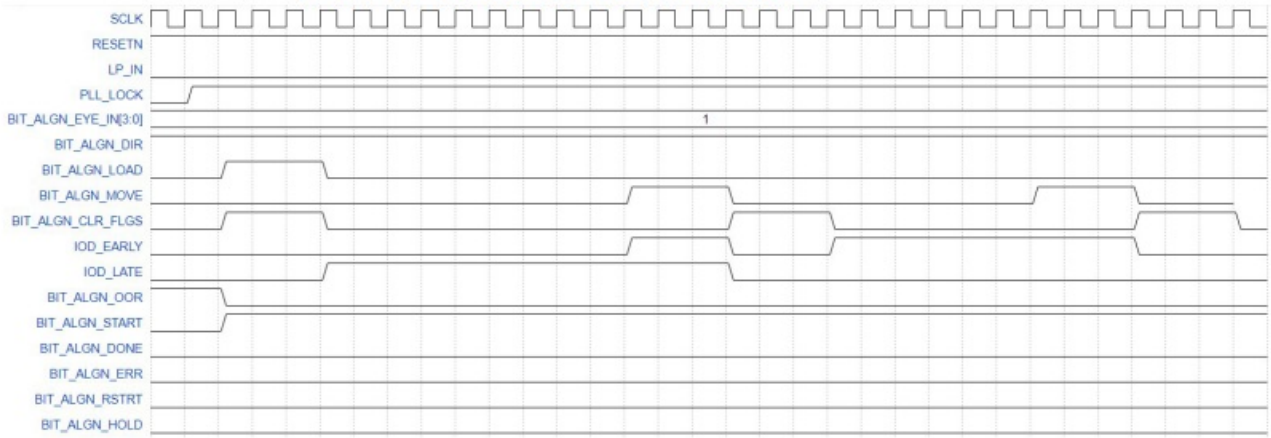
(Ask a Question)

- This section describes the timing diagram of the CoreRxIODBitAlign.

CoreRxIODBitAlign Training Timing Diagram (Ask a Question)

- The following timing diagram is an example of a training sequence with the following parameters.

Figure 5-1. CoreRxIODBitAlign Timing Diagram



- CoreRxIODBitAlign works based on Fabric clock or SCLK, or OUT2_FABCLK_* from CCC or PLL component, and PF_IOD_GENERIC_RX IOD component used works based on OUT*_HS_IO_CLK_* or Bank clock or

BCLK for bit alignment. Here, the PF_IOD_GENERIC_RX IOD component receives the serial data for bit alignment. For example, if the required data rate is 1000 Mbps at DDRx4 Fabric mode, then the OUT2_FABCLK_0 or SCLK must be driven from the PLL or CCC component as 125 MHz and OUT0_HS_IO_CLK_0 or BCLK to PF_IOD_GENERIC_RX must be 500 MHz.

- CoreRxIODBitAlign starts the training once the PLL_LOCK is stable and driven high. Then the start of training by driving BIT_ALGN_START as high and BIT_ALGN_DONE as low and then drives the output BIT_ALGN_LOAD to load the default settings in the PF_IOD_GENERIC_RX component. The BIT_ALGN_CLR_FLGS is used to clear the IOD_EARLY, IOD_LATE, and BIT_ALGN_OOR flags.
- CoreRxIODBitAlign proceeds with BIT_ALGN_MOVE followed by BIT_ALGN_CLR_FLGS for every TAP and records the IOD_EARLY and IOD_LATE flags. Once BIT_ALGN_OOR is set high by the PF_IOD_GENERIC_RX component, CoreRxIODBitAlign sweeps the recorded EARLY and LATE flags and finds the optimal Early and Late flags to calculate the required TAP delays for clock and data bit alignment.
- CoreRxIODBitAlign loads the calculated TAP delays and drives BIT_ALGN_START low and BIT_ALGN_DONE high to indicate the completion of the training.
- CoreRxIODBitAlign continues the Re-training dynamically if it detects noisy IOD_EARLY or IOD_LATE feedback assertion from the PF_IOD_GENERIC_RX component. Here, the BIT_ALGN_DONE is reset and driven low and BIT_ALGN_START is driven high again by CoreRxIODBitAlign to indicate the restart of the training. The time-out counter when reaches the time-out condition, asserts the BIT_ALGN_ERR at the end of the training.
- CoreRxIODBitAlign also provides a restart mechanism for the end user to restart the training whenever required. The BIT_ALGN_RSTRT input is active-high pulse must be driven high, for example, eight clocks.
- Here the BIT_ALGN_DONE is reset and driven low, and BIT_ALGN_START is driven high again by CoreRxIODBitAlign, to indicate the fresh start of the training.
- CoreRxIODBitAlign also provides a holding mechanism to hold the training in the middle. Here the HOLD_TRNG parameter must be set to 1, and then CoreRxIODBitAlign uses the BIT_ALGN_HOLD input and must assert active-high level based until it requires CoreRxIODBitAlign to hold the training and then continues the training once the input BIT_ALGN_HOLD is driven low.

Additional References

(Ask a Question)

- This section provides a list of additional information.
- For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the **Microchip FPGA Intellectual Property Cores**.

Known Issues and Workarounds (Ask a Question)

- There are no known limitations or workarounds in the CoreRxIODBitAlign v2.3.

Discontinued Features and Devices (Ask a Question)

- There are no discontinued features and devices in CoreRxIODBitAlign v2.3.

Resolved Issues

(Ask a Question)

- The following table lists all the resolved issues for the various CoreRxIODbitAlign releases.

Table 7-1. Resolved Issues

Release	Description
2.3	There are no resolved issues in this v2.3 release
2.2	There are no resolved issues in this v2.2 release
1.0	Initial Release

Device Utilization and Performance

(Ask a Question)

The CoreRxIODBitAlign macro is implemented in the families listed in the following table.

Table 8-1. Device Utilization and Performance

Device Details		FPGA Resources			Performance (MHz)
Family	**Device**	**DFF**	**LUTs**	**Logic Elements**	**SILK**
PolarFire®	MPF300TS	788	1004	1432	261
PolarFire SoC	MPF250TS	788	1004	1416	240

- **Important: The** data in the preceding table is achieved using Libero® SoC v2023.2.
- The data in the preceding table are achieved using typical synthesis and layout settings.
- The following top-level configuration GUI parameters have been modified from their default values.
- **The following are the default values:**
  - **SKIP_TRNG** = 1
  - **HOLD_TRNG** = 1
  - **MIPI_TRNG** = 1
  - **DEM_TAP_WAIT_CNT_WIDTH** = 3
- **Following are the clock constraints used to achieve the performance numbers:**
  - **SCLK** = 200 MHz
  - **Speed Grade** = –1
- Throughput is computed as follows: (Bit width/Number of cycles) × Clock Rate (Performance).

Revision History

(Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description
B	02/2024	The following is the list of changes in revision B of the document: • Updated for CoreRxIODBitAlign v2.3 • Added Change log information in the Introduction section • Updated 8. Device Utilization and Performance section • Added 7. Resolved Issues section
A	03/2022	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template • The document number was changed from 50200861 to DS50003255
3	—	The following is the list of changes in revision 3 of the document: • Updated for CoreRxIODBitAlign v2.2. • Updated the user guide for left and right data eye signals at the top. For additional information, refer to Figure 2-1 and 3.2. Ports.
2	—	The following is the list of changes in revision 2 of the document: • Updated for CoreRxIODBitAlign v2.1. • Updated: 2. Functional Description and 5. Timing Diagrams.
1	—	Revision 1.0 was the first publication of this document. Created for CoreRxIODBitAlign v2.0.

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References

- User Manual