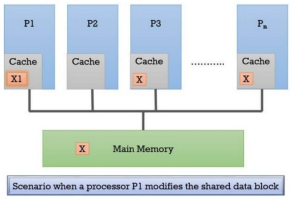

MICROCHIP TB3308 Handling Cache Coherency Issues at Runtime Using Cache Maintenance User Guide

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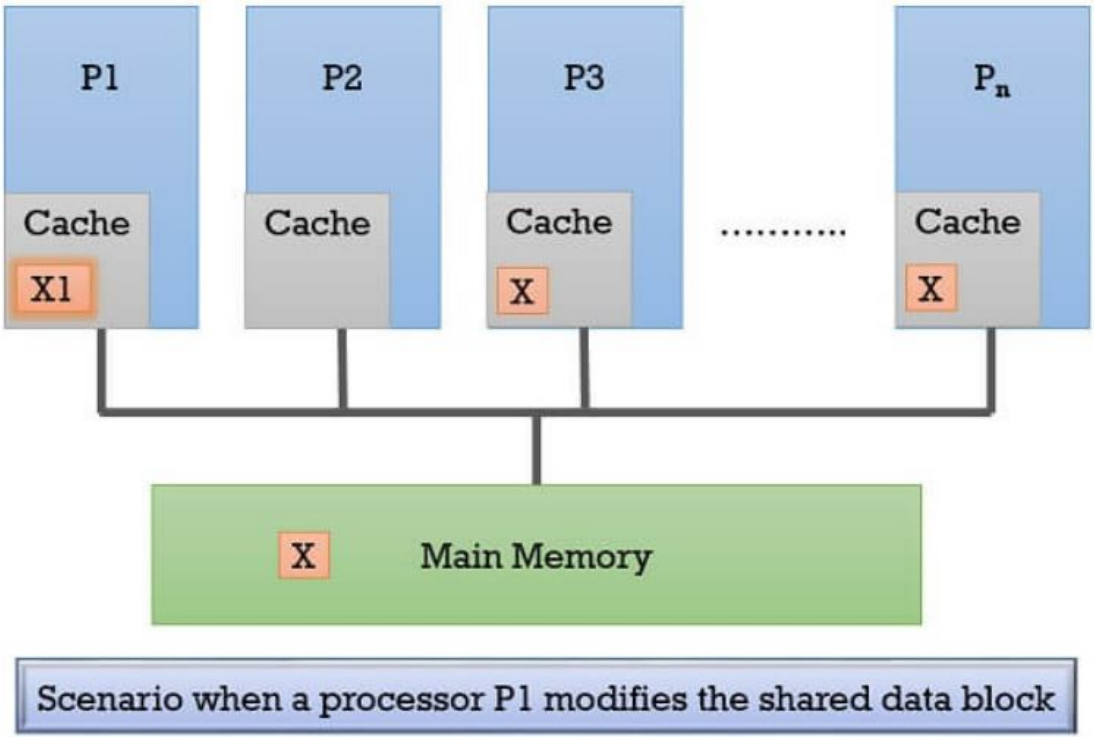


Introduction

The cache coherency issue is inevitable on applications running on microcontrollers (MCUs) that have cacheable memory regions, which use a Direct Memory Access (DMA) for data transfer operations. This is due to the CPU performing a read/write operation from the cache while the DMA transfers data between the peripheral and physical memory.

One of the methods to handle cache coherency requires the application to manage the cache at run-time using the cache maintenance operations. MPLAB® Harmony v3 provides cache maintenance Application Program Interfaces (APIs) for PIC32MZ devices.

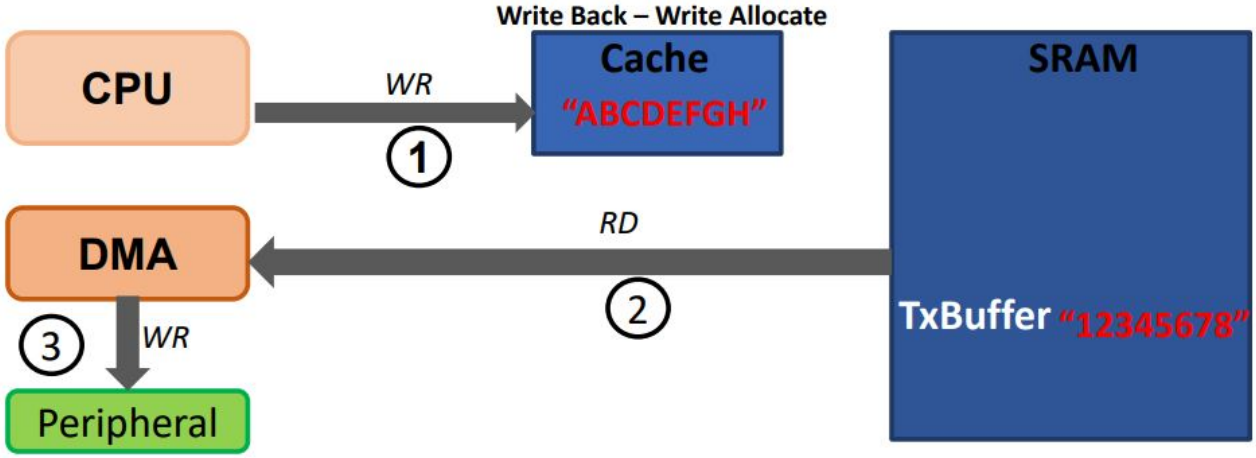
This document explains how an application can manage cache coherency issues at run time by using cache management APIs under MPLAB Harmony v3.

Note: The concepts discussed in this document are common for all PIC32MZ MCUs. The PIC32MZ EF is used as an example to discuss the concepts.

Description

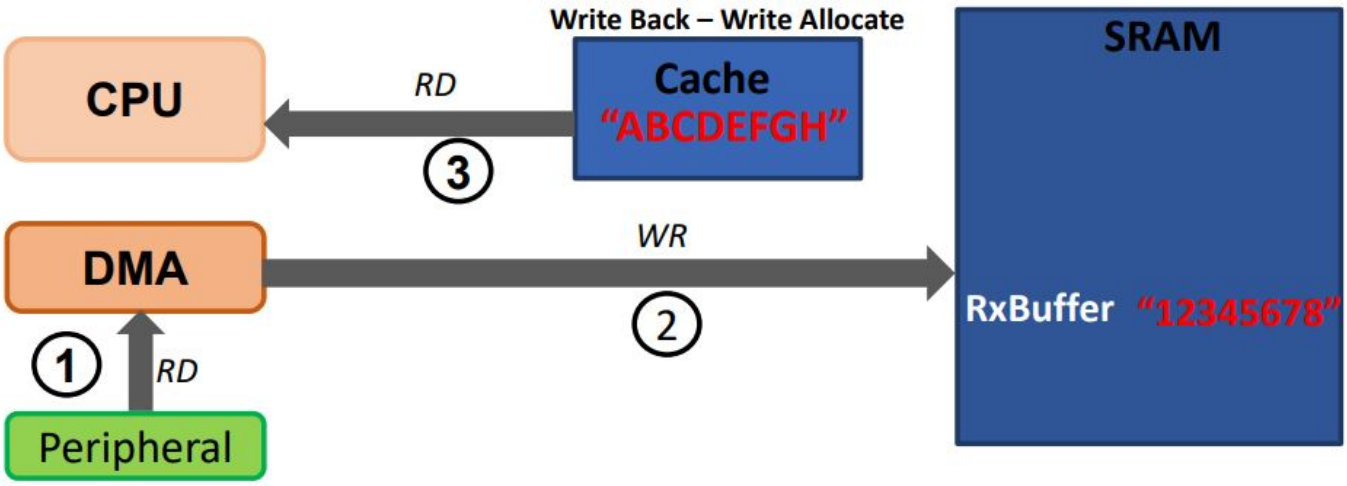
The following figure illustrates the cache coherency issue as observed when the DMA reads from the SRAM on the PIC32MZ EF MCU.

Figure 1-1. Memory-to-Peripheral Transfer (DMA Reads from SRAM)



The application submits a request to transfer the data buffer TxBuffer value ‘ABCDEFGH’ to the peripheral. The CPU populates the DMA write buffer (TxBuffer) with the data to be written ‘ABCDEFGH’ to the peripheral. However, due to the set cache policy Write Back and Write Allocate, the DMA write buffer (TxBuffer) may not be immediately written to the main memory, and the written data may remain in the data cache. The DMA write buffer (TxBuffer) in the main memory still contains the old value of ‘12345678’.
When the DMA is triggered to initiate the memory-to-peripheral transfer, the DMA reads the buffer (TxBuffer) from the main memory as ‘12345678’. As a result, the DMA ends up transferring stale data to the peripheral.
The following figure illustrates the cache coherency issue observed when the DMA writes to the SRAM.

Figure 1-2. Peripheral-to-Memory Transfer (DMA Writes to SRAM)

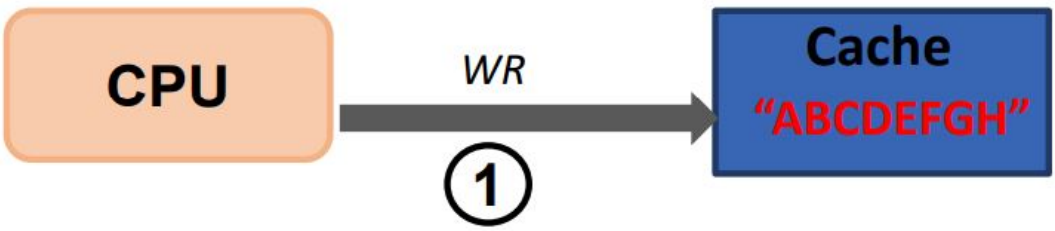


The application submits a request to receive data in the RxBuffer with a value of ‘12345678’ from the peripheral. The DMA populates the RxBuffer with a value of ‘12345678’ in the SRAM. However, the data cache is not updated, and it continues to hold the previous data. When the CPU reads the RxBuffer, it ends up reading the previous value contained in the buffer as ‘ABCDEFGH’.

Handling Cache Coherency
The two methods to handle the cache coherency issues are illustrated in Memory to Peripheral Transfer (DMA Reads from SRAM) and Peripheral-to-Memory Transfer (DMA Writes to SRAM). These methods involve the application managing the cache at run-time using the maintenance operations. The operations include the ability to perform these actions:
Invalidate the cache: Marks the cache lines as invalid. Subsequent access forces the data to be copied from the main memory to the cache.
Clean the cache: Writes the cache lines, which are marked as dirty, back to the main memory To handle the cache coherency discussed in Memory to Peripheral Transfer (DMA Reads from SRAM), perform the following actions:

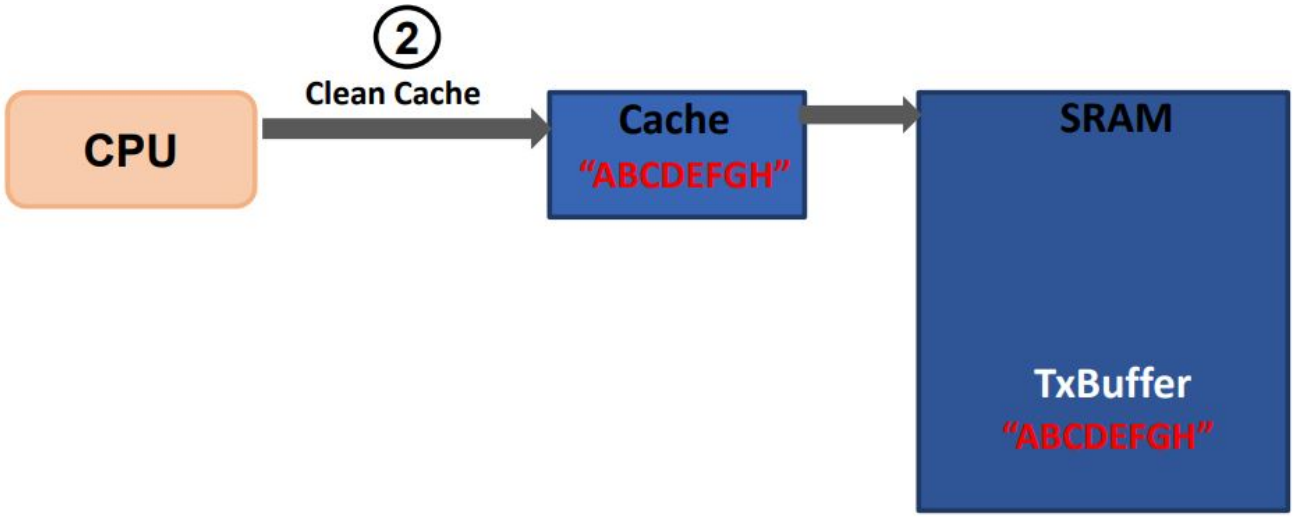
1. The application fills the write data buffer (TxBuffer) with a value ‘ABCEDFGH’. Due to the default cache policy(Write Back and Write Allocate), the written data may be in the cache.

   Figure 1-3. Populate Write Buffer



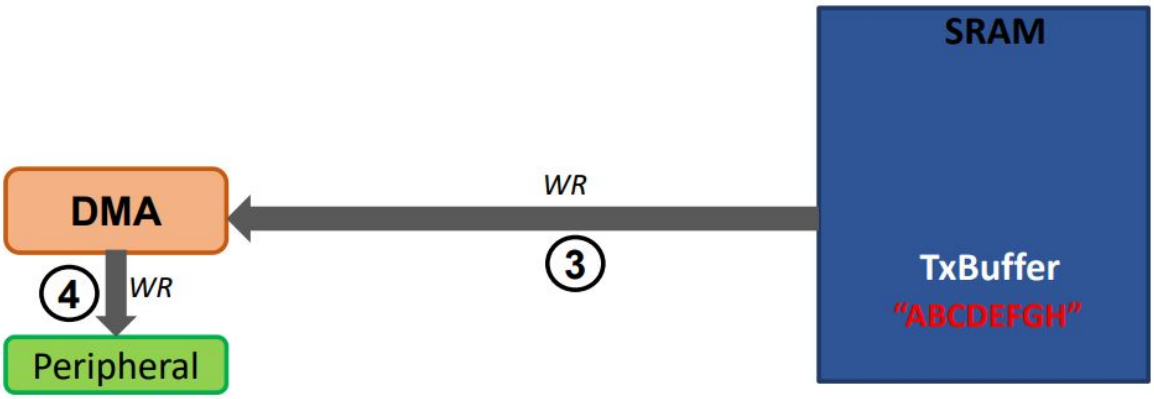
2. Flush the write data buffer (TxBuffer) with the value ‘ABCDEFGH’ to the main memory by calling the clean cache API.

   Figure 1-4. Flush Write Buffer



3. The application submits a request to transfer data from the TxBuffer with a value of 'ABCDEFGH' to the peripheral.

Figure 1-5. Write to Peripheral



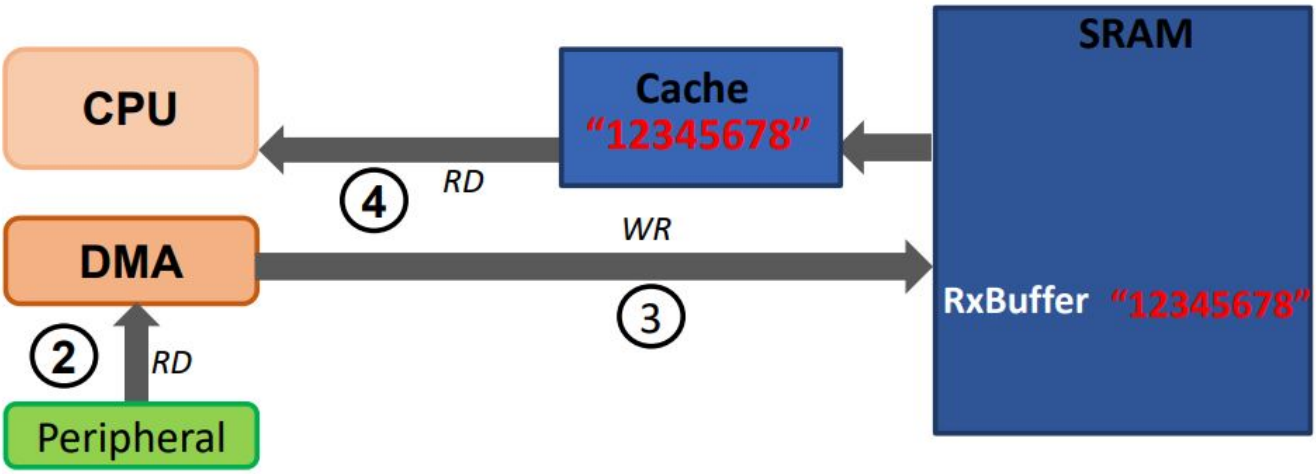
To handle the cache coherency as discussed in Peripheral to Memory Transfer (DMA Writes to SRAM), follow these steps:

1. The application calls the Invalidate cache API to mark the cache lines as invalid.

Figure 1-6. Invalidate Cache

2. The application submits a request to receive data in the RxBuffer with a value of '12345678' from the peripheral.
3. The DMA populates the RxBuffer with a value of '12345678' in the SRAM.
4. Because the cache line corresponding to the RxBuffer is in an invalid state, a read access by the CPU results in the RxBuffer being copied from the main memory into the data cache.

Figure 1-7. Handle Peripheral-to-Memory Transfer Cache Coherency

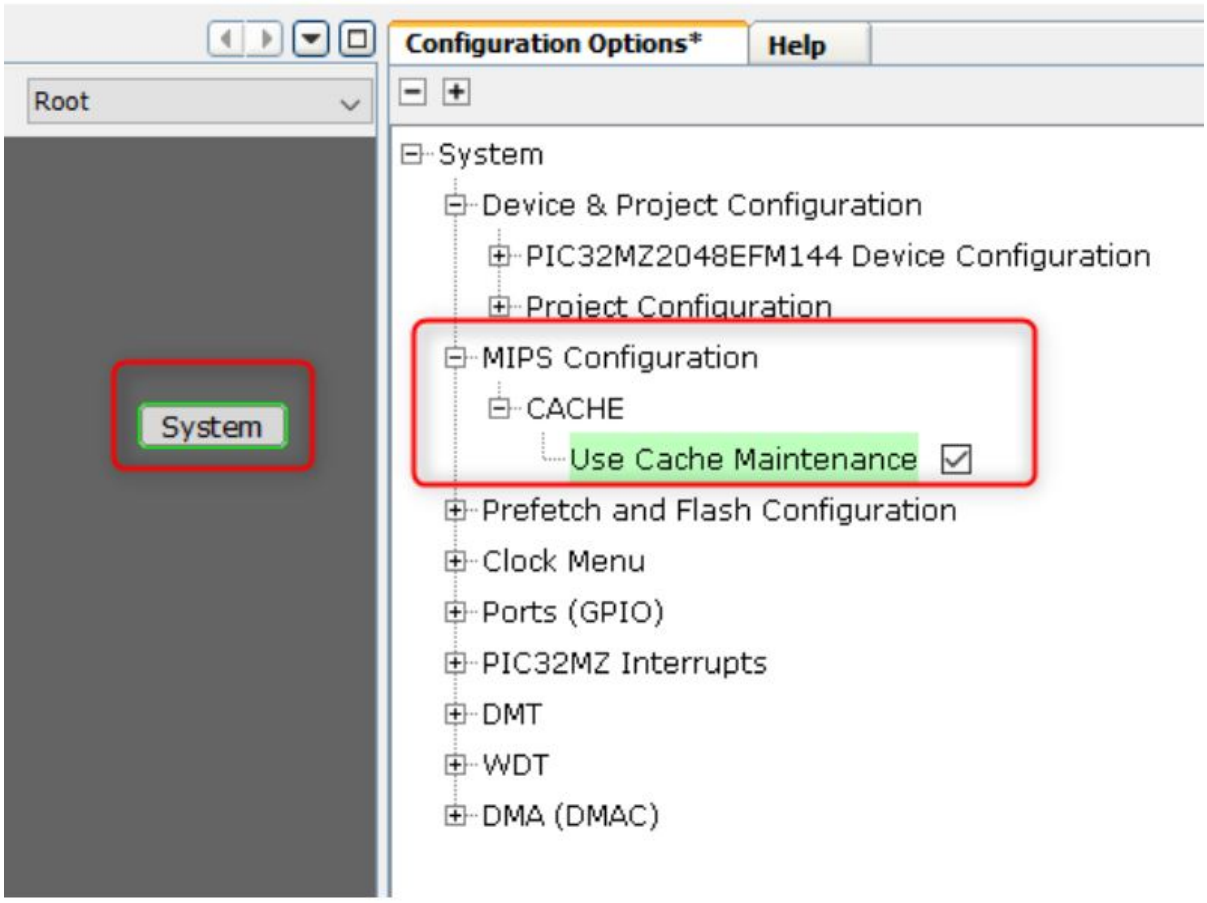


Implementation

Configuration

In an MPLAB Harmony v3 project for the PIC32 MZ EF, the cache maintenance operations are enabled by the MPLAB Harmony v3 Configurator (MHC) or MPLAB Code Configurator (MCC). In MHC or MCC, the configuration setting can be found under project graph > System > MIPS Configuration > Cache.

Figure 2-1. MHC Cache Configuration



Data-Cache Maintenance APIs

MPLAB Harmony v3 provides the following data-cache maintenance APIs:

Table 2-1. Data-Cache Maintenance APIs

Name	Description
DCACHE_INVALIDATE (void)	Invalidates the entire data cache before enablin g it.
DCACHE_CLEAN_BY_ADDR (uint32_t addr, size_t sz)	Write back and invalidate an address range in t he data cache.
DCACHE_INVALIDATE_BY_ADDR (uint32_t addr, size_t sz)	Invalidate an address range in the data cache.
DCACHE_CLEAN_INVALIDATE_BY_ADDR (uint32_t addr, si ze_t sz)	Write back and invalidate an address range in t he data cache.

Notes:

1. MCU specific data and instruction cache maintenance APIs are available as a peripheral library (PLIB) plib_cache.c. Refer to the PLIB application example at: **https://github.com/Microchip-MPLAB-Harmony/csp_apps_pic32mz_ef/tree/master/apps/cache/cache_maintenance.**
2. When using the cache clean and cache invalidate by address APIs:
    - **addr:** Must be aligned to the cache line size boundary. This means that the DMA buffer address must be aligned to the 16-byte boundary.
    - **dsize:** Must be a multiple of the cache line size. This means that the DMA buffer size must be a multiple of 16- bytes.

Example
The following code example demonstrates the usage of data-cache maintenance APIs along with the MPLAB Harmony v3 DMA peripheral library APIs to read and write data over the UART interface.

```
char __attribute__ ((aligned (16))) messageStart[] = "**** CACHE maintenance demo with UART
****\r\n\
**** Type a buffer of 10 characters and observe it echo back ****\r\n\
**** LED toggles on each time the buffer is echoed ****\r\n";
char __attribute__ ((aligned (16))) receiveBuffer[BUFFER_SIZE] = {};
char __attribute__ ((aligned (16))) echoBuffer[BUFFER_SIZE] = {};
char __attribute__ ((aligned (16))) messageError[BUFFER_SIZE] = "**** UART error occurred
****\r\n";

int main ( void )
{
/* Initialize all peripherals and modules */

While(1)
{
        if(readStatus == true)
        {
            readStatus = false;

        /* Fill the TxBuffer with the data to be transmitted.
    The TxBuffer may be in D-cache */

            memcpy(echoBuffer, receiveBuffer, READ_SIZE);
            echoBuffer[READ_SIZE] = '\r';
            echoBuffer[(READ_SIZE + 1)] = '\n';

            DCACHE_CLEAN_BY_ADDR((uint32_t)echoBuffer, sizeof(echoBuffer));

            DMAC_ChannelTransfer(DMAC_CHANNEL_0, echoBuffer, READ_SIZE+2,
            (const void *)&U2TXREG, 1, 1);
            LED_TOGGLE();
        }

        else if(writeStatus == true)
        {
            writeStatus = false;

            /* Invalidate cache lines having received buffer before using it
             * to load the latest data in the actual memory to the cache */
            DCACHE_INVALIDATE_BY_ADDR((uint32_t)receiveBuffer, sizeof(receiveBuffer));

            DMAC_ChannelTransfer(DMAC_CHANNEL_1, (const void *)&U2RXREG, 1,
         receiveBuffer, READ_SIZE, 1);
        }
}
/* Execution should not come here during normal operation */
return ( EXIT_FAILURE );
}
```

For detailed source code, refer to the PLIB application example at: https://github.com/Microchip-MPLAB-Harmony/csp_apps_pic32mz_ef/tree/master/apps/cache/cache_maintenance.

Note: The cache coherency issues discussed above can also be handled at link time by using the coherent variable attribute to the data buffer in contention.

unsigned int __attribute__((coherent)) buffer[1024];

In this code, the compiler allocates (at link time) the 1024 element in the non-cacheable memory region KSEG1.

References

The following documents are listed as resources. For additional information on cache coherency and related Microchip products, refer to the Microchip Website, or contact a local Microchip sales representative.

- Using L1 Cache on PIC32MZ Devices
- PIC32MZ EF Cache Maintenance PLIB Example
- MPLAB Harmony v3 Quick Docs package provides standalone help pages for users to get started developing applications on Microchip's 32-bit SAM and PIC32 MCUs. Download the quick_docs repository and start with the index.html file available in the docs folder.

  The online version is available at: microchip-mplab-harmony.github.io/quick_docs/.

- MPLAB Harmony v3 landing web page: **www.microchip.com/mplab/mplab-harmony**

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