

MICROCHIP SmartDesign MSS MSS and Fabric AMBA APB3 Design User Guide

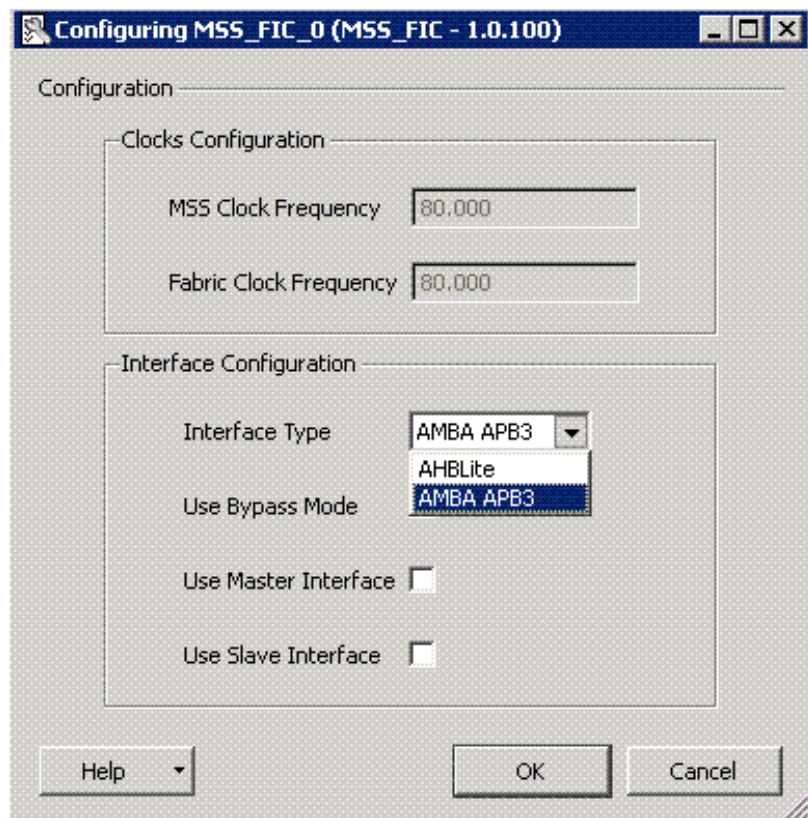
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MICROCHIP SmartDesign MSS MSS and Fabric AMBA APB3



Configuration and Connectivity

The SmartFusion Microcontroller Subsystem enables you to naturally extend the AMBA Bus into the FPGA fabric. You can configure the AMBA fabric interface as either APB3 or AHBLite depending on your design needs. A master and a slave bus interface is available in each mode. This document provides the essential steps to creating an MSS-FPGA fabric AMBA APB3 system using the MSS configurator available in the Libero® IDE software. APB peripherals are connected to the MSS using CoreAPB3 version 4.0.100 or greater. The following steps connect APB3 peripherals implemented in the FPGA fabric to the MSS.

MSS Configuration

Step 1. Select the MSS FCLK (GLA0) to fabric clock clock ratio.

Select the FAB_CLK divisor in the MSS Clock Management Configurator as shown Figure 1-1. You must perform post-layout static timing analysis to ensure that the design meets the timing requirements defined in the Clock Management Configurator. You may have to adjust the clock ratio between the MSS and the fabric to get a functional design.

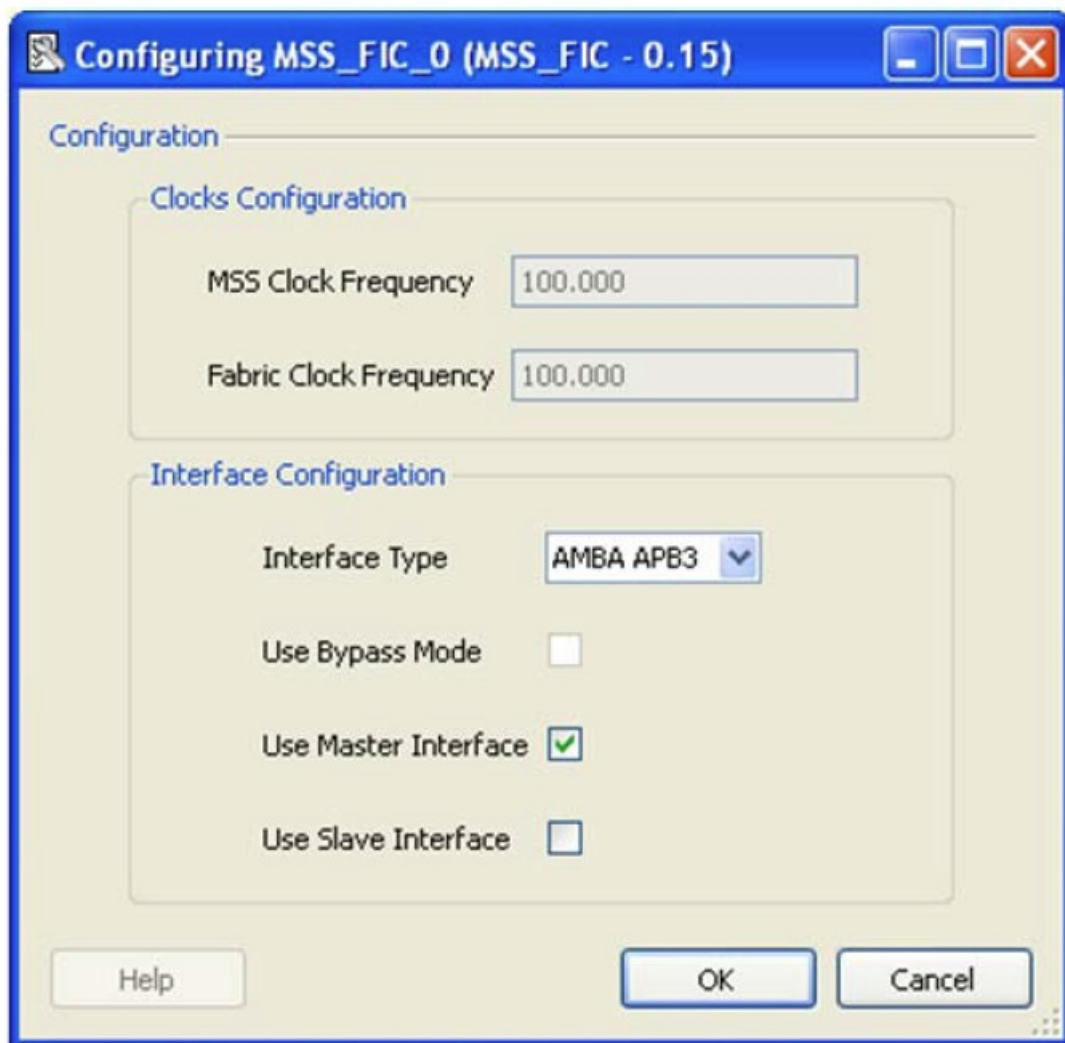


Figure 1-2 • AMBA APB3 Interface Selected

The AMBA and FAB_CLK are promoted to Top automatically and are available to any SmartDesign that instantiates the MSS.

Create the FPGA Fabric and AMBA Subsystem

The fabric AMBA subsystem is created into a regular SmartDesign component, and then the MSS component is instantiated into that component (as shown in Figure 1-5).

Step 1. Instantiate and configure CoreAPB3. APB Master Data Bus Width – 32-bit; the same width of the MSS AMBA data bus. Address Configuration – Varies depending on your slot size; see Table 1-1 for the correct values.

Table 1-1 • Address Configuration Values

	64KB Slot Size, up to 11 Slaves	4KB Slot Size, up to 16 Slaves	256 Byte Slot Size, up to 16 Slaves	16 Byte Slot Size, up to 16 Slaves
Number of address bits driven by the master	20	16	12	8
Position in slave address of upper 4 bits of master address	[19:16] (Ignored if master address width >= 24 bits)	[15:12] (Ignored if master address width >= 20 bits)	[11:8] (Ignored if master address width >= 16 bits)	[7:4] (Ignored if master address width >= 12 bits)
Indirect Addressing	Not in Use			

Enabled APB Slave Slots – Disable slots that you do not plan to use for your application. The number of slots available for the design is a function of the slot size selected. For 64KB only slots 5 to 15 are available due to fabric visibility from MSS memory map (from 0x4005000 to 0x400FFFFF). For smaller slot sizes, all slots are available. See the “Memory Map Computation” on page 7 for more details about slot sizes and slave/slot connection. Testbench – User License – RTL

Configuring CoreAPB3_0 (CoreAPB3 - 4.0.100)

Configuration

Data Width Configuration

APB Master Data Bus Width

☒ 32-bit ☐ 16-bit ☐ 8-bit

Address Configuration

Number of address bits driven by master: 20

Position in slave address of upper 4 bits of master address: [19:16] (Ignored if master address width >= 24 bits)

Indirect Addressing: Not in use

Allocate memory space to combined region slave

Slot 0: ☐ Slot 1: ☐ Slot 2: ☐ Slot 3: ☐
Slot 4: ☐ Slot 5: ☐ Slot 6: ☐ Slot 7: ☐
Slot 8: ☐ Slot 9: ☐ Slot 10: ☐ Slot 11: ☐
Slot 12: ☐ Slot 13: ☐ Slot 14: ☐ Slot 15: ☐

Enabled APB Slave Slots

Slot 0: ☐ Slot 1: ☐ Slot 2: ☐ Slot 3: ☐
Slot 4: ☐ Slot 5: ☒ Slot 6: ☒ Slot 7: ☒
Slot 8: ☐ Slot 9: ☐ Slot 10: ☐ Slot 11: ☐
Slot 12: ☐ Slot 13: ☐ Slot 14: ☐ Slot 15: ☐

Testbench: User

License:

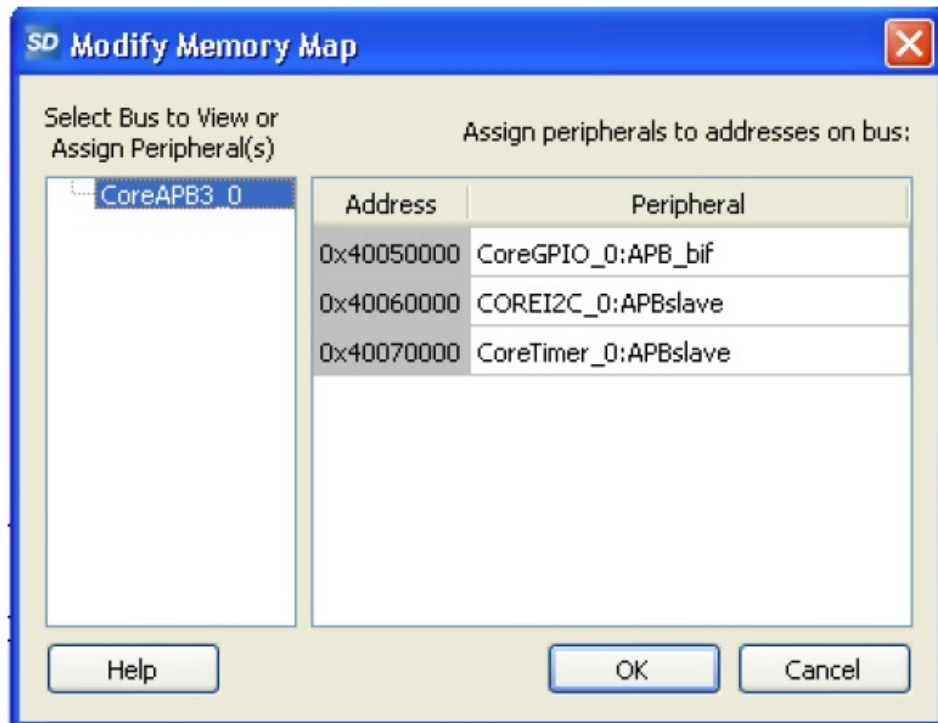
☐ Obfuscated ☒ RTL

Help OK Cancel

Step 2. Instantiate and configure AMBA APB peripherals in your design.

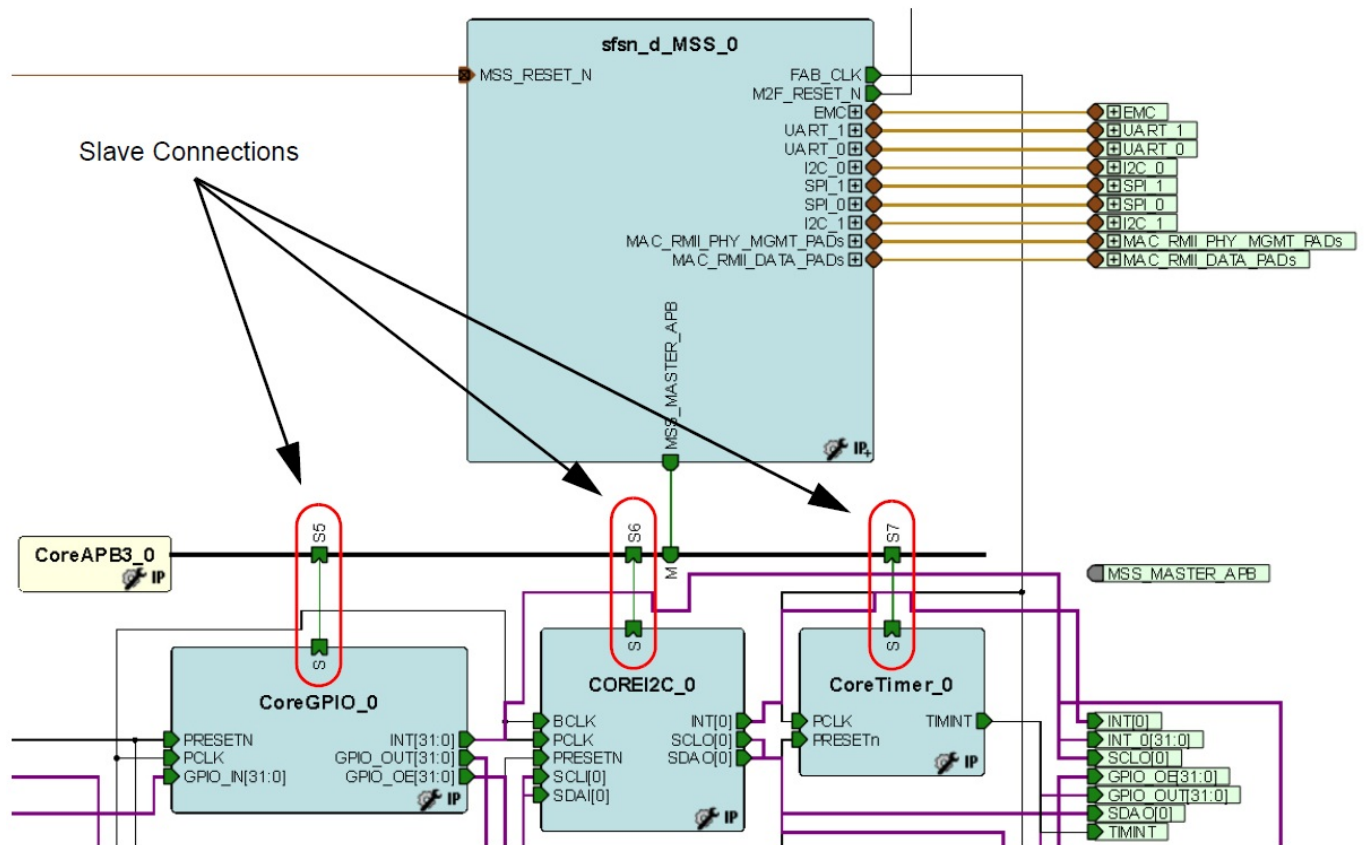
Step 3. Connect the subsystem together. This can be done automatically or manually. Automatic Connection – The SmartDesign auto-connect feature (available from the SmartDesign Menu, or by right-clicking the Canvas) automatically connects the subsystem clocks and resets and presents you with a Memory Map editor where you can assign the APB slaves to the proper addresses (Figure 1-4).

Note: that the auto-connect feature performs the clock and reset connections only if the FAB_CLK and M2F_RESET_N port names have not been changed on the MSS component.



Manual Connection – Connect the subsystem as follows:

- Connect the CoreAPB3 mirrored-master BIF to the MSS Master BIF (as shown in Figure 1-5).
- Connect the APB slaves to the proper slots as per your memory map specification.
- Connect FAB_CLK to PCLK of all APB peripherals in your design.
- Connect M2F_RESET_N to PRESET of all APB peripherals in your design.



Memory Map Computation

Only the following slot sizes are supported for MSS:

- 64 KB
- 4KB and below

General Formula

- For slot size equal to 64K, base address of client peripheral is: $0x40000000 + (\text{slot number} * \text{slot size})$
- For slot size less than 64K, base address of client peripheral is: $0x40050000 + (\text{slot number} * \text{slot size})$

The base address for the fabric is fixed at 0x4005000, but to simplify the memory map equation we show the base address as different in 64KB case.

Note: the slot size defines the number of addresses for that peripheral (i.e. 1k means there are 1024 addresses).

- **Example 1:** 64KB byte slot size 64KB slots = 65536 slots (0x10000).
- If the peripheral is at slot number 7, then, its address is: $0x40000000 + (0x7 * 0x10000) = 0x40070000$
- **Example 2:** 4KB byte slot size: 4KB slots = 4096 slots (0x1000)
- If the peripheral is at slot number 5, then, its address is: $0x40050000 + (0x5 * 0x800) = 0x40055000$

Memory Map View

You can view the system memory map by using the Reports feature (from the Design menu choose Reports). For example, Figure 2-1 is a partial memory map generated for the subsystem shown in

Address	Name	R/W	Width	Reset Value	Description
0x40050000	CTRL	R/W	8	0x00	
0x40050004	STAT	R	8	0xF8	
0x40050008	DATA	R/W	8	0x00	
0x4005000C	ADDR0	R/W	8	0x00	
0x40050010	SMB	R/W	8	0x78	
0x4005001C	ADDR1	R/W	8	0x00	

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call 800.262.1060
- From the rest of the world, call 650.318.4460
- Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by

email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request. The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support


For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select Yes in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page. Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at www.microsemi.com.

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Microsemi Corporate Headquarters

One Enterprise, Aliso Viejo CA 92656 USA Within the USA: +1 (949) 380-6100 Sales: +1 (949) 380-6136 Fax: +1 (949) 215-4996

Documents / Resources

	<p>MICROCHIP SmartDesign MSS MSS and Fabric AMBA APB3 Design [pdf] User Guide SmartDesign MSS MSS and Fabric AMBA APB3 Design, SmartDesign MSS, MSS and Fabric AMBA APB3 Design, AMBA APB3 Design</p>
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-  [Libero® SoC Design Suite Versions 2023.1 to 12.0 | Microchip Technology](#)

-  [Libero® SoC Design Suite Versions 2022.3 to 12.0 | Microchip Technology](#)
-  [Libero® SoC Design Suite Versions 2023.1 to 12.0 | Microchip Technology](#)
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