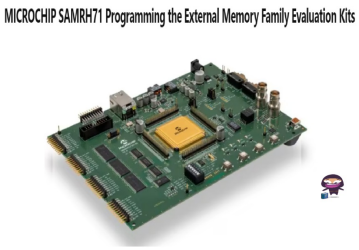


MICROCHIP SAMRH71 Programming the External Memory Family Evaluation Kits User Guide

Contents

MICROCHIP SAMRH71 Programming the External Memory Family Evaluation Kits

Specifications

- Product Name: SAMRH Family Evaluation Kits
- External Memory: Flash Memory
- Memory Devices:
  - SAMRH71F20-EK:
    - Memory Device: SST39VF040
    - Size: 4 Mbit
    - Organized as: 512K x 8
    - Mapped from: 0x6000_0000 to 0x6007_FFFF
  - SAMRH71F20-TFBGA-EK:
    - Memory Device: SST38VF6401
    - Size: 64 Mbit
    - Organized as: 4M x 16
    - Mapped from: 0x6000_0000 to 0x607F_FFFF
  - SAMRH707F18-EK:
    - Memory Device: SST39VF040
    - Size: 4 Mbit
    - Organized as: 512K x 8
    - Mapped from: 0x6007_FFFF

Product Usage Instructions

Prerequisites
This example runs on the versions listed below:

External Boot Memory Implementation
The SAMRH evaluation boards contain external flash memories connected to the NCS0 chip-select signals. NCS0 is configured in the HEMC to the 0x6000_0000 memory area at reset. This memory area can be mirrored to the Boot memory address via BOOT_MODE selection pins.

Memory Devices Features
The following table provides details about external flash memory for each evaluation kit:

Evaluation Kits	Memory Devices	Size	Organised as	Mapped from	Mapped to
SAMRH71F20-EK	SST39VF040	4 Mbit	512K x 8	0x6000_0000	0x6007_FFFF

Hardware Settings
This section provides the DIP switch configurations for the processor to boot from external memory.

SAMRH71F20-EK DIP Switch Configuration
The processor boots from external flash memory with a configurable data bus width set to 8-bit.

FAQ

Q: How do I know if my board is configured to boot from external memory?
A: Check the DIP switch settings according to the provided configurations in the user manual. Ensure the data bus width is correctly set for your evaluation kit.

Programming the External Memory of SAMRH Family Evaluation Kits using MPLAB-X with SAMBA Memory Handlers

Introduction

This application note explains how to make MPLAB-X IDE capable of programing and debugging the external boot memory embedded in the SAMRH family evaluation kits. This capability is provided by SAMBA Memory Handlers that are called from MPLAB-X IDE.
This document briefly describes the steps to set up MPLAB-X IDE projects that need to run from the external memory. Projects can be created from scratch or built from existing ones.

Prerequisites

This example runs on the versions listed below:

- MPLAB v6.15, or later versions
- SAMRH71 DFP packs v2.6.253, or later versions
- SAMRH707 DFP pack v1.2.156, or later versions

External Boot Memory Implementation

The SAMRH evaluation boards contain external flash memories which are connected to the NCS0 chip-select signals. NCS0 is configured in the HEMC to the 0x6000_0000 memory area at reset. This 0x6000_0000 memory area can be selected to be mirrored to the 0x0000_0000 Boot memory address via the BOOT_MODE selection pins at reset, see the relevant device datasheets.
The following table provides details about external flash memory for each evaluation kit.

Table 2-1. Memory Devices Features

Evaluation Kits	SAMRH71F20-EK	SAMRH71F20-TFBGA-EK	SAMRH707F18-EK
Memory Devices	SST39VF040	SST38VF6401	SST39VF040
Size	4 Mbit	64 Mbit	4 Mbit
Organised as	512K x 8	4M x 16	512K x 8
Mapped from	0x6000_0000		
To	0x6007_FFFF	0x607F_FFFF	0x6007_FFFF

The supplied SAMBA memory handlers have been developed to load data and code into these external flash memory devices while complying with the conditions exposed in the table above.

Hardware Settings

This section provides the DIP switch configurations that must be applied to the boards for the processor to boot from the external memory. The DIP switch configuration has been implemented according to the following convention:

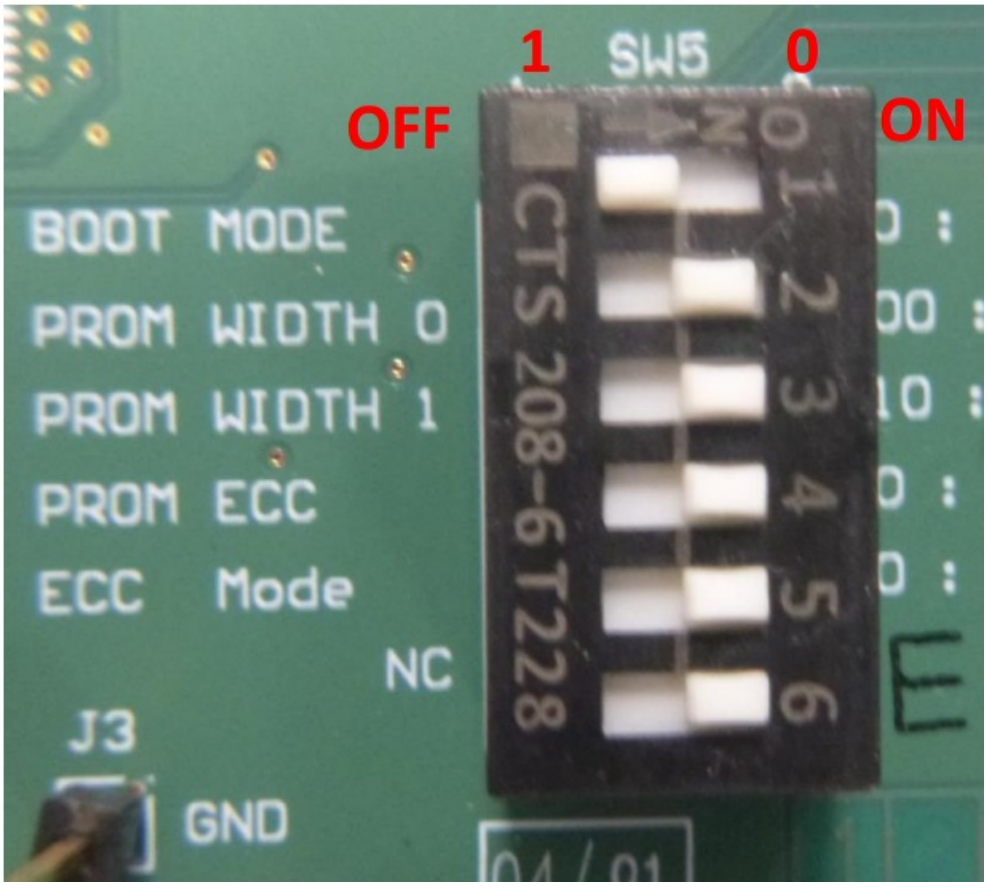
- The OFF position generates a logic 1
- The ON position generates a logic 0

SAMRH71F20-EK
On this kit the processor boots from external flash memory with a configurable data bus width that must be set to 8-bit.
The following table provides details about complete setting of the DIP switch.

Table 3-1. SAMRH71F20-EK Settings

SAMRH71F20 Processor				SAMRH71F20 EK	
Pin Numbers	**Pin Names**	**Function**	**Options**	**Selection**	**Required Configuration**
PF24	Boot Mode	Selects the memory boot	0: Internal Flash	External Flash	SW5-1 = 1 (OFF)
			1: External Flash		
PG24	CFG0	Selects the data bus width just for NSC0 chip select	CFG[1:0] = 00: 8 bit	8 bit	SW5-2 = 0 (ON)
			CFG[1:0] = 01: 16 bit		
PG25	CFG1		CFG[1:0] = 10: 32 bit		SW5-3 = 0 (ON)
			CFG[1:0] = 11: reserved		
PG26	CFG2	Selects the HECC activation/ deactivation **for all** NCSx	0: HECC Off	HECC Off	SW5-4 = 0 (ON)
			1: HECC On		
PC27	CFG3	Selects the HECC code correct or applied **for all** NCSx	0: Hamming	Hamming	SW5-5 = 0 (ON)
			1: BCH		
				Not Connected	SW5-6 = “Don’t care”

Figure 3-1. SAMRH71F20-EK DIP switch configuration



SAMRH71F20 – TFBGA – EK

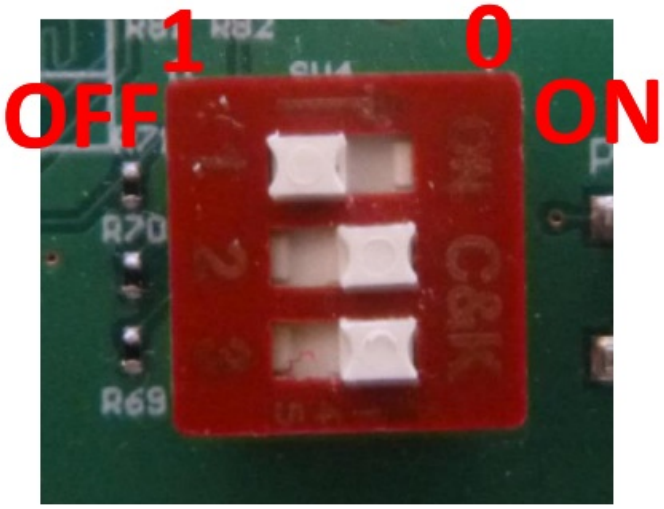
On this kit the processor boots from external flash memory with a configurable data bus width that has been hard-wired to 16-bit.

The following table provides details about complete setting of the DIP switch.

Table 3-2. SAMRH71F20-TFBGA-EK Settings

SAMRH71F20 Processor				**SAMRH71F20-TFBGA EK**		
Pin Numbers	**Pin Names**	**Function**	**Options**	**Selection**	**Required Configuration**	
PF24	Boot Mode	Selects the memory boot	0: Internal Flash	External Flash	SW4-1 = 1 (OFF)	
			1: External Flash			
PG26	CFG2	Selects the HECC activation / deactivation **for all** NCSx	0: HECC Off	HECC Off	SW4-2 = 0 (ON)	
			1: HECC On			
PC27	CFG3	Selects the HECC code corrector applied **for all** NCSx	0: Hamming	Hamming	SW4-3 = 0 (ON)	
			1: BCH			
PG24	CFG0	Selects the data bus width just for NSC0 chip select	CFG[1:0] = 00: 8 bit	16 bit	Hard Wired	PG24 = 1 (OFF)
			CFG[1:0] = 01: 16 bit			
PG25	CFG1		CFG[1:0] = 10: 32 bit			PG25 = 0 (ON)

Figure 3-2. SAMRH71F20-TFBGA-EK DIP switch configuration



Note:

“1” and “0” are inverted on the silkscreen of the board.

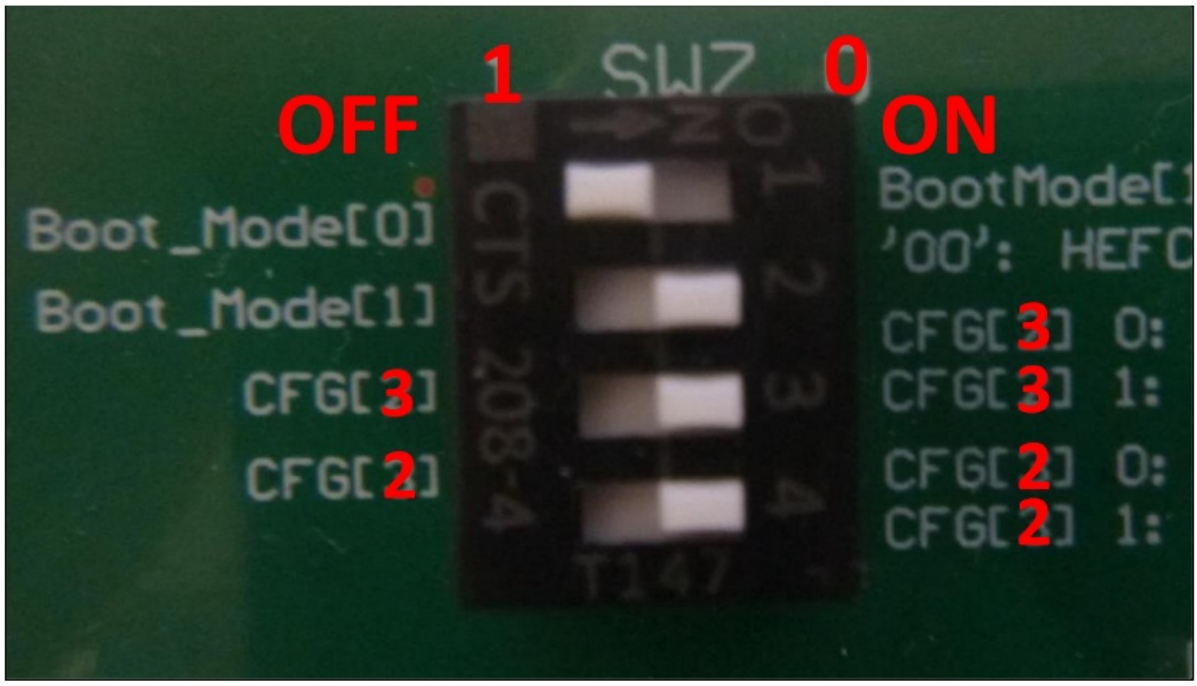
SAMRH707F18 – EK

On this kit the processor boots from external flash memory with a fixed 8-bit data bus width. The following table provides details about complete setting of the DIP switch.

Table 3-3. SAMRH707F18-EK Settings

<table>
<tr><th colspan="6">SAMRH707F18 Processor</th><th colspan="2">SAMRH707F18-EK</th></tr>
<tr><th>Pin Numbers</th><th>Pin Names</th><th colspan="3">Function</th><th>Options</th><th>Selection</th><th>Required Configuration</th></tr>
<tr><td>PC30</td><td>Boot Mode 0</td><td colspan="3" rowspan="2">Selects the boot memory</td><td>Boot Mode [1:0] = 00: Internal Flash (HEFC)</td><td rowspan="2">External Flash</td><td>SW7-1 = 1 (OFF)</td></tr>
<tr><td>PC29</td><td>Boot Mode 1</td><td colspan="2">Boot Mode [1:0] = 1X: Internal ROM</td><td>SW7-2 = 0 (ON)</td></tr>
<tr><td rowspan="5">PA19</td><td rowspan="5">CFG3</td><td colspan="4">Boot Mode [1:0] = 01 (External Flash)</td><td rowspan="5">N/A</td><td rowspan="5">SW7-3 = “Don’t care”</td></tr>
<tr><td colspan="2">Hamming code selected by default as HECC code corrector for all NCSx</td><td colspan="2">Internally driven to ‘0’</td></tr>
<tr><td colspan="4">Boot Mode [1:0] = 1X (Internal ROM)</td></tr>
<tr><td colspan="2" rowspan="2">Selects the active phase when the internal ROM is active</td><td colspan="2">0: Run Phase</td></tr>
<tr><td colspan="2">1: Maintenance Phase</td></tr>
<tr><td rowspan="7">PA25</td><td rowspan="7">CFG2</td><td colspan="4">Boot Mode [1:0] = 01 (External Flash)</td><td rowspan="7">HECC Off</td><td rowspan="7">SW7-4 = 0 (ON)</td></tr>
<tr><td colspan="2">Selects the HECC activation / deactivation for all NCSx when External Flash is active</td><td colspan="2">0: HECC Off</td></tr>
<tr><td colspan="2"></td><td colspan="2">1: HECC On</td></tr>
<tr><td colspan="4">Boot Mode [1:0] = 1X (Internal ROM)</td></tr>
<tr><td colspan="2" rowspan="4">Selects the communication mode when the Internal ROM is active</td><td colspan="2">0: UART Mode</td></tr>
<tr><td rowspan="3">1: SpaceWire Mode</td><td>Boot Mode 0 = 0</td></tr>
<tr><td>LVDS Interface</td></tr>
<tr><td>Boot Mode 0 = 1</td></tr>
<tr><td></td><td></td><td>TTL Mode</td></tr>
</table>

Figure 3-3. SAMRH707F18-EK DIP switch configuration



Note:
"CFG[2]" and "CFG[3]" are inverted on the silkscreen of the board.

Software Settings

The following section explains how to configure MPLAB X projects to run from external memory.

Board file
The board file is an XML file with the extension (*.xboard) that describes the parameters passed to SAMBA memory handlers. It must be placed in the user's MPLAB-X project folder.
For the SAMRH evaluation kits, the default name of the board file is "board.xboard", and its default location is the root folder of the project: "ProjectDir.X"
Two parameters contained in the board file must be configured by the user to make the file compliant with the structure of the user's application.
These two parameters are:

- [End_Address]: This parameter is related to the external boot memory size and defines the memory's last address.
- [User_Path]: This parameter defines the absolute path of SAMBA memory handlers' location.

The other parameters depend on SAMBA memory handler's implementation and can be kept at their default values.
The following figure provides a structure example of the board file.

Figure 4-1. Board file content example

Figure 4-1. Board file content example

```
<?xml version="1.0"?>
<ranges>
    <range start="0x60000000" end="[End_Address]" type="samba">
        <applet_type>InternalFlash</applet_type>
        <code_url>[User_Path]</code_url>
        <code_addr>0x21000000</code_addr>
        <mailbox_addr>0x21000004</mailbox_addr>
        <entry_addr>0x21000080</entry_addr>
        <instance>0</instance>
        <ioset>1</ioset>
    </range>
</ranges>
```

The following table provides the default user parameters of the board files supplied for the SAMRH evaluation kits.

Table 4-1. Board File Parameters

SAMRH Evaluation Kit	[End_Address]	[User_Path]
SAMRH71F20-EK	6007_FFFFh	${ProjectDir}\sst39vf040_loader_samba_sam_rh71_ek_sram.bin
SAMRH71F20-TFGBAEK	607F_FFFFh	${ProjectDir}\sst38vf6401_loader_samba_sam_rh71_tfbga_sram.bin
SAMRH707F18-EK	6007_FFFFh	${ProjectDir}\sst39vf040_loader_samba_sam_rh707_ek_sram.bin

Project Configuration

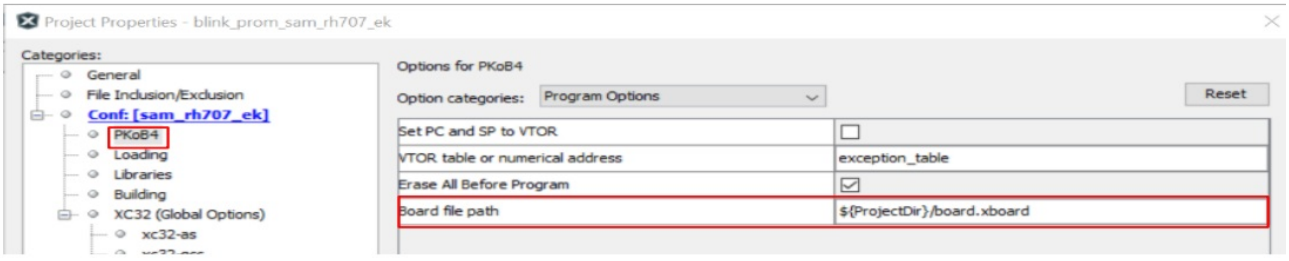
Board File

The board file must be defined in the “Board file path” field of the project properties of MPLAB X projects, as shown in the following figure. “Board file path” field is accessible from the debugger tool options (PKoB4 in our example), then “Program Options” is selected from the “Option Categories” menu.

By default, the board file path field is set to: ${ProjectDir}/board.xboard If the board file is not present in the folder, SAMBA memory handlers are ignored.

Figure 4-2. Declaration of the Board File in the MPLAB X project properties

Figure 4-2. Declaration of the Board File in the MPLAB X project properties

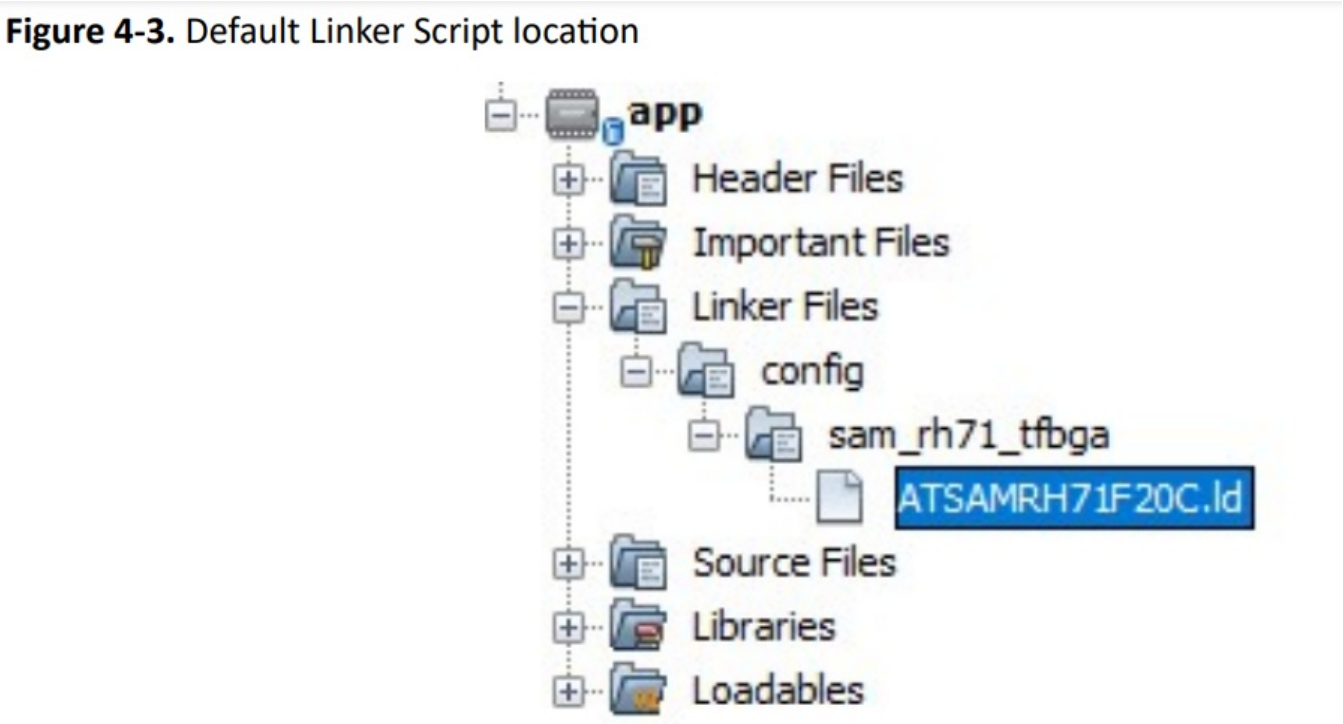


External Memory

MPLAB-X Harmony 3 (MH3) sample projects use a default linker script that configures the application to run from internal boot memory.

By default, the linker script file “ATSAMRH71F20C.ld” is implemented in harmony projects, as shown in the following figure.

Figure 4-3. Default Linker Script location



The linker script uses the internal parameters ROM_ORIGIN and ROM_LENGTH, as shown in the following figure, to define the location and length of the boot memory. The application depends on these parameters to create the executable.

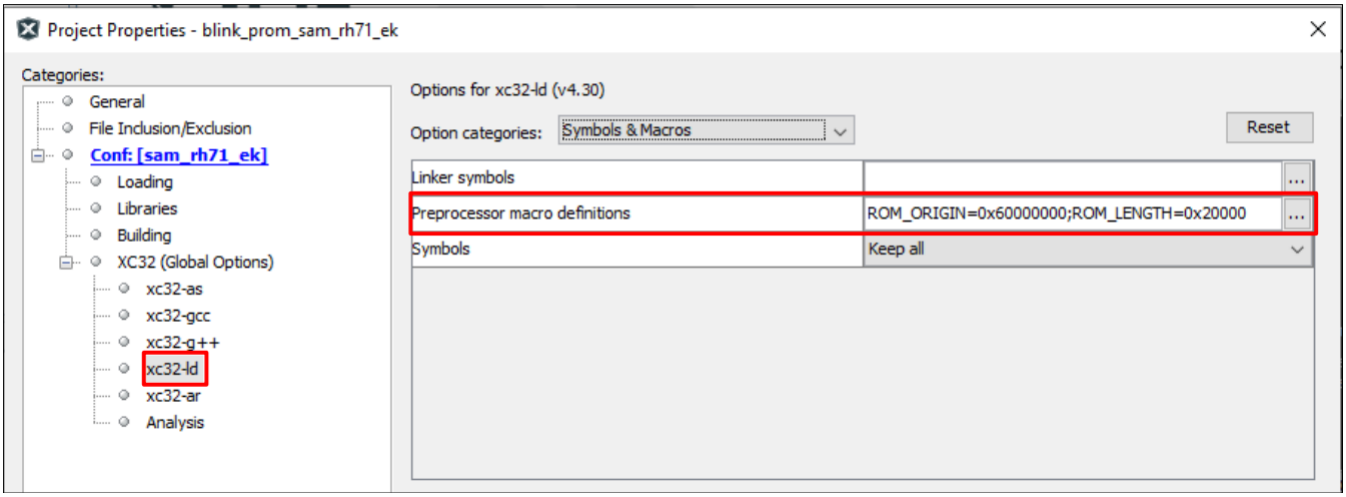
Figure 4-4. Linker Script's ROM_ORIGIN and ROM-LENGTH definitions

```
ENTRY(__XC32_RESET_HANDLER_NAME)

/*******************************************************************************
 * Memory-Region Macro Definitions
 * The XC32 linker preprocesses linker scripts. You may define these
 * macros in the MPLAB X project properties or on the command line when
 * calling the linker via the xc32-gcc shell.
 ******************************************************************************/

#ifndef ROM_ORIGIN
#  define ROM_ORIGIN 0x10000000
#endif
#ifndef ROM_LENGTH
#  define ROM_LENGTH 0x20000
#elif (ROM_LENGTH > 0x20000)
#  error ROM_LENGTH is greater than the max size of 0x20000
#endif
```

The sample linker script above limits the parameter ROM_LENGTH to 0x0002_0000 which is the length of the internal flash and generates a compilation error if this condition is not met.
However, this limitation may not be compliant with the use of the external flash memory, as its length could be greater than 0x0002_0000.
If the code programmed in the external memory is smaller than 0x0002_0000, there is no need to update the linker script file. However, if it exceeds this length, the ROM_LENGTH parameter should be updated to reflect the actual length of the external memory.
The ROM_ORIGIN parameter can also be overridden without modifying the linker script file.

Before overriding the ROM_LENGTH parameter, the linker script must be edited to match your hardware configuration.
To override the ROM_LENGTH parameter, you can use the “Preprocessor macro definitions” field in the MPLAB-X project properties. This field can be accessed from the “XC32-ld” item, and then
“Symbols & Macros” can be selected from the “Options Categories” menu, as shown in the following figure.

Figure 4-5. Preprocessor macro definitions field



For example, for the SST39VF040 flash memory device:
If the ROM_LENGTH has not been modified and the built code length should be smaller than 0x0002_0000.

- ROM_LENGTH=0x20000
- ROM_ORIGIN=0x60000000

If the ROM_LENGTH has been updated to 0x0008_0000 and the built code length should be smaller than 0x0005_0000.

- ROM_LENGTH=0x50000
- ROM_ORIGIN=0x60000000

Software Deliveries

SAMBA memory handlers’ mechanism is based on binary applets, which differ according to the processor version and the external boot memory implemented. There are three binary applets specific to the SAMRH evaluation kits:

- sst39vf040_loader_samba_sam_rh71_ek_sram.bin
- sst39vf040_loader_samba_sam_rh707_ek_sram.bin
- sst38vf6401_loader_samba_sam_rh71_tfbga_sram.bin

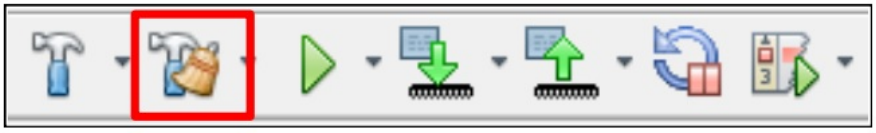
These applets run in the processor’s internal RAM and include both the SAMBA interface for communicating with debug scripts and the routines that perform programming operations (erase, write, and so on) on external boot memory.
Three zipped software packages are supplied to support the SAMRH evaluation kits. Each package includes:

- The dedicated board file
- The dedicated binary applet file.

Compiling, Programming, and Debugging from the External Boot Memory
Once the MPLAB X project has been completely setup with a valid SAMBA memory handler, user can compile, program, and debug this project in the external boot memory using the buttons and icon bar from the top menu, as shown in the following figures.

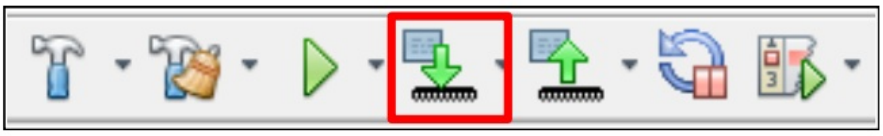
1. To clean and compile the project, click the Clean and Build.

Figure 6-1. Clean and Build Button



2. To program the application to the device, click the Make and Program.

Figure 6-2. Make and Program Button



3. To run the code, click the Debug Project.

Figure 6-3. Debug and Program Button

4. To stop the code, click the Finish Debugger Session.

Figure 6-4. Finish Debugger Session Button

    1. Or to pause it, click the Pause.

Figure 6-5. Pause Button

Reference

This section lists documents that provide more information about the MPLAB X, SAMRH71 and SAMRH707 devices.

MPLAB X
MPLAB X IDE User's Guide, DS50002027D. https://www.microchip.com/en-us/tools-resources/develop/mplab-x-ide#tabs

SAMRH71 Device

- SAMRH71F20 Device Datasheet, DS60001593
  ww1.microchip.com/downloads/en/DeviceDoc/SAMRH71_Datasheet_DS60001593F.pdf
- SAMRH71F20 Evaluation Kit User Guide, DS50002910.

https://ww1.microchip.com/downloads/en/DeviceDoc/SAMRH71F20-EK-Evaluation-Kit-User-Guide-DS50002910A.pdf

- SAMRH71-TFBGA-EK Evaluation Kit User Guide, DS50003449A
  https://ww1.microchip.com/downloads/aemDocuments/documents/AERO/ProductDocuments/UserGuides/
- Getting started with SAMRH71F20 Evaluation Kit, DS00004008.
  https://ww1.microchip.com/downloads/en/Appnotes/
- Getting_Started_with_the_SAMRH71F20_Evaluation_Kit_DS00004008A.pdf
- SST38LF6401RT and SAMRH71 Reference Design, DS0004274
  https://ww1.microchip.com/downloads/aemDocuments/documents/AERO/ApplicationNotes/ApplicationNo

SAMRH707 Device

SAMRH707F18 Device Datasheet, DS60001634
https://ww1.microchip.com/downloads/aemDocuments/documents/AERO/ProductDocuments/DataSheets/SAMRH707_Datasheet_DS60001634.pdf
Getting Started with SAMRH707F18 Microcontroller using MPLAB-X IDE and MCC Harmony Framework, DS00004478
https://ww1.microchip.com/downloads/aemDocuments/documents/AERO/ApplicationNotes/ApplicationNotes/00004478.pdf
SAMRH707-EK Evaluation Kit User Guide, DS60001744
https://ww1.microchip.com/downloads/aemDocuments/documents/AERO/ProductDocuments/UserGuides/SAMRH707_EK_Evaluation_Kit_User_Guide_60001744.pdf
SST38LF6401RT and SAMRH707 Reference Design, DS00004583
ww1.microchip.com/downloads/aemDocuments/documents/AERO/ApplicationNotes/ApplicationNotes/SAMRH707-SST38LF6401RT-Reference-Design-00004583.pdf

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	04/2024	Initial Revision

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	MICROCHIP SAMRH71 Programming the External Memory Family Evaluation Kits [pdf] User Guide SAMRH71, SAMRH71 Programming the External Memory Family Evaluation Kits, Programming the External Memory Family Evaluation Kits, External Memory Family Evaluation Kits, Family Evaluation Kits, Evaluation Kits, Kits

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