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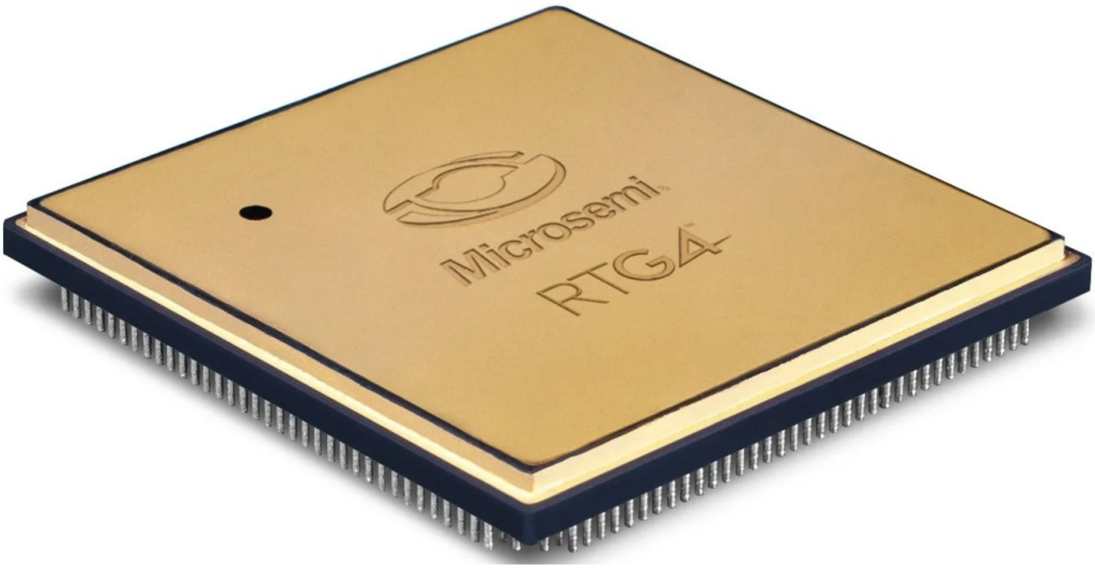
MICROCHIP RTG4 Radiation Tolerant Generation4



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INTRODUCTION

This Application Note describes various Vectron clock sources and interface circuits that can be used to drive the Reference Clock (REFCLK) Inputs of the SerDes Blocks of the RTG4 radiation-tolerant FPGA.

The Microchip RTG4 (Radiation-Tolerant Generation4) FPGA (Field Programmable Gate Array) can receive clock signals in two types of clock inputs:

1. Clock signals into the RTG4 general purpose and dedicated clock input pins, for use as a clock to the logic in the Digital Fabric.
2. Clock signals into the SerDes Blocks Reference Clock input pins, which input a reference clock for use by the dedicated high-speed SerDes Blocks on chip.

Of the two types of clock inputs, RTG4 REFCLK Inputs will be examined for this Application Note. The RTG4 REFCLK Inputs can be programmed by a FPGA designer to one of the various receiver types (differential or single-ended signal), and each has logic level requirements that will need direct interface or translation interface circuit connections to work properly when used with a standard clock driver (See Table 4). Information for providing clock input to the RTG4 Digital Fabric (type ‘1’ above) is not presented here, but it can be connected with a standard driver clock the same as providing clock input to the RTG4 REFCLK receivers.

In addition to listing and discussing these devices, this Application Note also summarizes the RTG4 REFCLK Inputs specification logic levels required for the clock source drivers with output logic levels presented in Table 4. The Application Note also shows setups and measurements with some typical waveforms tested in the RTG4 DevKit, to provide confidence that the solutions do work in hardware.

CLOCKS FOR DRIVING RTG4 FPGA REFCLK INPUTS

This application note details the use of multiple oscillator series, the required circuitry, and the corresponding settings for the RTG4 REFCLK. Table 1 provides a quick reference for customers for orderable oscillator part numbers at common frequencies. The oscillators listed are 2.5V or 3.3V single-ended CMOS or 3.3V complementary LVDS output, 100 krad minimum total ionizing dose (TID), and can be directly coupled to the RTG4 with the LVCMOS25, LVCMOS33, or LVDS25_ODT setting. The lowest cost options that meet full compliance for the screening levels of the RTG4 have been listed. Information after Table 1 is provided if other configurations, radiation levels (up to 300 krad), or oscillator enclosures are required. The information after Table 1 is also provided for compliance purposes.

TABLE 1: RECOMMENDED VECTRON HIGH RELIABILITY OSCILLATOR MODELS AT THREE PRIMARY REFERENCE CLOCK FREQUENCIES.

FPGA Screening Level	Main Clock Frequency	Output Logic	Oscillator Model Number	Vectron High Reliability Oscillator Standard Reference
ES, MS, Proto	100 MHz	CMOS	1157D100M0000BX	OS-68338
B			1157B100M0000BE	
EV, V			1157R100M0000BS	
ES, MS, Proto	100 MHz	LVDS	1203D100M0000BX	DOC203679
B			1203B100M0000BE	
EV, V			1203R100M0000BS	
ES, MS, Proto	125 MHz	CMOS	1403D125M0000BX	DOC204900
			1403D125M0000CX	
B	125 MHz	CMOS	1403B125M0000BE	DOC204900
			1403B125M0000CE	
EV	125 MHz	CMOS	1403R125M0000BS	DOC204900
			1403R125M0000CS	
ES, MS, Proto	125 MHz	LVDS	1203D125M0000BX	DOC203679
B			1203B125M0000BE	
EV, V			1203R125M0000BS	
ES, MS, Proto	156.25 MHz	LVDS	1203D156M2500BX	DOC203679
B			1203B156M2500BE	

EV, V			1203R156M2500BS	

If a program requires an alternate frequency, logic output, supply voltage, TID level, or oscillator enclosure, all of the following Vectron High Reliability Oscillator Standards are recommended for use as the REFCLK.

- LVDS (See Setup Figure 2 and Figure 4):
  - DOC203679, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, LVDS Output
  - DOC206903, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, 300 krad Tolerant, LVDS Output
- LVPECL (See Setup Figure 7, Figure 9, and Figure 11):
  - DOC203810, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, LVPECL Output
- CMOS (See Figure 13):
  - OS-68338, Oscillator Specification, Hybrid Clock, Hi-Rel Standard, CMOS Output (3.3V supply, 100 krad)
  - DOC206379, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, 300 krad Tolerant CMOS (3.3V supply, 300 krad)
  - DOC204900, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, High Frequency CMOS (2.5V/3.3V supply, 100 krad)

RTG4 FPGA REFCLK INPUTS

The RTG4 REFCLK Inputs can be configured, by the FPGA designer, to any one of the IO Standards listed below (Reference: Table 5 of UG0567 User Guide, RTG4 FPGA High-Speed Serial Interfaces).

TABLE 2: INPUT CONFIGURATION OPTIONS

SERDES_VDDI Supply	**3.3V**	**2.5V**	**1.8V**
	LVTTL/LVCMOS33	LVCMOS25	LVCMOS18

Supported Standards	LVDS33	LVDS25 (Note 1)	SSTL18-Class 1
	LVPECL	RSDS	SSTL18-Class 2
	RSDS	Mini-LVDS	HSLT18-Class 1
	Mini-LVDS	SSTL25-Class 1	—
	—	SSTL25-Class 2	—

Note

1. For LVDS33 and LVDS25, designers should reference RGT4 I/O Users Guide and DS0131 RTG4 FPGA data sheet for correct termination and common-mode recommendations to achieve optimal jitter performance.
2. HCSL inputs are supported directly with LVDS I/O STD inputs from the Libero. There is no specific HCSL I/O STD available in Libero and designs requiring HCSL are supported by using the LVDS25 I/O standard.

Programming the I/O Standard will also set the corresponding REFCLK Inputs type. The following popular REFCLK Inputs are presented in this Application Note with recommendations:

- **LVDS25_ODT:** ODT improves the signaling environment by reducing the electrical discontinuities introduced with off-die termination; thus, it enables reliable operation at higher signaling rates (Microchip_RTG4_FPGA_IO_user_Guide_UG0741_V4). This also provides the common-mode noise rejection on the transmission lines all the way to the receiver with the built-in ODT to reduce noise emission and noise interferences. An LVDS or LVPECL clock (interface circuit needed) can be used to drive the LVDS25_ODT.
- **LVDS25:** It is recommended to use LVDS25_ODT for best waveform and jitter performance. When LVDS25 is used an external differential termination is required. An external differential termination resistor of 200Ω (typical) may be implemented to improve the VID minimum requirement margin

when using with a standard LVDS driver.
The 200Ω load must be placed as close as possible to the RTG4 receiver input pins for better waveform and jitter performance.

- **LVDS33:** This is not recommended for use due to the minimum VID requirement of 0.50V, which is higher than a standard LVDS output differential voltage of 0.34V and is also higher than the minimum LVPECL output differential voltage of 0.470V according to Table 4.
- **LVPECL33:** This is not recommended for use due to the VICM requirement of 1.8V maximum, which is lower than the standard LVPECL output common mode voltage of 2.0V, and due to the VID requirement of 0.600V minimum, which is higher than the minimum LVPECL output differential voltage of 0.470V according to Table 4.
- **LVCMOS33/LVCMOS25:** This is recommended for use. These are single-ended REFCLK Inputs, requiring no interface translating circuit for simple direct connections to reduce component count. OS-68338 3.3V clock up to 100 MHz can be used for driving LVCMOS33. The 300 krad DOC206379 3.3V clock up to 80 MHz can be used for driving LVCMOS33. For faster speed, the high frequency 2.5V/3.3V CMOS clock of DOC204900 up to 125 MHz can be used for driving LVCMOS25 (used with 2.5V clock) or LVCMOS33 (used with 3.3V clock). The max operating frequency of the high frequency CMOS DOC204900 is 160 MHz, but the application is limited to 125 MHz due to the high input capacitance 20 pF max of the RTG4 receiver. This application limit is based on the output sink/ source current capability of the oscillator clocks and the capacitive load (20 pF in this case), using the power dissipation formula.

Capacitive-Load Power Consumption is calculated via the following equation.

EQUATION 1:

Where:
C = The load capacitance.
f = The signal frequency.
IC = The dynamic consumption current.

$P = C \times VCC^2 \times f = VCC \times IC$

$IC = C \times VCC \times f$

For example, at 125 MHz and 3.0V supply, the consumption current is calculated as 20 pF x 3.0V x 125 MHz = 7.5 mA, as expected to be lower than the recommended sink/source current of 12 mA (Reference: TI 54AC00-SP, output buffer used in the DOC204900 oscillator).

RTG4 REFCLK INPUT VOLTAGE SPECIFICATIONS AND DRIVER OUTPUT DATA

The input voltage requirements of the RTG4 REFCLK Inputs are listed in Table 3 to provide the specification limits to the driver output data presented in Table 4.

TABLE 3: RTG4 SERDES REFCLK INPUT VOLTAGE SPECIFICATIONS (Note 1)

REFCLK Input	Supply Voltage (VDDI)	VID (Note 2)			VICM (Note 2)		
		Min.	Typ.	Max.	Min.	Typ.	Max.
LVDS25_ODT	2.5V ± 5%	0.20V	0.35V	2.40V	0.05V	1.25V	1.50V
LVDS25	2.5V ± 5%	0.20V	0.35V	2.40V	0.05V	1.25V	2.20V
LVDS33 (Note 3)	3.3V ± 5%	0.50V	—	2.40V	0.60V	1.25V	1.80V
LVPECL33 (Note 3)	3.3V ± 5%	0.60V	—	2.40V	0.60V	—	1.80V

—		VIL			VIH		
LVCMOS 25	2.5V ± 5%	–0.30V	—	0.70V	1.7V	—	2.625V
LVCMOS 33	3.3V ± 5%	–0.30V	—	0.80V	2.0V	—	3.450V

Note

1. See Microchip RTG4_FPGA data sheet for more details on SerDes REFCLK Input Voltage Specifications.
2. Figure 1 depicts the VID and VICM for the differential inputs. Note that VID is half of VDiff, and is equivalent to a single-ended signal referenced from one input to ground.
3. Do not use LVDS33 and LVPECL33 as explained in the RTG4 FPGA REFCLK INPUTS section for LVDS33 and LVPECL33. These specification limits compared with the output data ranges in Table 4 are used to support this conclusion.

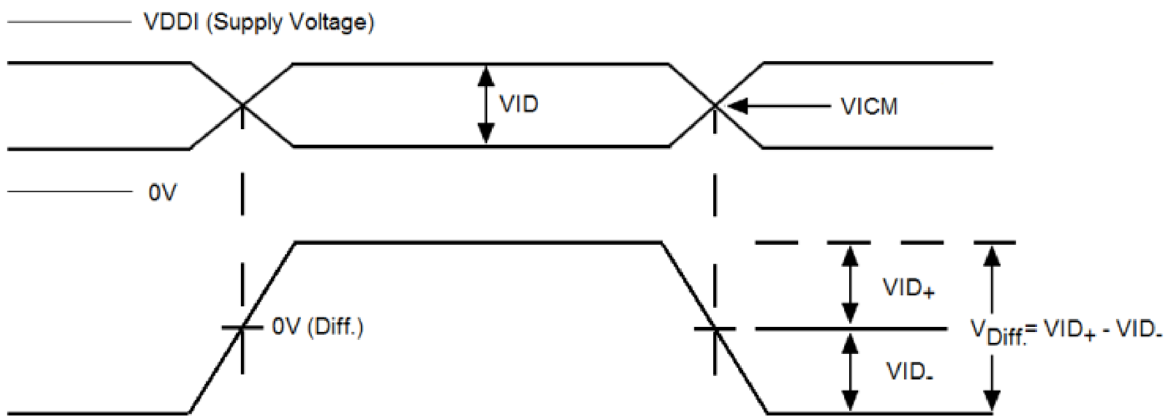


FIGURE 1: VID and VICM for Differential Inputs.

Also, the VICM and VID have to meet the conditions of the formulas below:

EQUATION 2:

$$VICM + (V ID/2) < VDDI + 0.4V$$

and

VICM- (VID/2)>–0.3V

TABLE 4: CLOCK DRIVER INTERFACE CONFIGURATION AND OUTPUT DATA (Note 1)

Setup Figure	Interface Configuration	VID (Note 2)			VICM (Note 2)		
		Min.	Typ.	Max.	Min.	Typ.	Max.
Figure 2 (Note 3)	LVDS to LVDS25_ODT Direct Interface	0.250 V	0.340 V	0.450 V	1.125 V	1.250 V	1.450 V
Figure 4 (Note 4)	LVDS to LVDS25 200Ω Termination	0.520 V	0.610 V	0.720 V	1.125 V	1.350 V	1.500 V
Figure 7 (Note 5)	LVPECL to LVDS25_ODT VICM 3.3V-Bias	0.470 V	0.800 V	0.950 V	Note 5	1.240 V	Note 5
Figure 9 (Note 6)	LVPECL to LVDS25_ODT VICM Self-Bias	0.470 V	0.800 V	0.950 V	1.030 V	1.233 V	1.437 V
Figure 11 (Note 7)	LVPECL to LVDS25_ODT VICM Self-Bias2	0.289 V	0.493 V	0.586 V	1.030 V	1.233 V	1.437 V
—		VIL			VIH		
Figure 13 (Note 8)	CMOS to LVCMOS33	0.297 V	0.330 V	0.363 V	2.673 V	2.970 V	3.267 V

(Note 8)	CMOS to LVCMOS25	0.237 V	0.250 V	0.263 V	2.138 V	2.250 V	2.363 V

Note

1. Output Data is recorded as VID and VICM to be consistent with the RTG4 REFCLK Inputs Voltage references. See the Setup Figures and resulted waveforms for details on the clock source use and interface circuits. Also see the Jitter Measurements section for additional information.
2. VID and VICM are referenced to Ground. VID is a single-ended signal measured at the input of the RTG4 receiver to correspond with the specification VID of the RTG4 REFCLK Inputs (see Note 2 of Table 3). All the logic levels also meet the conditions of the formulas required for the RTG4 REFCLK Inputs: VICM + (VID/2) < VDDI + 0.4V and VICM – (VID/2) > –0.3V.
3. **Setup Figure 2:** The VID and VICM limits are defined by the output voltage levels from Table 2 of Vectron DOC203679 for standard LVDS.
4. **Setup Figure 4:** The typical values of VID and VICM are determined by measurements.
5. **Setup Figure 7:** The VID range is determined using the output voltage levels from Table 2 of Vectron DOC203810, "Output Voltage: VOH = VCC – 1.085 to VCC – 0.880, VOL = VCC – 1.830 to VCC – 1.555".
   The biasing network resistors (R3 to R6) and its supply voltage will determine the VICM range for this scheme.
6. **Setup Figure 9:** The VID range is determined using the output voltage levels from Table 2 of Vectron DOC203810, "Output Voltage: VOH = VCC – 1.085 to VCC – 0.880, VOL = VCC – 1.830 to VCC – 1.555".
   The LVPECL output common mode voltage is calculated as VCC – 1.3V. With a VCC of 3.3V ±10%, the VICM ranges from 1.030V to 1.437V for this interface scheme with the resistor nominal values.
7. **Setup Figure 11:** The VID range is determined using the output voltage levels from Table 2 of Vectron
   DOC203810, "Output Voltage: VOH = VCC – 1.085 to VCC – 0.880, VOL =

VCC – 1.830 to VCC – 1.555”, and through the voltage divider, the 51Ω and 82Ω resistor network. The LVPECL output common mode voltage is calculated as VCC – 1.3V. With a VCC of 3.3V ±10%, the VICM ranges from 1.030V to 1.437V for this interface scheme with the resistor nominal values.

8. **Setup Figure 13:** The VIL and VIH range is determined by the standard CMOS logic levels as VIL = VCC x 0.1 and VIH = VCC x 0.9, where VCC is the supply voltage 3.3V ±10% or 2.5V ±5%.

COMPARISON OF RTG4 SCREENING LEVELS VS. OSCILLATOR SCREENINGS AND PEDIGREES

Due to differences in the requirements listed in MIL-PRF-38535 (for radiation hardened electronics) and MIL-PRF55310 (for crystal oscillators), exact matches in screening levels and component pedigrees are not available. Table 5 summarizes screening levels for the RTG4, and the recommended corresponding screening and pedigree levels for Vectron Oscillators. Customers are encouraged to review applicable specifications for mission critical applications to ensure full compliance.

TABLE 5: RTG4 SCREENING LEVELS VS. OSCILLATOR SCREENING AND PEDIGREES

RTG4 Screening Level	Oscillator Screening	Oscillator Component Pedigree	Description
ES, MS, Proto	X	D	Engineering Model Hardware using high reliability design with com- metrical grade components and non-swept quartz.
B	E	B	Military Grade Hardware using high reliability design with military grade components and swept quartz.

EV, V	S	R	Space Grade Hardware with 100 krad die, space grade components, and swept quartz.

GENERAL RECOMMENDATIONS AND SUMMARY

1. When an external resistor like the 200Ω termination for differential driving is used, it must be placed as close as possible to the differential receiver input pins. Otherwise, waveform and jitter will greatly degrade.
2. RTG4 differential receiver must be terminated at the inputs either with an external resistor (100Ω or 200Ω) or with ODT (RTG4 On-Die Termination) for all clock driver types for best waveform and jitter performance.
3. The clock oscillator driver should be placed as close as possible to the input pins of the RTG4 receiver to help reduce interferences and minimize reflection on the transmission line due to possible impedance mismatching.
4. It is recommended to use the drivers and interface circuits listed in Table 4. Do not use the RTG4 REFCLK Inputs LVDS33 and LVPECL33.

TABLE 6: RTG4 REFCLK INPUTS AND CLOCK DRIVER MATRIX

Signal Type	RTG4	Vectron Clock Driver					
	REFCLK Input	**Clock Type**	**Spec Drawing**	**Radiation Tolerance**	**Supply Voltage**	**Max. Frequency**	**Termination Circuit**
	LVDS25_ODT	LVDS	DOC203679	100 krad	3.3V	200 MHz	Direct Interface Figure 2
			DOC206903	300 krad	3.3V	200 MHz	
	LVDS25_ODT	LVPECL	DOC203810	50 krad (ELDRS)	3.3V	700 MHz	Figure 7, Figure 9, Figure 11

Differential	LVDS25	LVDS	DOC203679	100 krad	3.3V	200 MHz	200Ω, Figure 4
			DOC206903	300 krad	3.3V	200 MHz	
	LVDS33	Do Not Use					
	LVPECL33	Do Not Use					
Single-Ended	LVCMOS33	CMOS	OS-68338	100 krad	3.3V	100 MHz	Direct Interface Figure 13
			DOC204900	100 krad	3.3V	125 MHz	
			DOC206379	300 krad	3.3V	80 MHz	
	LVCMOS25	CMOS	DOC204900	100 krad	2.5V	125 MHz	Direct Interface Figure 13

For differential signal application, the only choice for RTG4 to set to is LVDS25_ODT (used with LVDS or LVPECL clock driver) or LVDS25 (used with LVDS clock driver and external 200Ω termination). The CMOS single-ended signal solution offers the best Total Jitter and Deterministic Jitter performance (See Jitter Measurements Table 7, Table 8, and Table 9), simple direct interface and options to use either the 2.5V or 3.3V supply, but speed is limited to 100 MHz (OS-68338), 80 MHz (DOC206379) and 125 MHz (DOC204900) for the three Vectron CMOS clocks.

CIRCUIT INTERFACE AND DATA

FIGURE 2: LVDS to RTG4 LVDS25_ODT, Direct Interface.

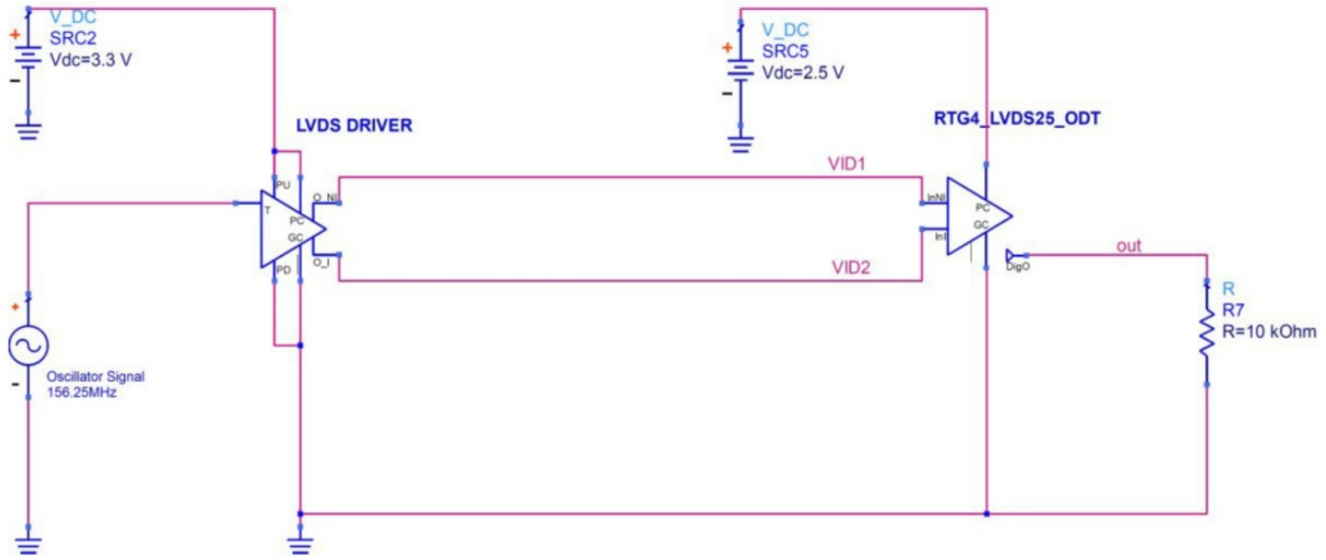
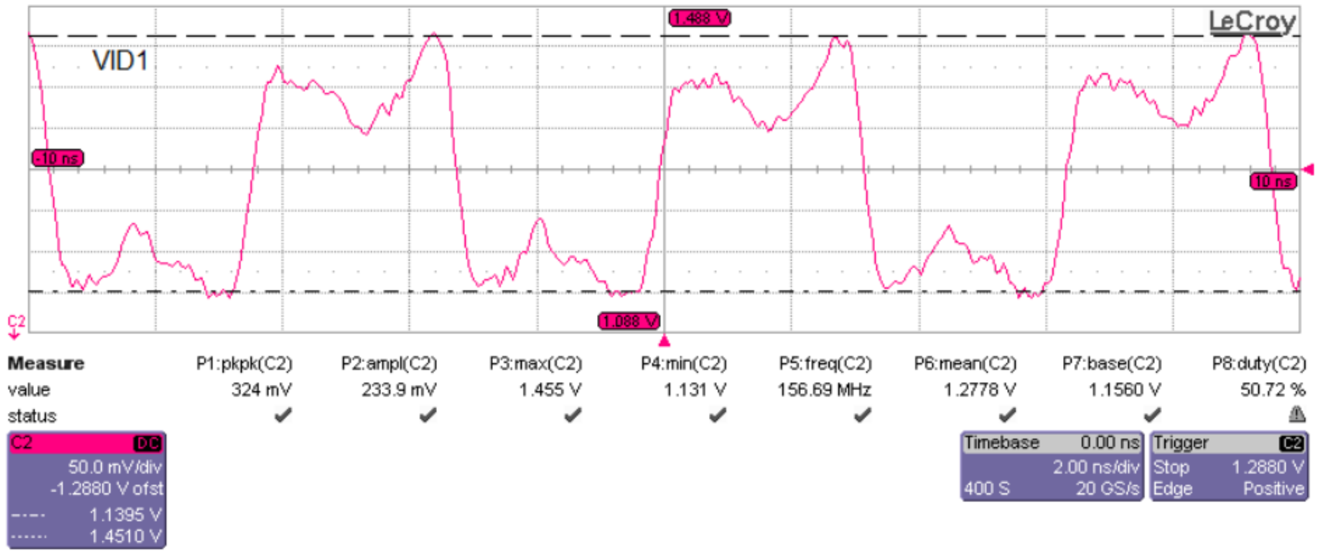
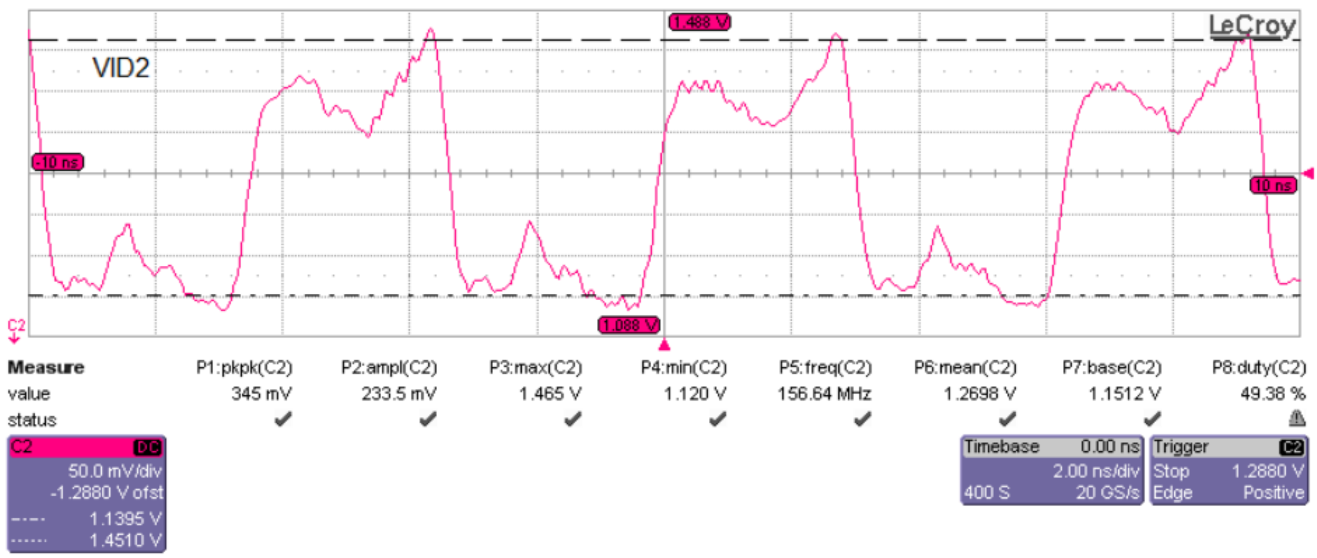


FIGURE 3: Measured Waveforms, LVDS to LVDS25_ODT, Direct Interface (Waveforms Measured on RTG4 DevKit).





Note

2. A LeCroy active probe ZS1500 1.5 GHz was used for the measurements. VID1 and VID2 were measured with reference to Ground at room temperature.
3. See Figure 2 for the setup diagram. The oscillator clock driver (1204R156M25000BF used) was mounted on the RTG4 DevKit in place of the REFCLK 125 MHz (disabled and isolated) and the whole board was tested over temperature from –40°C to +85°C with Microchip EPCS Demo GUI software used to check for the error-free transmission loop.

FIGURE 4: LVDS to RTG4 LVDS25 External 200Ω Termination.

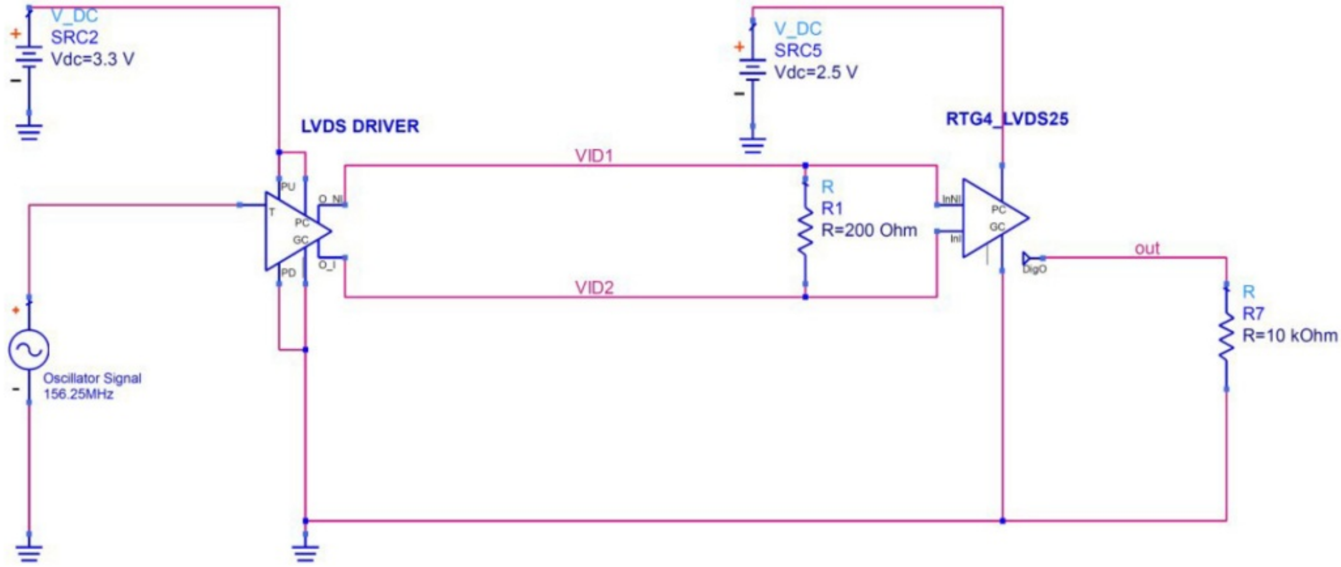
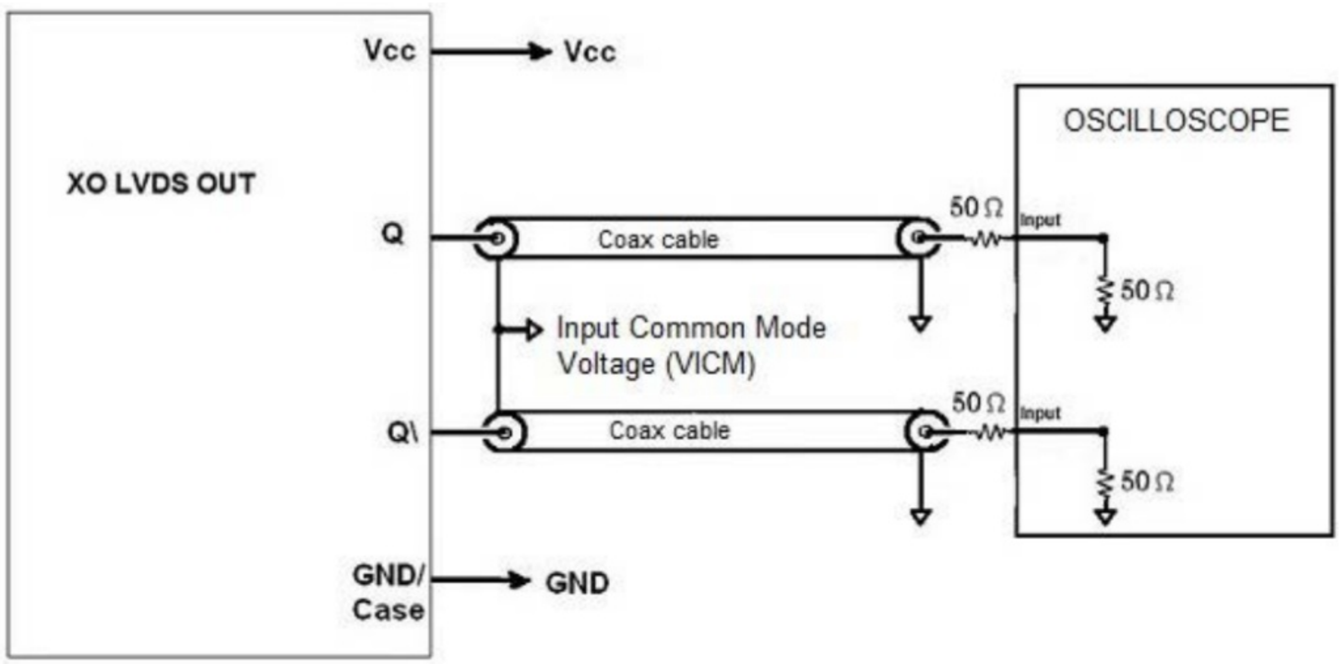


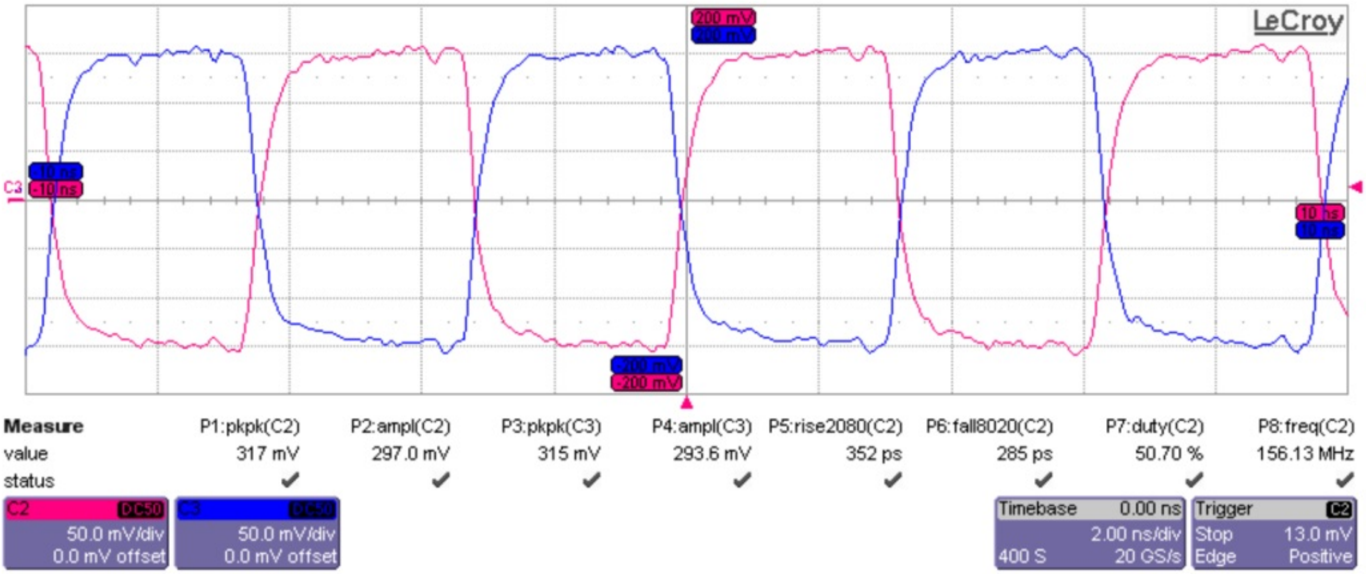
FIGURE 5: Setup Diagram for LVDS 200Ω Termination.



Note

1. This test setup was used to measure the waveforms for the diagram Figure 4 to present here in place of the waveforms measured on the RTG4 DevKit. The waveforms measured on the DevKit using the setup of Figure 4 were not so representative because the 200Ω load resistor used with the RTG4 LVDS25 couldn’t be placed as close to the receiver inputs as recommended to obtain good waveforms.
2. The load was placed at the input of the oscilloscope for better waveform measurements. Only half of the signal was measured using this setup. The 50Ω series resistors connected via the oscilloscope ground form a load of 200Ω between two outputs of the LVDS oscillator. The clock source used was 1204R156M25000BF.

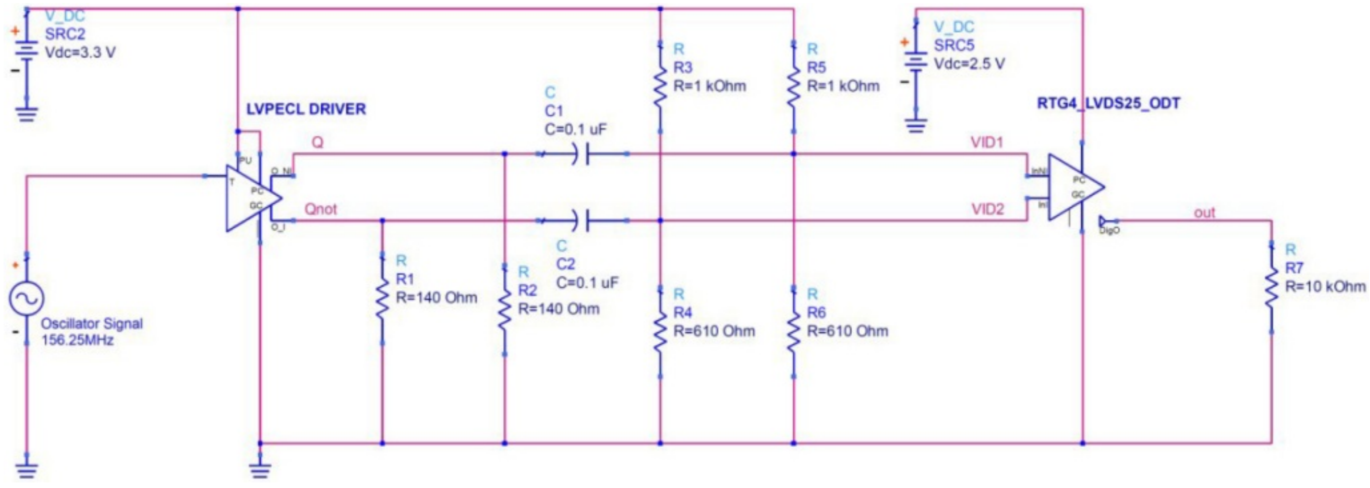
FIGURE 6: Measured Waveforms, LVDS to LVDS25, External 200Ω Termination (Waveforms Measured with Bench Fixture and 50Ω Coax Cables).



Note

1. The actual signal is two times the measured value, as explained in Figure 5. Waveform was measured at room temperature.

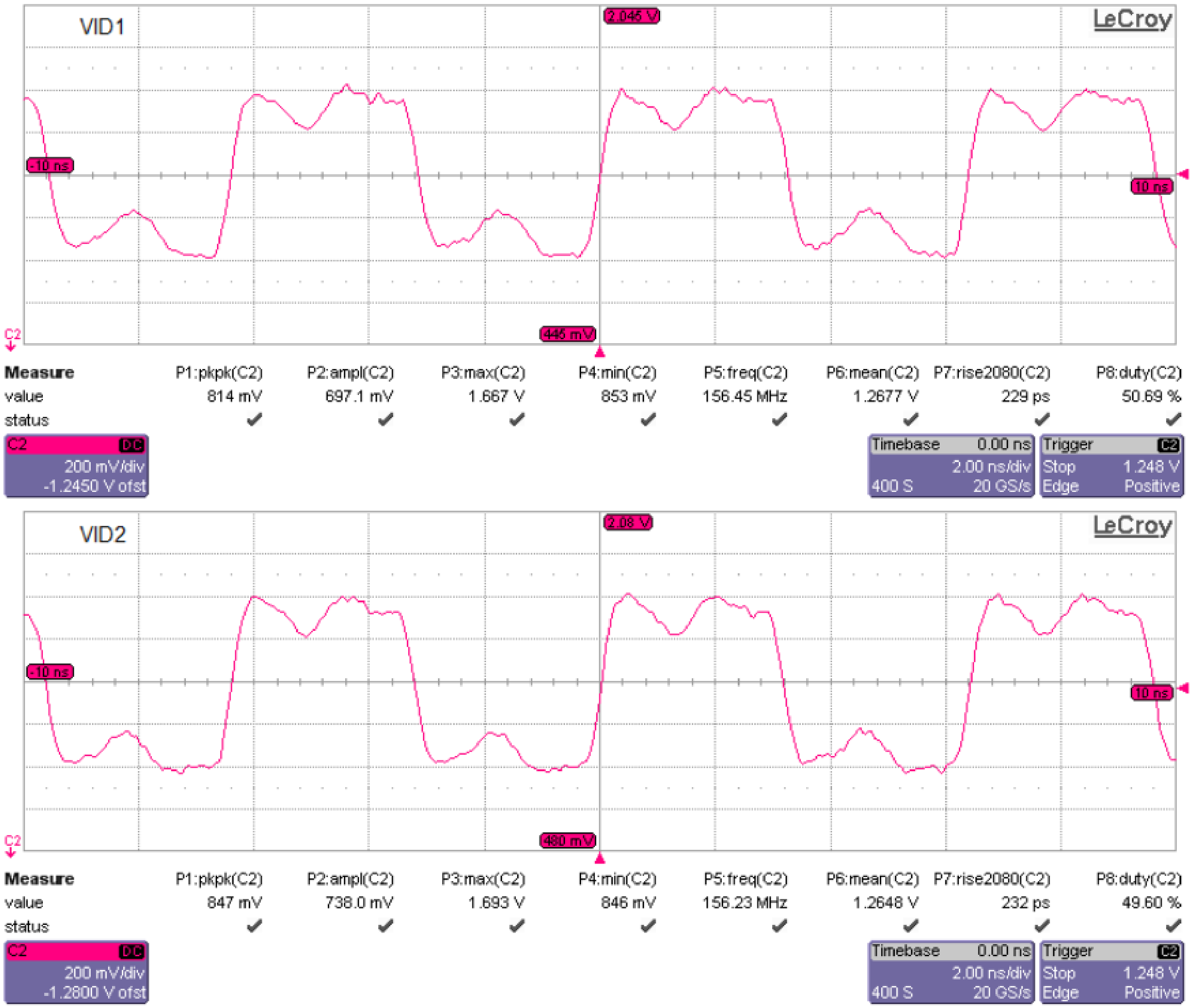
FIGURE 7: LVPECL to LVDS25_ODT, VICM 3.3V-Bias.



Note

1. Use 1 kΩ for R4 and R6 if a supply voltage of 2.5V is used for the biasing network.
2. C1 and C2 of 0.1 µF not only serve as a DC block, but also provide a full LVPECL differential signal swing to drive the receiver with little attenuation. The AC-coupling capacitors should have low ESR and low inductance at targeted clock frequency.

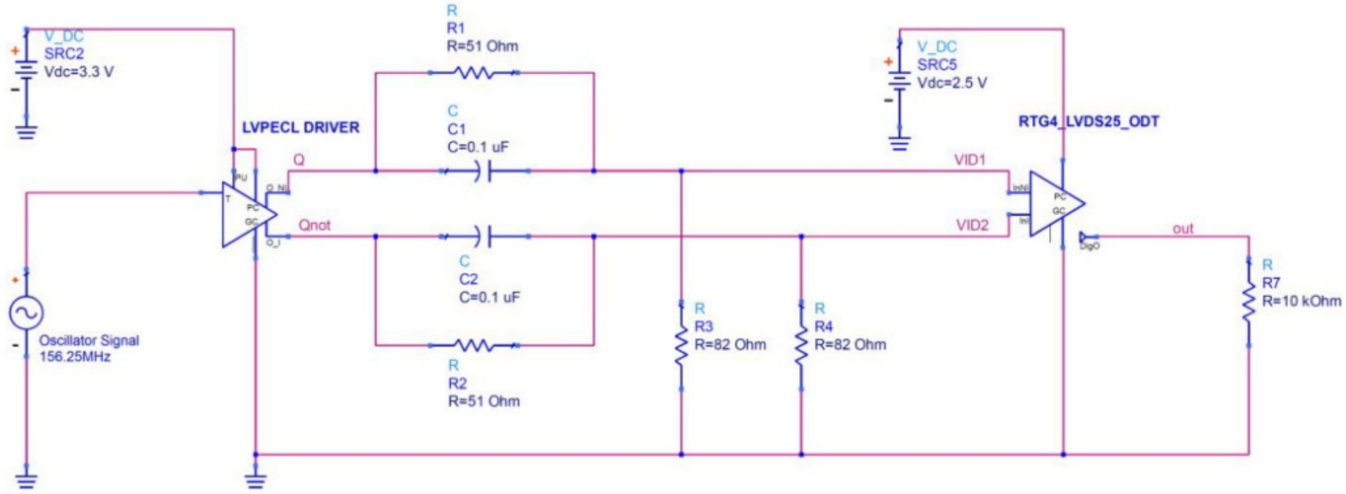
FIGURE 8: Measured Waveforms, LVPECL to LVDS25_ODT, VICM 3.3V-Bias (Waveforms Measured on RTG4 DevKit).



Note

1. A LeCroy active probe ZS1500 1.5 GHz was used for the measurements. VID1 and VID2 were measured with reference to Ground at room temperature.
2. See Figure 7 for the setup diagram. The oscillator clock driver (1304R156M25000BF used) was mounted on the RTG4 DevKit in place of the REFCLK 125 MHz (disabled and isolated) for testing.

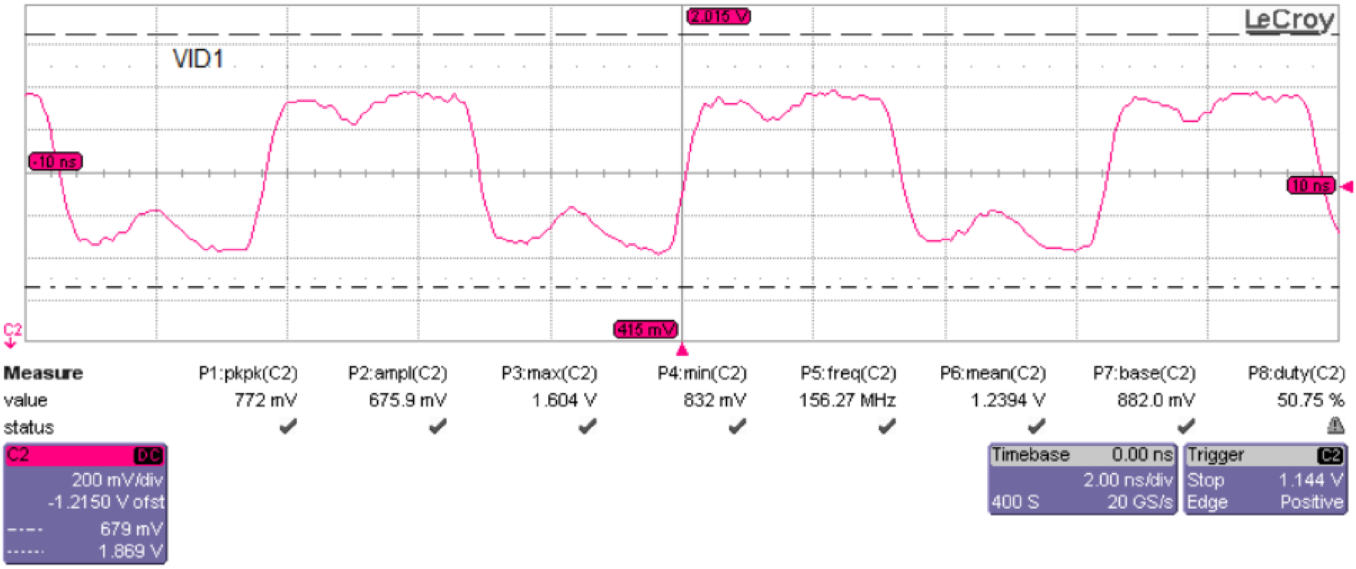
FIGURE 9: LVPECL to LVDS25_ODT, V*ICM* Self-Bias.

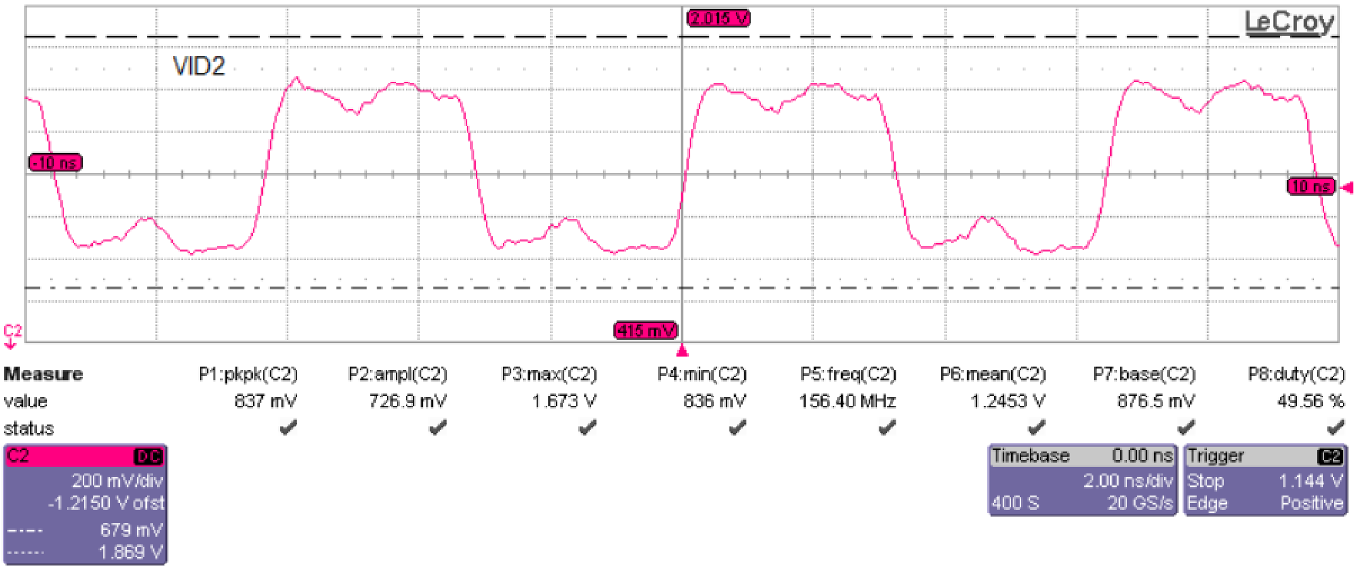


Note

1. This VICM Self-Bias Termination is an alternative to that of Figure 7. This scheme requires no external supply voltage for the biasing and saves two resistors over that of Figure 7.
2. C1 and C2 of 0.1 µF provide a full LVPECL differential signal swing to drive the receiver with little attenuation. The AC-coupling capacitors should have low ESR and low inductance at targeted clock frequency.

FIGURE 10: Measured Waveforms, LVPECL to LVDS25_ODT, VICM Self-Bias (Waveforms Measured on RTG4 DevKit).

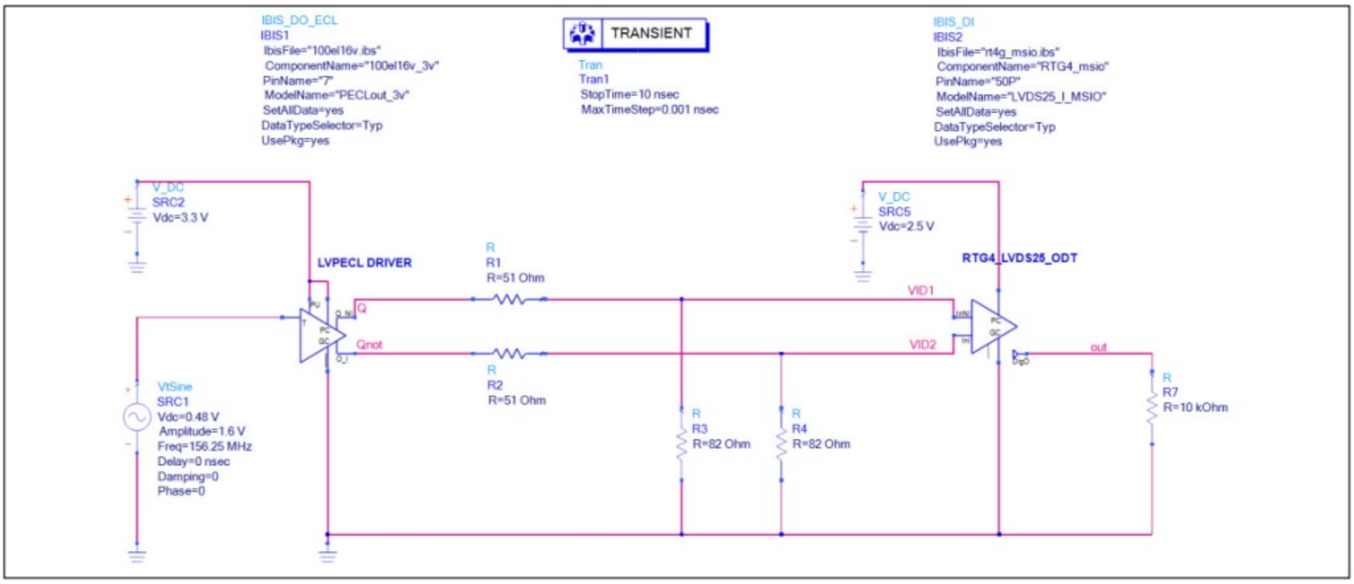




Note

1. A LeCroy active probe ZS1500 1.5 GHz was used for the measurements. VID1 and VID2 were measured with reference to Ground at room temperature.
2. See Figure 9 for the setup diagram. The oscillator clock driver (1304R156M25000BF used) was mounted on the RTG4 DevKit in place of the REFCLK 125 MHz (disabled and isolated) for testing.

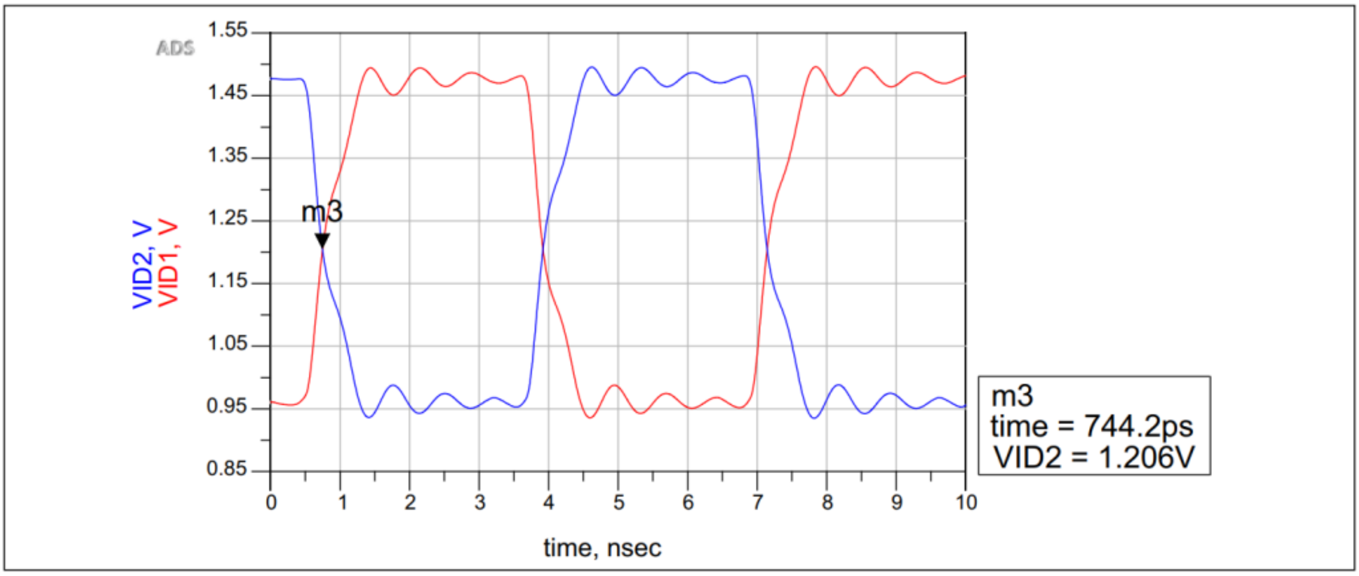
FIGURE 11: LVPECL to LVDS_ODT, VICM Self-Bias2.



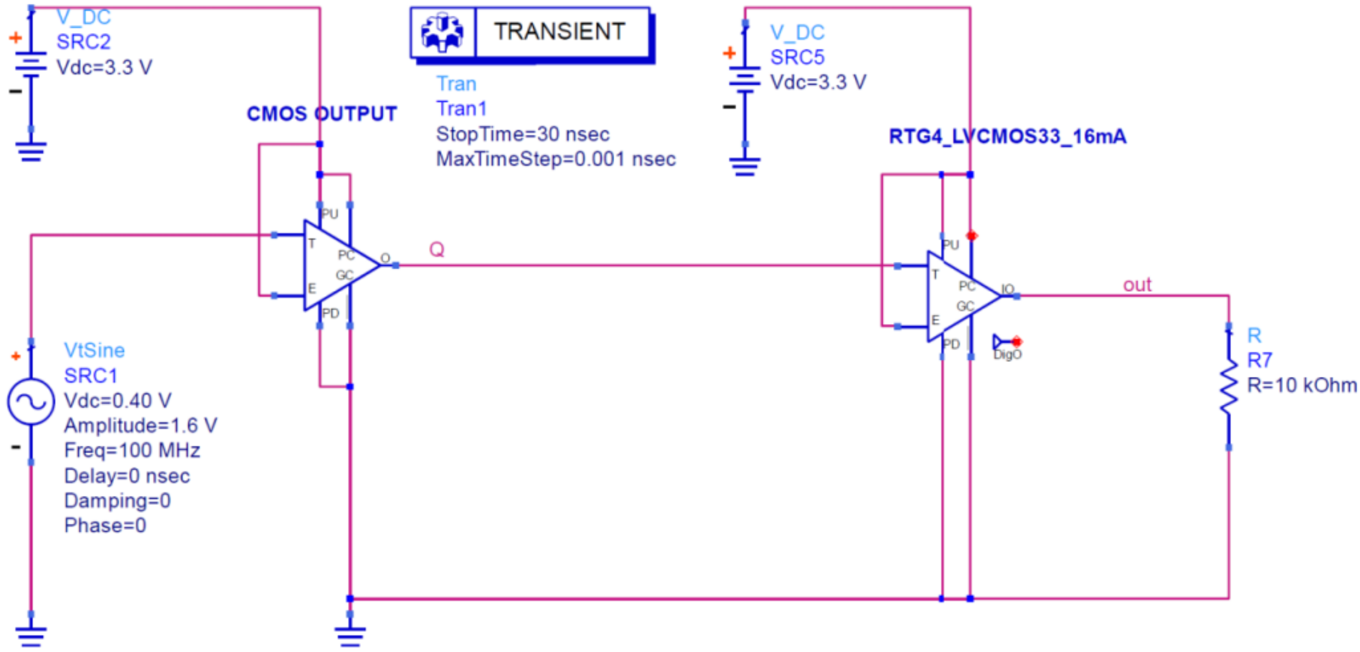
Note

1. This VICM Self-Bias termination is similar to the setup of Figure 9 without the coupling capacitors C1 and C2. The driver output signal is divided down by the resistor network but is still large enough to drive the RTG4 LVDS25_ODT. The rad-hard oscillator 1304R156M25000BF can be used for the clock source.

FIGURE 12: Simulated Waveforms, LVPECL to LVDS25_ODT, VICM Self-Bias2 (Keysight ADS 2017 software used).



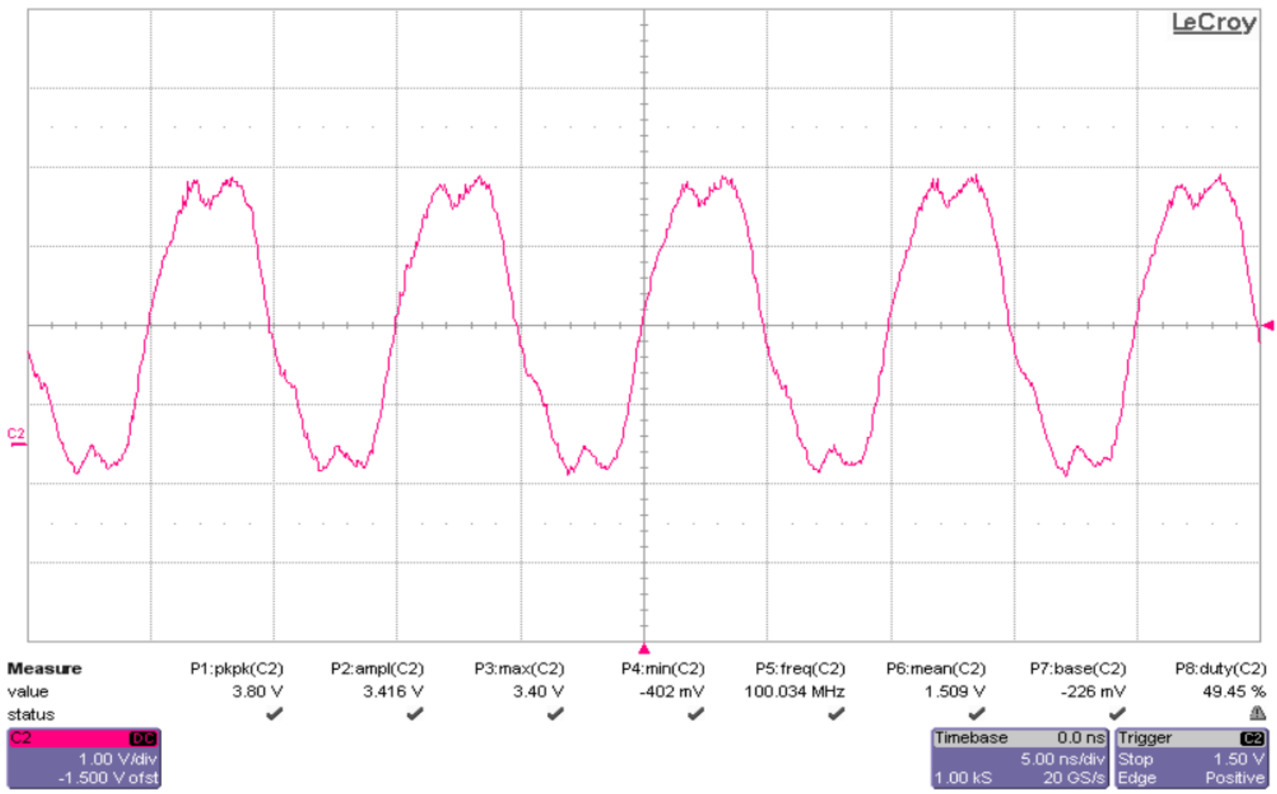
IGURE 13: CMOS to RTG4 LVCMOS33.



Note

1. A Vectron OS-68338 1103R100M00000BF 3.3V CMOS clock was used in the setup to drive the RTG4 LVCMOS33 and the waveform at Q was measured and presented in Figure 14.

FIGURE 14: Measured Waveforms, CMOS CLOCK (OS-68338 100 MHz) to LVCMOS33.



Note

1. A LeCroy active probe ZS1500 1.5 GHz was used for the measurement. The waveform was measured at the output of the clock driver at room temperature.
2. See Figure 13 for the setup diagram. The oscillator clock driver (1103R100M00000BF used) was mounted on the RTG4 DevKit in place of the REFCLK 125 MHz (disabled and isolated) for testing.

JITTER MEASUREMENTS

Within each transmitter of the SerDes, the time base provided by the reference clock to the TXPLL directly affects the quality of the SerDes serial output data. The jitter and phase variations present on the reference clock the TXPLL receives will also appear on the high-speed serial data stream it produces. The following data represents the jitter content of the high-speed serial data from the SerDes using the various reference clock schemes. The data below shows the quality of a 3.125 Gbps PRBS7 data stream transmitted with the discussed reference clock solutions.

FIGURE 15: Jitter Data, LVDS to LVDS25_ODT, Direct Interface (Setup Figure 2).

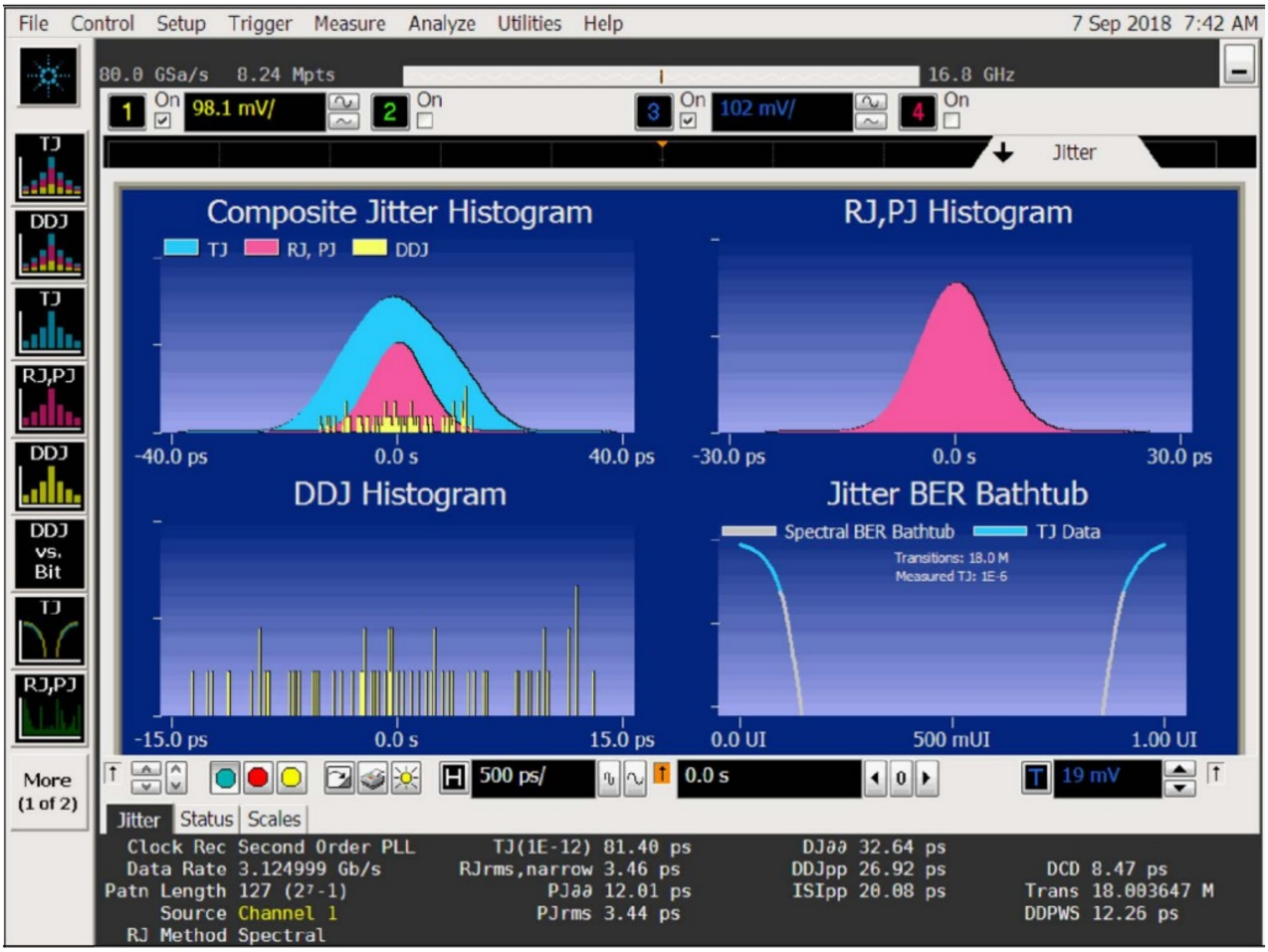


FIGURE 16: Eye Diagram, LVDS to LVDS25_ODT, Direct Interface (Setup Figure 2).

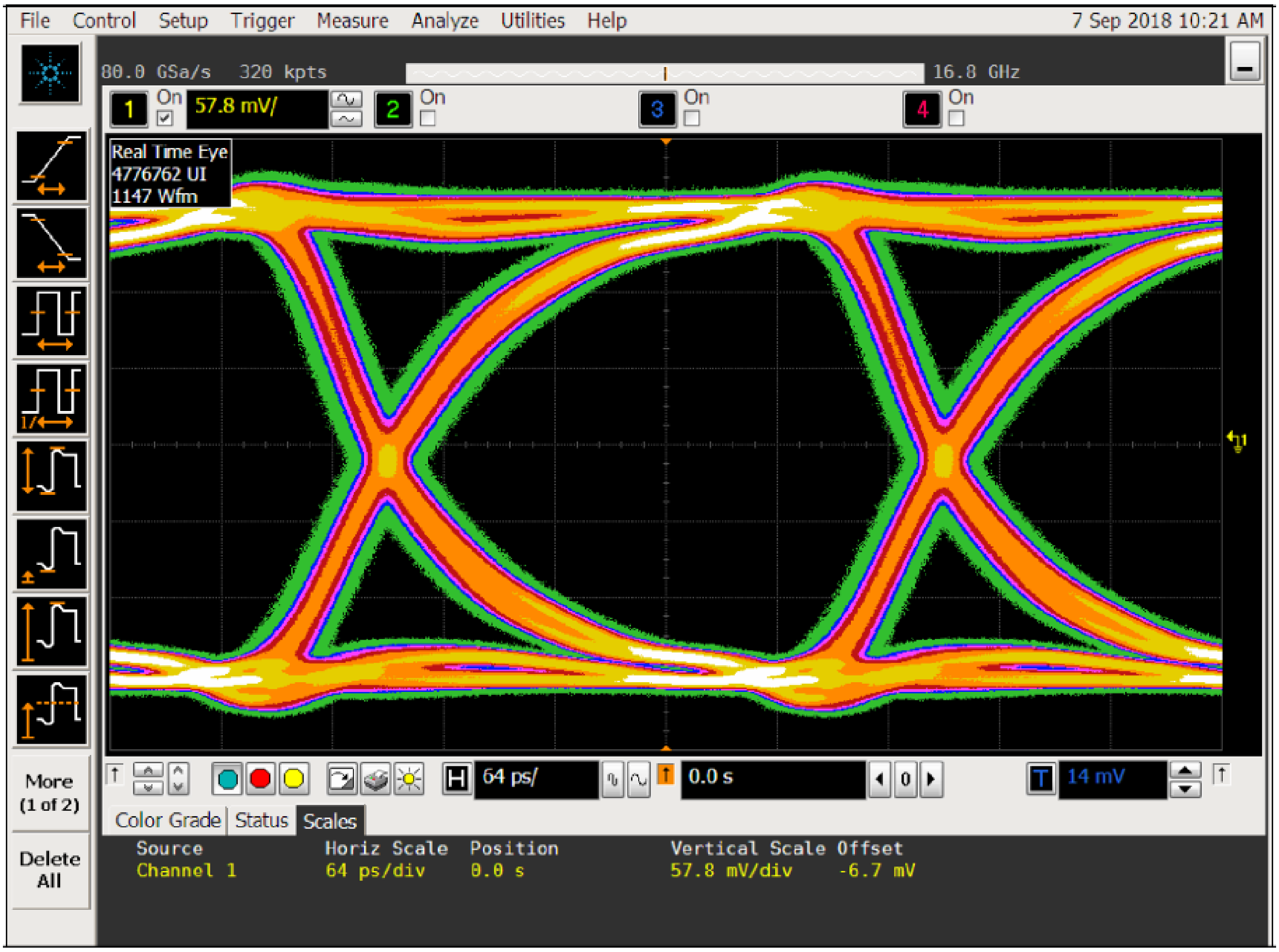


FIGURE 17: Jitter Data, LVDS to LVDS25 200Ω External Termination (Setup Figure 4).

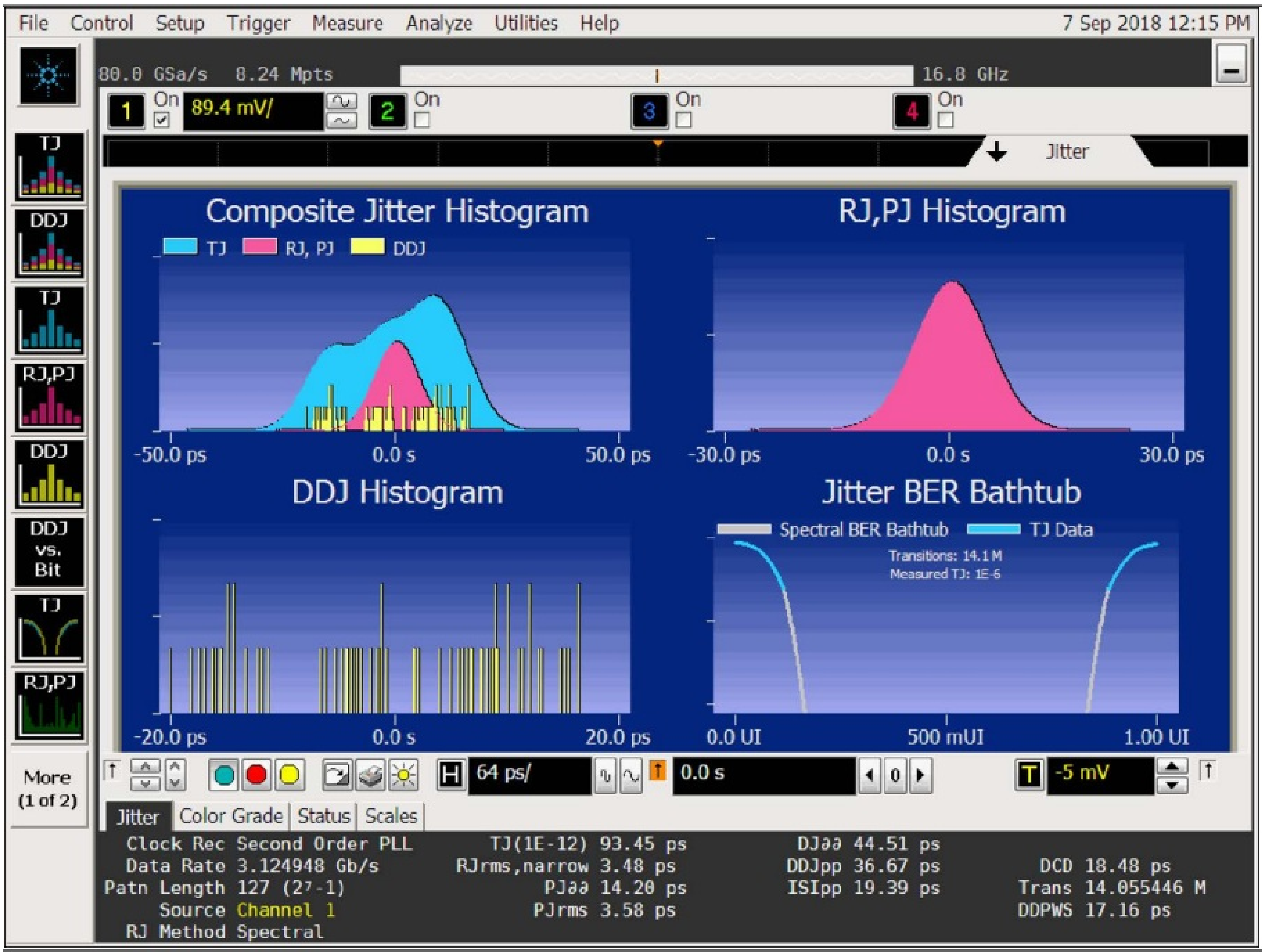


FIGURE 18: Eye Diagram, LVDS to LVDS25 200Ω External Termination (Setup Figure 4).

FIGURE 19: Jitter Data, LVPECL to LVDS25_ODT (Setup Figure 9).

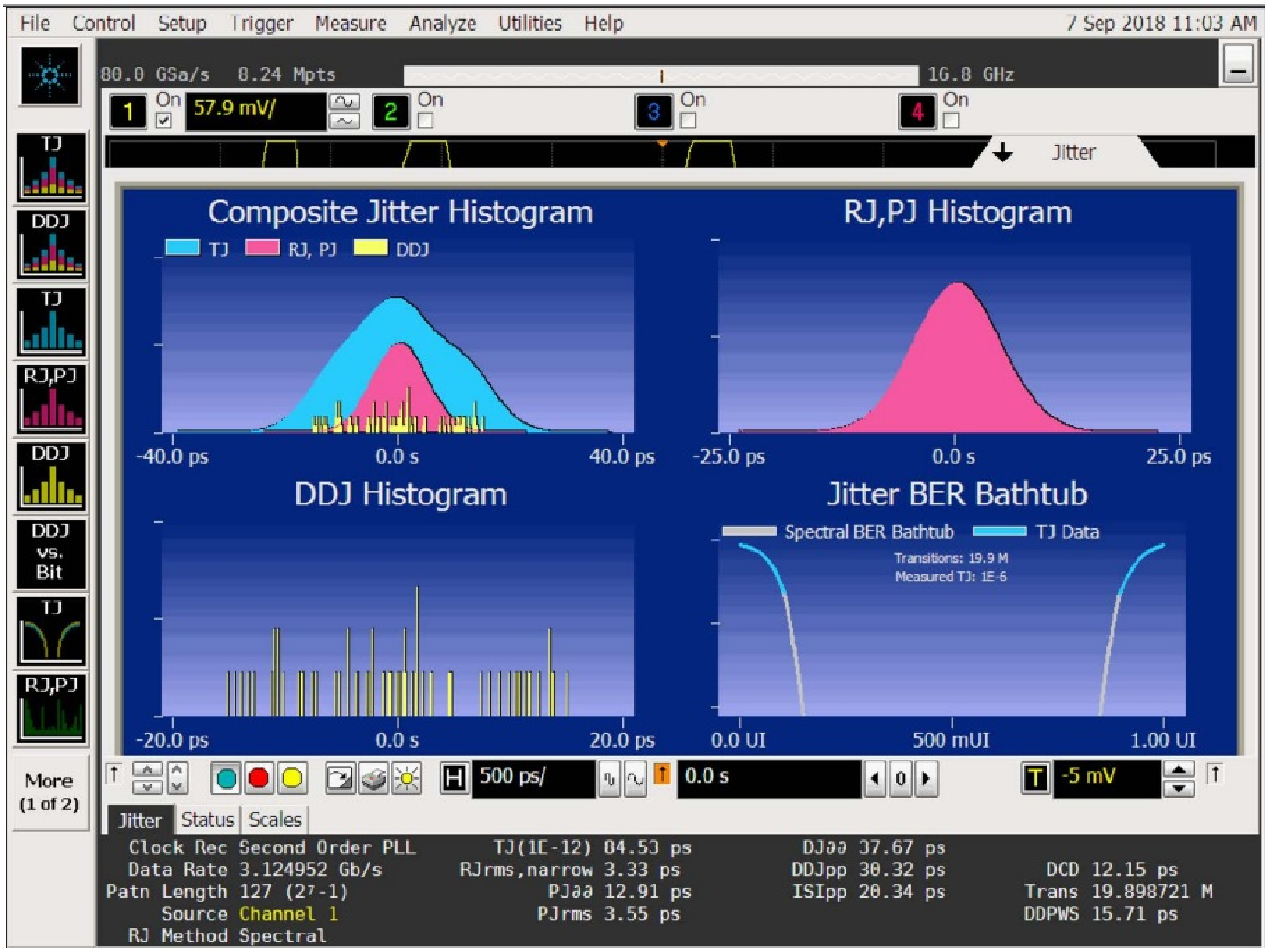
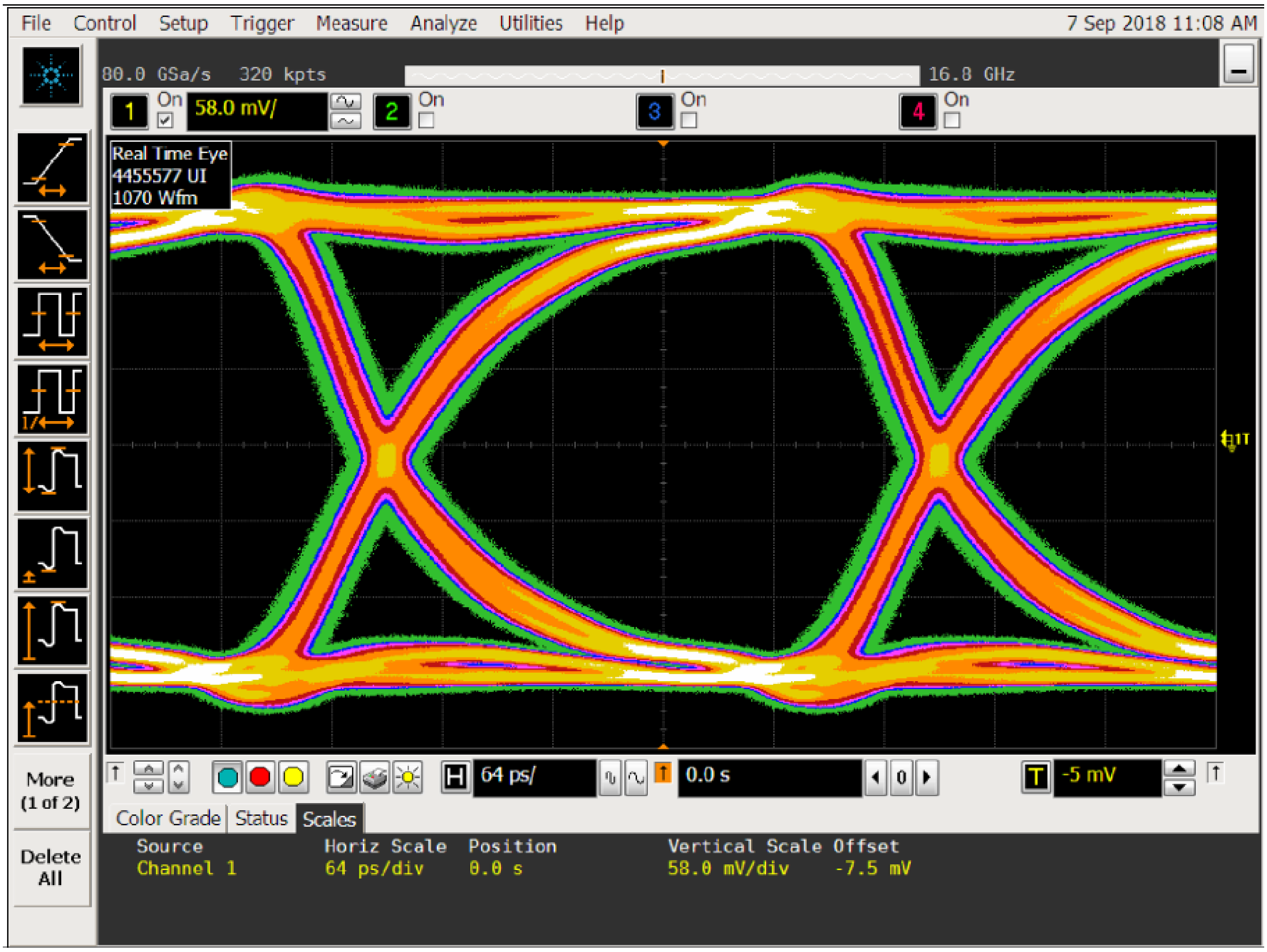


FIGURE 20: Eye Diagram, LVPECL to LVDS25_ODT (Setup Figure 9).



The following tables present the study done by the Microsemi characterization team, comparing SerDes transmit jitter to different RefClk types.

TABLE 7: JITTER DATA, RTG4 SERDES OUTPUT AT 3.125 GBPS FOR ALL REFCLK STANDARDS.

Device Number	Temp.	Voltage Condition	Parameter	LVDS 2.5V	LVCMOS 2.5V	LVCMOS 3.3V	SSTL 1.8V	SSTL 2.5V	HSTL 1.8V
	125 °C	Min.	Total Jitter (mUI)	318	309	306	481	371	445
			Deterministic Jitter (mUI)	257	266	265	438	328	403

902	25°C	Typ.	Total Jitter (mUI)	343	289	287	355	406	358
			Deterministic Jitter (mUI)	291	246	247	315	366	318
	–55 °C	Max.	Total Jitter (mUI)	257	263	273	340	458	316
			Deterministic Jitter (mUI)	221	222	232	304	414	275
905	125 °C	Min.	Total Jitter (mUI)	309	304	301	429	362	453
			Deterministic Jitter (mUI)	250	263	259	386	317	409
	25°C	Typ.	Total Jitter (mUI)	325	287	286	371	458	364
			Deterministic Jitter (mUI)	275	251	246	334	422	326
	–55 °C	Max.	Total Jitter (mUI)	336	265	277	307	423	320
			Deterministic Jitter (mUI)	297	226	237	270	381	278
	125 °C	Min.	Total Jitter (mUI)	350	320	294	402	435	435
			Deterministic Jitter (mUI)	286	276	250	357	391	390

911	25°C	Typ.	Total Jitter (mUI)	332	303	301	427	451	333
			Deterministic Jitter (mUI)	273	257	253	384	407	291
	–55 °C	Max.	Total Jitter (mUI)	320	277	264	312	385	331
			Deterministic Jitter (mUI)	278	239	223	271	342	293

TABLE 8: JITTER DATA, RTG4 SERDES OUTPUT AT 2.5 GBPS FOR ALL REFCLK STANDARDS.

Device Number	Temp.	Voltage Condition	Parameter	LVDS 2.5V	LVCMOS 2.5V	LVCMOS 3.3V	SSTL 1.8V	SSTL 2.5V	HSTL 1.8V
902	125 °C	Min.	Total Jitter (mUI)	202	164	168	188	188	224
			Deterministic Jitter (mUI)	164	135	129	157	159	216
	25°C	Typ.	Total Jitter (mUI)	200	143	146	181	214	241
			Deterministic Jitter (mUI)	170	117	120	151	185	213
	–55 °C	Max.	Total Jitter (mUI)	169	161	148	186	186	231

	°C		Deterministic Jitter (mUI)	136	135	122	159	159	168
905	125 °C	Min.	Total Jitter (mUI)	174	165	167	187	194	217
			Deterministic Jitter (mUI)	146	131	136	153	166	190
	25° C	Typ.	Total Jitter (mUI)	189	144	147	173	190	242
			Deterministic Jitter (mUI)	163	118	118	147	161	196
	–55 °C	Max.	Total Jitter (mUI)	157	152	146	190	187	229
			Deterministic Jitter (mUI)	130	127	120	161	158	156
911	125 °C	Min.	Total Jitter (mUI)	193	185	184	200	223	252
			Deterministic Jitter (mUI)	166	151	147	169	177	190
	25° C	Typ.	Total Jitter (mUI)	182	163	175	197	196	215
			Deterministic Jitter (mUI)	151	131	143	164	163	159
	–55 °C	Max.	Total Jitter (mUI)	159	145	150	208	199	182

			Deterministic Jitter (mUI)	134	119	118	166	169	155

TABLE 9: JITTER DATA, RTG4 SERDES OUTPUT AT 1.25 GBPS FOR ALL REFCLK STANDARDS.

Device Number	Temp.	Voltage Condition	Parameter	LVDS 2.5 V	LVCMOS 2.5V	LVCMOS 3.3V	SSTL 1.8 V	SSTL 2.5 V	HSTL 1.8 V
902	125 °C	Min.	Total Jitter (mUI)	92	106	99	134	95	114
			Deterministic Jitter (mUI)	73	85	80	114	66	91
	25° C	Typ.	Total Jitter (mUI)	100	99	99	88	99	108
			Deterministic Jitter (mUI)	16	77	76	68	76	79
	–55 °C	Max.	Total Jitter (mUI)	97	93	94	114	91	106
			Deterministic Jitter (mUI)	78	73	72	90	65	84
905	125 °C	Min.	Total Jitter (mUI)	100	100	106	97	122	130
			Deterministic Jitter (mUI)	76	74	87	69	90	101
	25° C	Typ.	Total Jitter (mUI)	90	97	104	103	103	99

			Deterministic Jitter (mUI)	66	70	83	79	80	77
	–55 °C	Max.	Total Jitter (mUI)	98	87	91	115	98	100
			Deterministic Jitter (mUI)	79	67	70	93	71	74
911	125 °C	Min.	Total Jitter (mUI)	82	108	117	137	730	155
			Deterministic Jitter (mUI)	65	79	97	105	101	107
	25° C	Typ.	Total Jitter (mUI)	115	115	776	108	110	146
			Deterministic Jitter (mUI)	90	83	85	72	82	116
	–55 °C	Max.	Total Jitter (mUI)	99	96	104	111	117	91
			Deterministic Jitter (mUI)	75	78	81	78	90	62

Hardware and Software Tools Used

The RTG4 Development Kit was used for testing the reference clocks and for waveform measurements. The RTG4 Development Kits on-board REFCLK CCLD-033-50-125.000 oscillator was disabled, isolated, and replaced with the Vectron clock driver LVPECL or LVDS along with the interface circuit for each testing of the clock types. Also, in-house test fixtures were developed for the specific tests of LVDS with a 200Ω load.

Microchip Software Libero SoC V11.9 was used to program the RTG4 Development Kits, loading project designs and setting the SerDes REFCLK Input receiver type for testing with the corresponding clock. Microchip EPCS Demo GUI was used to check the signal quality by testing the error-free data loop between the RTG4 transmitter and receiver of the SerDes block, and also to verify the clock circuit connections in the RTG4 development board.

Keysight ADS 2017 was used to generate circuit diagrams and for simulations when needed; IBIS models used in the simulations were Microsemi RTG4 REFCLK Receiver rt4g_msio.ibs, Michel Semiconductor ibisTop_100el16 in sc07p07el0160a, Aero flex/Chobham ut54lvds031lvucc.ibs, and Fairchild ACT3301 cgs3311m 3_3V.ibs.

REFERENCES, RELATED WEBSITES, AND DATA SHEETS

- Microchip Hi-Rel Clock Oscillator Landing Page: Space Oscillators
- Microchip RTG4 Radiation-Tolerant FPGAs: https://www.microsemi.com/product-directory/rad-tolerant-fpgas/3576-rtg4#documents
- Microchip DS0131 Data Sheet RTG4 FPGA: https://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet
- Microchip RTG4 Development Kits: https://www.microsemi.com/product-directory/dev-kits-solutions/3865-rtg4-kits
- Microchip DG0624 Demo Guide RTG4 FPGA SerDes EPCS Protocol Design: https://www.microsemi.com/document-portal/doc_download/135196-dg0624-rtg4-fpga-serdes-epcs-protocol-design-libero-soc-v11-9-sp1-demoguide
- Microchip UG0567, RTG4 FPGA High Speed Serial Interfaces User Guide: https://www.microsemi.com/document-portal/doc_download/134409-ug0567-rtg4-fpga-high-speed-serial-interfaces-user-guide
- Microchip SY100EL16V: https://www.microchip.com/wwwproducts/en/SY100EL16V
- Front grade Technologies, UT54LVDS031LV/E Quad Driver: https://www.frontgrade.com/sites/default/files/documents/Datasheet-UT54LVDS031LVE.pdf
- Keysight Technologies, Advanced Design Systems (ADS): https://www.keysight.com/en/pc-1297113/advanced-design-system-adscc=US&lc=eng

- TI SN54AC00-SP Radiation Hardened Quad 2 Input NAND Gate: http://www.ti.com/lit/ds/symlink/sn54ac00-sp.pdf

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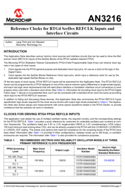	MICROCHIP RTG4 Radiation Tolerant Generation4 [pdf] Instruction Manual RTG4, RTG4 Radiation Tolerant Generation4, RTG4, Radiation Tolerant Generation4, Tolerant Generation4, Generation4

References

- User Manual

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