MICROCHIP RTG4 FPGAs Board Design and Layout Guidelines User Guide

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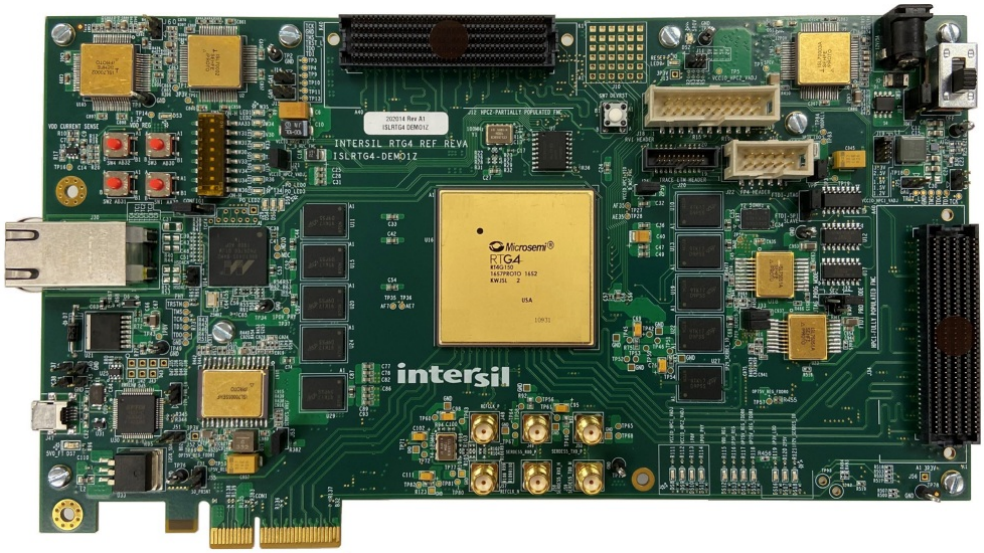

Contents

Introduction

This addendum to AC439: Board Design and Layout Guidelines for RTG4 FPGA Application Note, provides supplemental information, to emphasize that the DDR3 length matching guidelines published in revision 9 or later take precedence over the board layout used for the RTG4™ development kit. Initially, the RTG4 development kit was only available with Engineering Silicon (ES). After the initial release, the kit was later populated with standard (STD) speed grade and -1 speed grade RTG4 production devices. Part numbers, RTG4-DEV-KIT and RTG4-DEV-KIT-1 come with STD speed grade and -1 speed grade devices respectively.

Furthermore, this addendum includes details on the device I/O behavior for various power-up and power-down sequences, as well as, DEVRST_N assertion during normal operation.

Analysis of RTG4-DEV-KIT DDR3 Board Layout

RTG4 development kit implements a 32-bit data and 4-bit ECC DDR3 interface for each of the two built-in RTG4 FDDR controllers and PHY blocks (FDDR East and West). The interface is physically organized as five data byte lanes.

The kit follows the fly by routing scheme as described in the DDR3 Layout Guidelines section of AC439: Board Design and Layout Guidelines for RTG4 FPGA Application Note. However, since this development kit was designed before publishing the application note, it does not conform to the updated length matching guidelines described in the application note. In the DDR3 specification, there is a +/- 750 ps limit on the skew between data strobe (DQS) and DDR3 clock (CK) at each DDR3 memory device during a write transaction (tDQSS).

When the length matching guidelines in AC439 revision 9 or later versions of the application note are followed, the RTG4 board layout will meet the tDQSS limit for both -1 and STD speed grade devices across the entire process, voltage and temperature (PVT) operating range supported by RTG4 production devices. This is accomplished by factoring in the worst-case output skew between DQS and CK at the RTG4 pins. Specifically, when using the built-RTG4 FDDR controller plus PHY, the DQS leads CK by 370 ps maximum for a -1 speed grade device and DQS Leads CK by 447 ps maximum for a STD speed grade device, in worst-case conditions.

Based on the analysis shown in the Table 1-1, the RTG4-DEV-KIT-1 meets tDQSS limits at each memory device, at worst-case operating conditions for the RTG4 FDDR. However, as shown in the Table 1-2, the RTG4-DEV-KIT layout, populated with STD speed grade RTG4 devices, does not meet tDQSS for the fourth and fifth memory

devices in the fly-by topology, at worst-case operating conditions for the RTG4 FDDR. In general, the RTG4-DEV-KIT is used at typical conditions, such as room temperature in a lab environment. Therefore, this worst-case analysis is not applicable to the RTG4-DEV-KIT used in typical conditions. The analysis serves as an example of why it is important to follow the DDR3 length matching guidelines listed in AC439, so that a user board design meets tDQSS for a flight application.

To further elaborate on this example, and demonstrate how to manually compensate for a RTG4 board layout which cannot meet the AC439 DDR3 length matching guidelines, the RTG4-DEV-KIT with STD speed grade devices can still meet tDQSS at each memory device, at worst-case conditions, because the built-in RTG4 FDDR controller plus PHY has the ability to statically delay the DQS signal per data byte lane. This static shift can be used to reduce the skew between DQS and CK at a memory device which has a tDQSS > 750 ps. See the DRAM Training section, in UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide for more information about using the static delay controls (in register REG_PHY_WR_DQS_SLAVE_RATIO) for DQS during a write transaction. This delay value can be used in Libero® SoC when instantiating an FDDR controller with automatic initialization by modifying the auto-generated CoreABC FDDR initialization code. A similar process can be applied to a user board layout which does not meet tDQSS at each memory device.

Table 1-1. Evaluation of RTG4-DEV-KIT-1 tDQSS Calculation For -1 Parts and FDDR1 Interface

Path Analyzed	Clock Length (mils)	Clock Propagation Delay (ps)	Data Length (mils)	Data Propagation Delay (ps)	Difference between CLKDQS due to Routing (mils)	tDQSS at every memory, after board skew+FPGA DQSCLK skew (ps)
FPGA-1st Memory	2578	412.48	2196	351.36	61.12	431.12
FPGA-2nd Memory	3107	497.12	1936	309.76	187.36	557.36
FPGA-3rd Memory	3634	581.44	2231	356.96	224.48	594.48
FPGA-4th Memory	4163	666.08	2084	333.44	332.64	702.64
FPGA-5th Memory	4749	759.84	2848	455.68	304.16	674.16

Note: In worst case conditions, RTG4 FDDR DDR3 DQS-CLK skew for -1 devices is 370 ps maximum and 242 ps minimum.

Table 1-2. Evaluation of RTG4-DEV-KIT tDQSS Calculation for STD Parts and FDDR1 Interface

Path Analyzed	Clock Length (mils)	Clock Propagation Delay (ps)	Data Length (mils)	Data Propagation Delay (ps)	Difference between CLKDQS due to Routing (mils)	tDQSS at every memory, after board skew + FPGA DQS CLK skew (ps)
FPGA-1st Memory	2578	412.48	2196	351.36	61.12	508.12
FPGA-2nd Memory	3107	497.12	1936	309.76	187.36	634.36
FPGA-3rd Memory	3634	581.44	2231	356.96	224.48	671.48
FPGA-4th Memory	4163	666.08	2084	333.44	332.64	779.64
FPGA-5th Memory	4749	759.84	2848	455.68	304.16	751.16

Note: In worst case conditions, RTG4 FDDR DDR3 DQS-CLK skew for STD devices is 447 ps maximum and 302 ps minimum.

Note: Board propagation delay estimate of 160 ps/inch has been used in this analysis example for reference. The actual board propagation delay for a user board depends on the specific board being analyzed.

Power Sequencing

This addendum to AC439: Board Design and Layout Guidelines for RTG4 FPGA Application Note, provides supplemental information, to emphasize the criticality to follow the Board Design Guidelines. Ensure guidelines are followed with respect to Power-Up and Power-Down.

Power-Up

The following table lists the recommended power-up use cases and their corresponding power-up guidelines.

Table 2-1. Power-Up Guidelines

Use Case	Sequence Requirement	Behavior	Notes

DEVRST_N Asserted during power-up, until all RTG4 power supplies have reached recommended operating conditions	No specific ramp-up order required. Supply ramp-up must rise monotonically.	Once VDD and VPP reach activation thresholds (VDD ~= 0.55V, VPP ~= 2.2V) and DEVRST_N is released, the POR Delay Counter will run for ~40ms typical (50ms max), then device power-up to functional adheres to Figures 11 and 12 (DEVRST_N PUFT) of System Controller User's Guide (UG0576). In other words this sequence takes 40 ms + 1.72036 ms (typical) from the point DEVRST_N has been released. Note that subsequent use of DEVRST_N does not wait for the POR counter to perform power-up to functional tasks and thus this sequence takes only 1.72036 ms (typical).	By design, outputs will be disabled (i.e. float) during power- up. Once the POR counter has completed, DEVRST_N is released and all VDDI I/O supplies have reached their ~0.6V threshold, then the I/Os will be tristated with weak pull- up activated, until the outputs transition to user control, per Figures 11 and 12 of UG0576. Critical outputs which must remain low during power-up require an external 1K-ohm pull- down resistor.

DEVRST_N pulled-up to VPP and all supplies ramp up at approximately the same time	VDDPLL must not be the last power-supply to ramp up, and must reach the minimum recommended operating voltage before the last supply (VDD or VDDI) starts ramping up to prevent PLL lock output glitches. See the RTG4 Clocking Resources User Guide (UG0586) for an explanation of how to use the CCC/PLL READY_VDDPLL input to remove the sequencing requirements for the VDDPLL power supply. Either tie SERDES_x_Lyz_VDDAIO to the same supply as VDD, or ensure they power-up simultaneously.	Once VDD and VPP reach activation thresholds (VDD ~= 0.55V, VPP ~= 2.2V) the 50 ms POR delay counter will run. Device power-up to functional timing adheres to Figures 9 and 10 (VDD PUFT) of System Controller User's Guide (UG0576). In other words, total time is 57.95636 ms.	By design, outputs will be disabled (i.e. float) during power- up. Once the POR counter has completed, DEVRST_N is released and all VDDI IO supplies have reached their ~0.6V threshold, then the I/Os will be tristated with weak pull- up activated, until the outputs transition to user control, per Figures 9 and 10 of UG0576. Critical outputs which must remain low during power-up require an external 1K-ohm pull- down resistor.

VDD/ SERDES_VDDAIO -> VPP/VDDPLL ->	Sequence listed in Scenario Column. DEVRST_N is pulled-up to VPP.	Once VDD and VPP reach activation thresholds (VDD ~= 0.55V, VPP ~= 2.2V) the 50ms POR delay counter will run. Device power-up to functional timing adheres to Figures 9 and 10 (VDD PUFT) of System Controller User's Guide (UG0576). Completion of the device power-up sequence and power-up to functional timing is based upon the last VDDI supply that is powered on.	By design, outputs will be disabled (i.e. float) during power- up. Once the POR counter has completed, DEVRST_N is released and all VDDI I/O supplies have reached their ~0.6V threshold, then the IOs will be tristated with weak pull- up activated, until the outputs transition to user control, per Figures 9 and 10 of UG0576. No weak pull-up activation during power-up until all VDDI supplies reach ~0.6V. The key benefit of this sequence is that the last VDDI supply that reaches this activation threshold will not have the weak pull-up activated and will instead transition directly from disabled mode to user defined mode. This can help minimize the number of external 1K pull-down resistors required for designs which have the majority of I/O banks powered by the last VDDI to rise. For all other I/O banks powered by any VDDI supply other than the last VDDI supply to rise, the critical outputs which must remain low during power-up require an external 1K- ohm pull-down resistor.

Considerations during DEVRST_N Assertion and Power-Down

If AC439: Board Design and Layout Guidelines for RTG4 FPGA Application Note guidelines are not followed please review the following details:

1. For the given power-down sequences in Table 2-2, the user may see I/O glitches or inrush and transient current events.
2. As stated in the Customer Advisory Notification (CAN) 19002.5, deviation from the power-down sequence that is recommended in the RTG4 datasheet can trigger a transient current on the 1.2V VDD supply. If the 3.3V VPP supply is ramped down before the 1.2V VDD supply, a transient current on VDD will be observed as VPP and

DEVRST_N (powered by VPP) reach approximately 1.0V. This transient current does not occur if VPP is powered down last, per the datasheet recommendation. – The magnitude and duration of the transient current are dependent on the design programmed in the FPGA, specific board decoupling capacitance, and the transient response of the 1.2V voltage regulator. In rare cases, a transient current up to 25A (or 30 Watts on a nominal 1.2V VDD supply) has been observed. Due to the distributed nature of this VDD transient current across the entire FPGA fabric (not localized to a specific area), and its short duration, there is no reliability concern if the power-down transient is 25A or less. – As a best design practice, follow the datasheet recommendation to avoid transient current.

3. I/O glitches may be approximately 1.7V for 1.2 ms.
   – High glitch on outputs driving Low or Tristate may be observed.
   – Low glitch on outputs driving High may be observed (the low glitch cannot be mitigated by adding a 1 KΩ pull-down).
4. Powering down VDDIx first allows monotonic transition from High to Low, but output briefly drives low which would affect a user board which attempts to externally pull the output high when RTG4 VDDIx is powered down. RTG4 requires that I/O Pads not be externally driven above the VDDIx bank supply voltage hence if an external resistor is added to another power rail, it should power-down simultaneously with VDDIx supply.

Table 2-2. I/O Glitch Scenarios When Not Following Recommended Power-Down Sequence in AC439

Default Output State	**VDD (1.2 V)**	**VDDIx (<3.3V) VDDIx (3.3V)**	**VPP (3.3V)**	**DEVRST_N**	**Power Down Behavior**	
					I/O Glitch	**Current In-Rush**
I/O Driving Low or Tristated	Ramp down after VPP in any order		Ramp down first	Tied to VPP	Yes1	Yes
	Ramp down in any order after DEVRST_N assertion			Asserted before any supplies ramp down	Yes1	No
I/O Driving High	Ramp down after VPP in any order		Ramp down first	Tied to VPP	Yes	Yes
	Ramp down in any order before VPP		Ramp down last	Tied to VPP	No2	No
	Ramp down in any order after DEVRST_N assertion			Asserted before any supplies ramp down	Yes	No

(1) An external 1 KΩ pull-down resistor is recommended to mitigate the high glitch on critical I/Os, which must remain Low during power-down.
(2) A low glitch is only observed for an I/O that is externally pulled-up to a power supply which remains powered as VPP ramps down. However, this is a violation of device recommended operating conditions since the PAD must not be high after the corresponding VDDIx ramps down.

5. If DEVRST_N is asserted, the user may see a low glitch on any output I/O that is driving high and also externally pulled-up via a resistor to VDDI. For example, with a 1KΩ pull-up resistor, a low glitch reaching a minimum voltage of 0.4V with a duration of 200 ns may occur prior to the output being tristated.

Note: DEVRST_N must not be pulled above the VPP voltage. To avoid the above it is highly recommended to follow power-up and power-down sequences described in AC439: Board Design and Layout Guidelines for RTG4 FPGA Application Note.

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 3-1. Revision History

Revision	Date	Description
A	04/2022	• During DEVRST_N assertion, all RTG4 I/Os will be tristated. Outputs that are driven high by the FPGA fabric and externally pulled high on the board might experience a low glitch prior to entering the tristate condition. A board design with such an output scenario must be analyzed to understand the impact of interconnections to FPGA outputs that might glitch when DEVRST_N is asserted. For more information, see Step 5 in section 2.2. Considerations during DEVRST_N Assertion and Power-Down. • Renamed *Power-Down* to section 2.2. Considerations during DEVRST_N Assertion and Power-Down. • Converted to Microchip template.
2	02/2022	• Added the Power-Up section. • Added the Power Sequencing section.
1	07/2019	The first publication of this document.

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