MICROCHIP PWM v4.2 Three Phase Low Voltage Motor Control User Guide

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Contents

Introduction (Ask a Question)

The Three-phase Pulse Width Modulation (PWM) generates carrier-based, center-aligned PWM to trigger the switches of a three-phase inverter. The module also introduces a configurable dead time to avoid dead short circuits.
A delay time can be introduced to synchronize multiple three-phase PWM block instantiations for multi-axis or for harmonic cancellation in the case of multi-level inverters.

Summary (Ask a Question)

The following table provides a summary of the Three-phase PWM IP characteristics.

Core Version	This document applies to Three-phase PWM v4.2.
Supported Device Families	• PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v11.8 or later releases.
Licensing	Complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. Three-phase PWM is licensed with encrypted RTL that must be purchased separately. For more information, see **Three-phase PWM**.

Features (Ask a Question)

Three-phase PWM has the following key features:

- Generate three-phase pulse-width modulated signals based on three independent references
- Introduce a delay time to adjust the phase of PWM cycles between two three-phase PWM blocks
- Introduce a configurable dead time to avoid dead shorts in the inverter bridge
- Enable or disable signal to shut down the PWM output signals within one system clock cycle
- Generate timing pulses for other blocks, configurable as one or two pulses per period

Implementation of IP Core in Libero Design Suite (Ask a Question)

IP core must be installed to the IP Catalog of the Libero® SoC software. This is done automatically through the IP Catalog update function in the Libero SoC software, or the IP core can be manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, the core can be configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero project list.

Device Utilization and Performance (Ask a Question)

The following table lists the device utilization used for Three-phase PWM.

Table 1. Three-phase PWM Utilization

Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T	433	44	200	0	0	0	0
PolarFire	MPF300T	433	44	200	0	0	0	0
SmartFusion® 2	M2S150	433	44	200	0	0	0	0

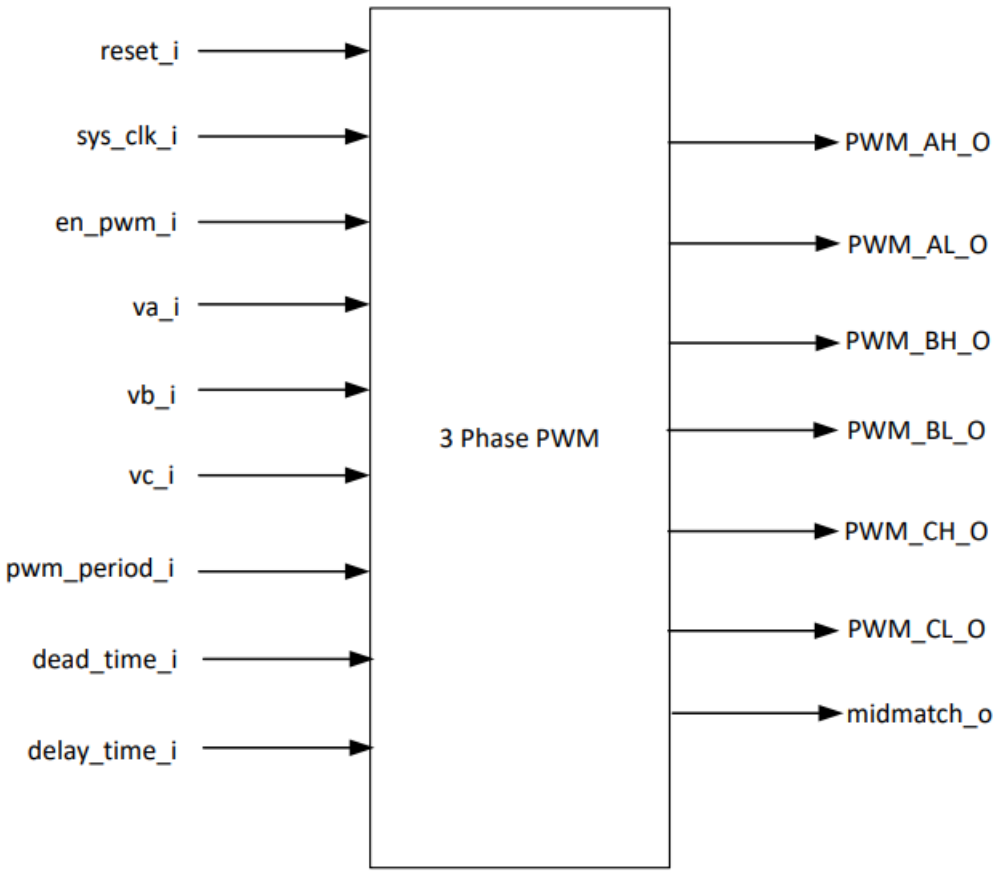
Important:

1. The data in this table is captured using typical synthesis and layout settings. CDR reference clock source was set to Dedicated with other configurator values unchanged.
2. Clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers.

Functional Description (Ask a Question)

This section describes the implementation details of the Three-phase PWM.
The following figure shows the system-level block diagram of the Three-phase PWM.

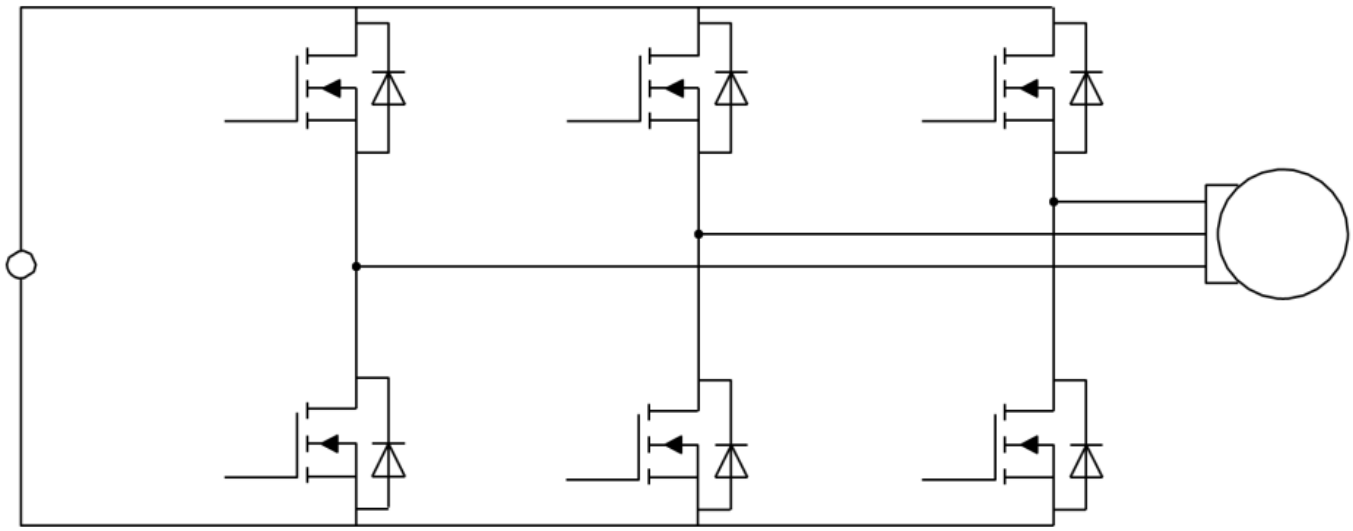
Figure 1-1. System-Level Block Diagram of Three-phase PWM



Theory of Operation (Ask a Question)

The three-phase inverter is the core of any AC motor drive. PWM pulses generated by the three-phase PWM drive the inverter bridge.
The following figure shows the inverter bridge.

Figure 1-2. Three-phase Inverter Bridge

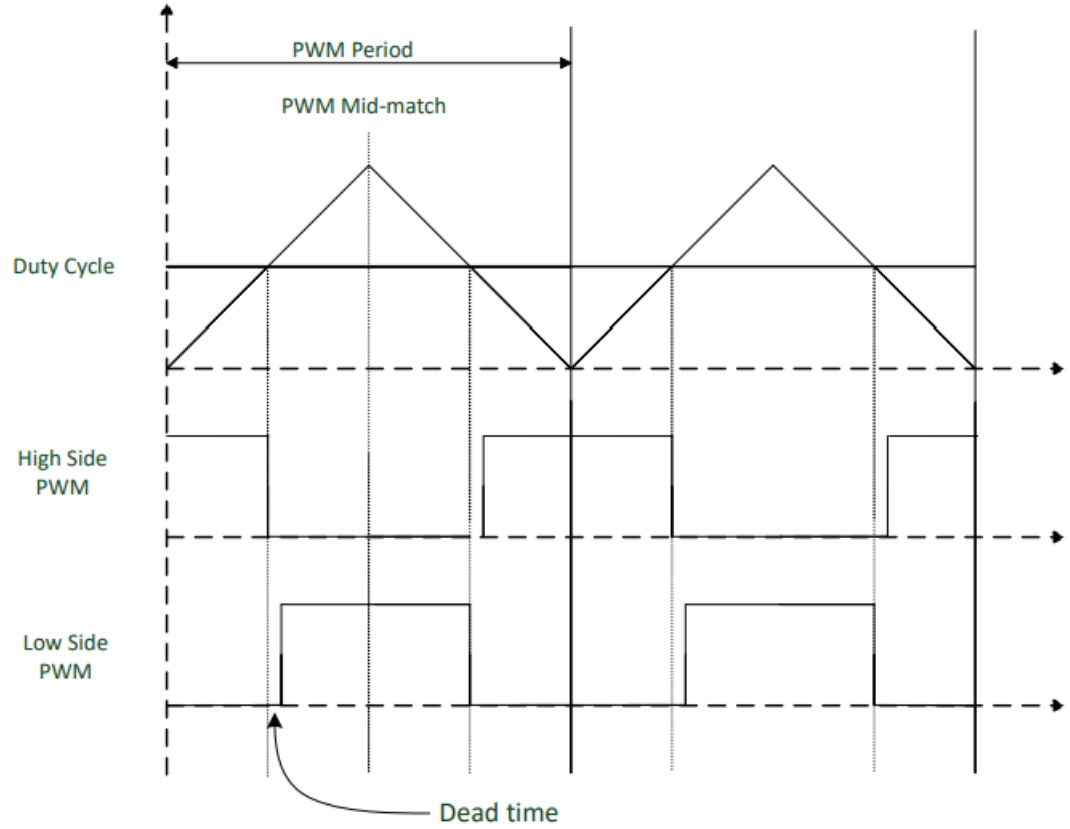


A three-phase two level inverter consists of three power electronic switches (Transistors), two in each leg for each phase of motor winding. The switches in each leg are driven by complementary pulses to switch the phase voltage between positive and negative DC voltage. The DC voltage passes through the transistor switches to the load when at least one of the three-phase pulses is active. Dead time is introduced between these high and low pulses of a phase or channel to allow the transistor to turn off completely, so that the DC source does not get shorted during operation

Generating Center Aligned PWM (Ask a Question)

In center aligned PWM, the PWM counter goes from a down-count to an up-count to down-count again, and so on. the following figure represents the operation of center aligned PWM. The PWM counter keeps running as long as the module is not in reset state, even when the PWM module is not enabled.

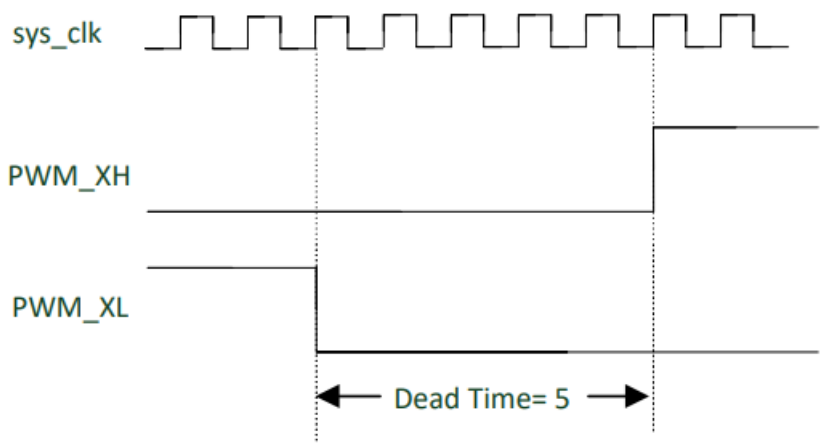
Figure 1-3. Center Aligned PWM



Dead Time and Delay Time (Ask a Question)

A time delay is introduced between turning off one of the transistors of a leg of an inverter to turning on the other transistor to ensure that a dead short circuit does not occur. This is called dead time.
The following figure shows the dead time insertion.

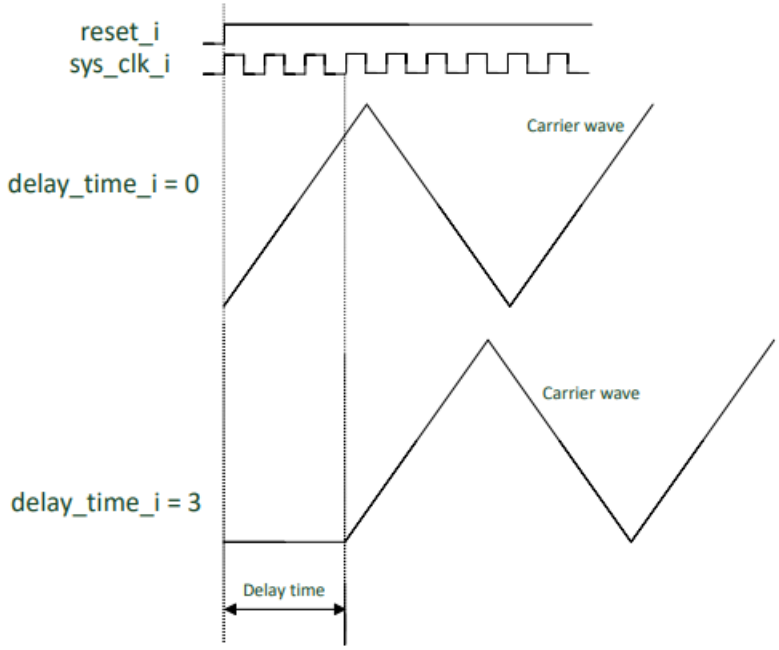
Figure 1-4. Dead Time Insertion



When multiple PWM blocks are present in a single system, some harmonics can be eliminated by phase shifting the PWM carrier wave. This time delay is referred to as delay time. This time delay is accounted for by the delay in generating carrier waves after reset.

The following figure shows how delay time is introduced.

Figure 1-5. Effect of Delay Time



Three-phase PWM Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the Three-phase PWM GUI configurator and I/O signals.

Inputs and Outputs Signals (Ask a Question)

The following table lists the input and output ports of Three-phase PWM.

Table 2-1. Inputs and Outputs of Three-phase PWM

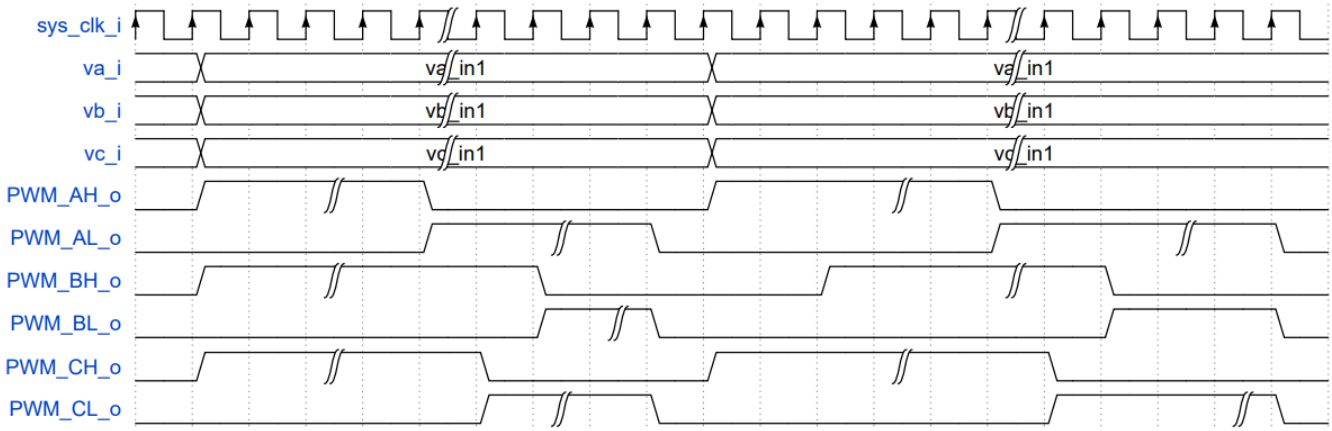
Signal Name	Direction	Description
reset_i	Input	Asynchronous active low reset signal
sys_clk_i	Input	System Clock
en_pwm_i	Input	Asynchronous enables: When set to 0, PWM outputs are driven to 0 When set to 1, PWM outputs are generated.
en_dual_trig_i	Input	When set to 1, PWM produces two trigger pulses distributed evenly per cycle at the midmatch_o output. When set to 0, PWM produces one trigger pulse per cycle at the midmatch_o output.
va_i	Input	Phase A duty cycle with respect to pwm_period
vb_i	Input	Phase B duty cycle with respect to pwm_period
vc_i	Input	Phase C duty cycle with respect to pwm_period
pwm_period_i	Input	Time period of PWM in number of system clock time
dead_time_i	Input	Dead time
delay_time_i	Input	Delay time
midmatch_o	Output	Period mid-match interrupt produces two pulses per PWM cycle when en_dual_trig_i input is 1, and produces one pulse per PWM cycle when en_dual_trig_i input is 0.
PWM_AH_O	Output	Channel A PWM for high side switch
PWM_AL_O	Output	Channel A PWM for low side switch
PWM_BH_O	Output	Channel B PWM for high side switch
PWM_BL_O	Output	Channel B PWM for low side switch
PWM_CH_O	Output	Channel C PWM for high side switch
PWM_CL_O	Output	Channel C PWM for low side switch

Timing Diagrams (Ask a Question)

This section discusses Three-phase PWM timing diagram.

The following figure shows the timing diagram of Three-phase PWM.

Figure 3-1. Three-phase PWM Timing Diagram



Testbench (Ask a Question)

A unified testbench is used to verify and test Three-phase PWM called as user testbench. Testbench is provided to
check the functionality of the Three-phase PWM IP.

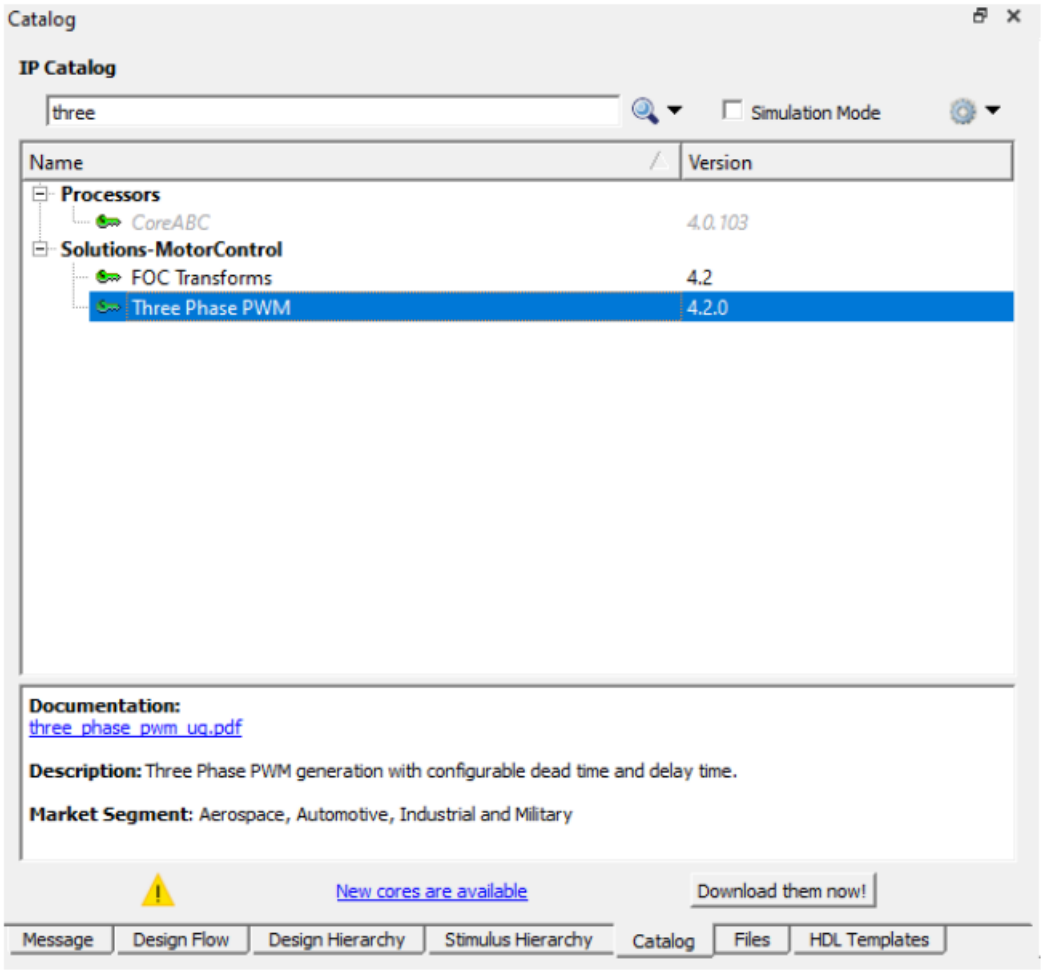
Simulation (Ask a Question)

The following steps describe how to simulate the core using the testbench:

1. Open Libero SoC, click **Catalog** tab, and then click **Solutions-MotorControl.**
2. Double-click **Three-phase PWM** and then click **OK.** The documentation associated with the IP are listed under **Documentation.**

   Important: If you do not see the **Catalog** tab, click **View,** open **Windows** menu, and then click Catalog to make it visible.

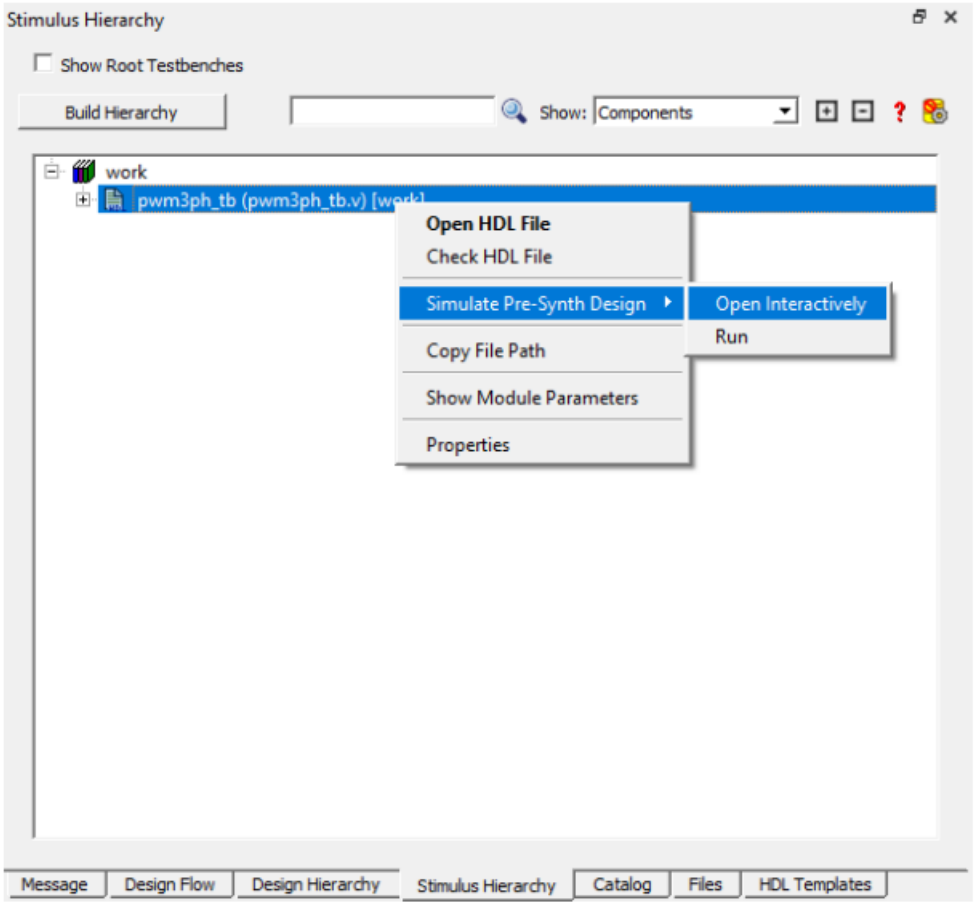
   Figure 4-1. Three-phase PWM IP Core in Libero SoC Catalog



3. On the **Stimulus Hierarchy** tab, click the testbench (three_phase_pwm_tb.v), point to **Simulate PreSynth Design,** and then click **Open Interactively.**

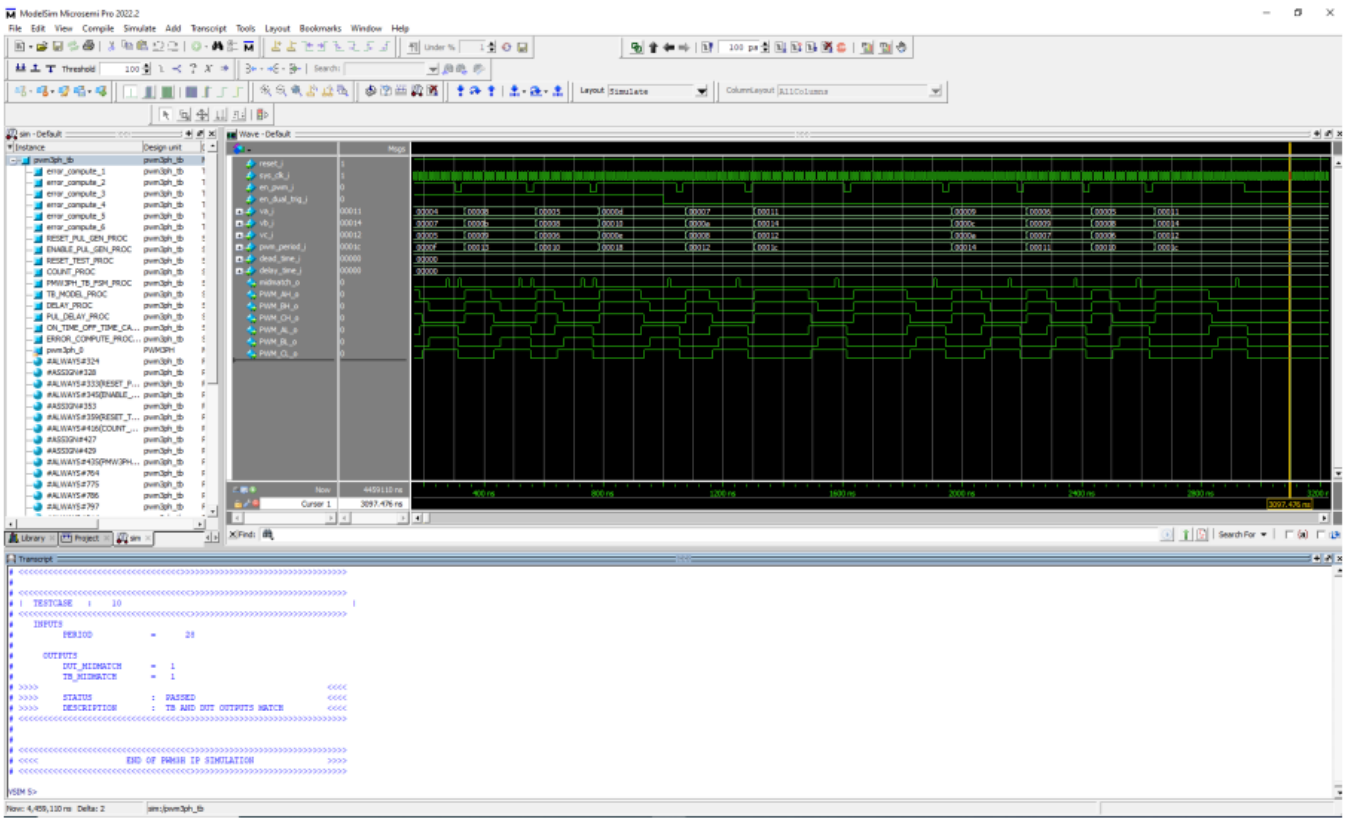
Important: If you do not see the **Stimulus Hierarchy** tab, click **View,** open **Windows** menu, and then click **Stimulus Hierarchy** to make it visible.

Figure 4-2. Simulating Pre-Synthesis Design



ModelSim opens with the testbench file, as shown in the following figure.

Figure 4-3. ModelSim Simulation Window



Important: If the simulation is interrupted due to the runtime limit specified in the .do file, use the run -all

command to complete the simulation.

Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	03/2023	The following are the list of changes in revision A of the document: • Migrated the document to the Microchip template. • Updated the document number to DS00004917A from 50200362. • Added 3. Timing Diagrams. • Added 4. Testbench.
6.0	—	The following is a summary of the changes in revision 6.0 of this document. • The Key Features and Supported Families sections were added to the Overview chapter . • The Inverter Bridge for AC Motors section was renamed Theory of Operation in the Over view chapter.
5.0	—	The following is a summary of the changes in revision 5.0 of this document. • A new pin is added in the block diagram of three-phase PWM. • Added the en_dual_trig_i entry in the input and output ports of three-phase PWM table. • Deleted the Configuration Parameters section from the Hardware Implementation chapter. • Updated Resource Utilization Report of Three-phase PWM values in the table.
4.0	—	Updated and merged the user guide
3.0	—	The following is a summary of the changes in revision 3.0 of this document. • Updated the Inputs and Outputs of Three-phase PWM table.
2.0	—	The following is a summary of the changes in revision 2.0 of this document. • Updated the title of the user guide. • Updated the Inputs and Outputs of Three-phase PWM table.
1.0	—	Revision 1.0 was the first publication of this document.

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