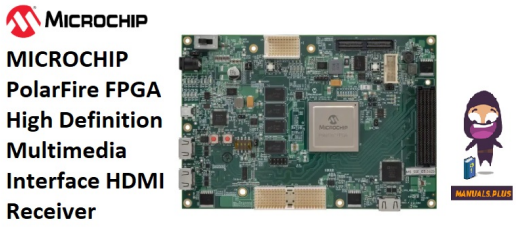

MICROCHIP PolarFire FPGA High Definition Multimedia Interface HDMI Receiver User Guide

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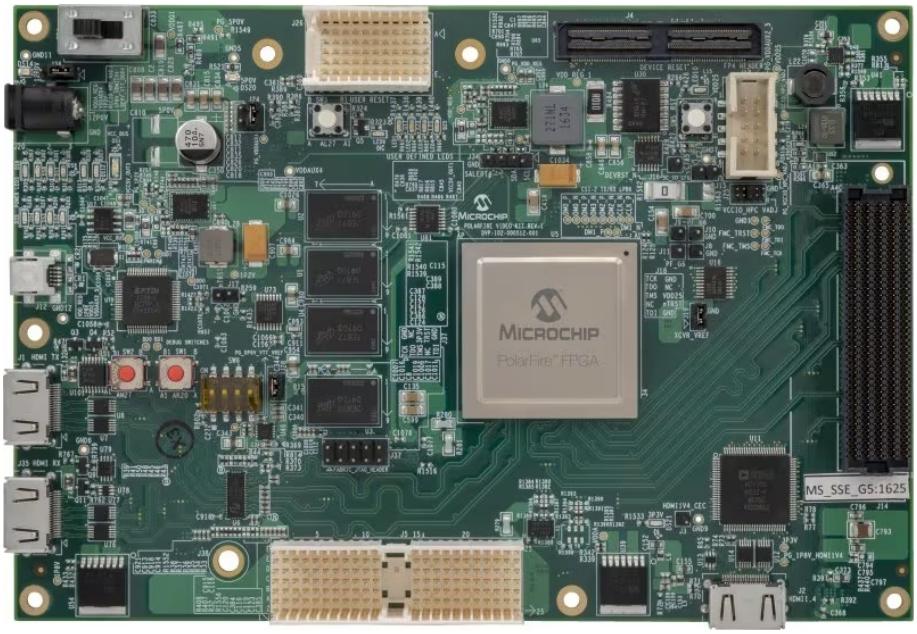


Introduction (Ask a Question)
Microchip's High-Definition Multimedia Interface (HDMI) receiver IP supports video data and audio packet data reception described in the HDMI standard specification. HDMI RX IP is specifically designed for PolarFire® FPGA and PolarFire System on Chip (SoC) FPGA devices supporting HDMI 2.0 for resolutions up to 1920 × 1080 at 60 Hz in one pixel mode and up to 3840 × 2160 at 60 Hz in four pixel mode. RX IP supports Hot Plug Detect (HPD) for monitoring power on or off and unplug or plug events to indicate communication between HDMI source and HDMI sink.

The HDMI source uses the Display Data channel (DDC) to read the sink's Extended Display Identification Data (EDID) to discover the Sink's configuration and/or capabilities. The HDMI RX IP has pre-programmed EDID, which an HDMI source can read through a standard I2C channel. PolarFire FPGA and PolarFire SoC FPGA device transceivers are used along with RX IP to deserialize serial data into 10-bit data. The data channels in HDMI are allowed to have a considerable skew between them. The HDMI RX IP removes the skew among the data channels using First-In First-Out (FIFOs). This IP converts the Transition Minimized Differential Signaling (TMDS) data received from the HDMI source through transceiver into 24-bit RGB pixel data, 24-bit audio data and control signals. The four standard control tokens specified in HDMI protocol are used to phase align the data during deserialization.

Summary

The following table provides a summary of the HDMI RX IP characteristics.

Table 1. HDMI RX IP Characteristics

Core Version	This user guide supports HDMI RX IP v5.4.
Supported Device Families	• PolarFire® SoC • PolarFire
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Supported Interfaces	Interfaces supported by the HDMI RX IP are: • AXI4-Stream: This core supports AXI4-Stream to the output ports. When configured in this mode, IP outputs AXI4 Stream standard complaint signals. • Native: When configured in this mode, IP outputs native video and audio signals.
Licensing	HDMI RX IP is provided with the following two license options: • Encrypted: Complete encrypted RTL code is provided for the core. It is available for free with any of the Libero license, enabling the core to be instantiated with SmartDesign. You can perform Simulation, Synthesis, Layout and program the FPGA silicon using the Libero design suite. • RTL: Complete RTL source code is license locked, which needs to be purchased separately.

Features

HDMI RX IP has the following features:

- Compatible for HDMI 2.0
- Supports 8, 10, 12 and 16 Bits Color Depth
- Supports Color Formats like RGB, YUV 4:2:2 and YUV 4:4:4
- Supports One or Four Pixels Per Clock Input
- Supports Resolutions up to 1920 × 1080 at 60 Hz in One Pixel mode and upto 3840 × 2160 at 60 Hz in Four Pixel mode.
- Detects Hot-Plug
- Supports Decoding Scheme – TMDS
- Supports DVI Input
- Supports Display Data Channel (DDC) and Enhanced Display Data Channel (E-DDC)
- Supports Native and AXI4 Stream Video Interface for Video Data Transfer
- Supports Native and AXI4 Stream Audio Interface for Audio Data Transfer

Unsupported Features

Following are the unsupported features of HDMI RX IP:

- 4:2:0 color format is not supported.
- High Dynamic Range (HDR) and High-bandwidth Digital Content Protection (HDCP) are not supported.

- Variable Refresh Rate (VRR) and Auto Low Latency Mode (ALLM) are not supported.
- Horizontal Timing parameters which are not divisible by four in Four Pixel mode are not supported.

Installation Instructions
The IP core must be installed to the IP Catalog of Libero® SoC software automatically through the IP Catalog update function in Libero SoC software, or it is manually downloaded from the catalog. Once the IP core is installed in Libero SoC software IP Catalog, it is configured, generated and instantiated within Smart Design for inclusion in the Libero project.

Tested Source Devices (Ask a Question)

The following table lists the tested source devices.

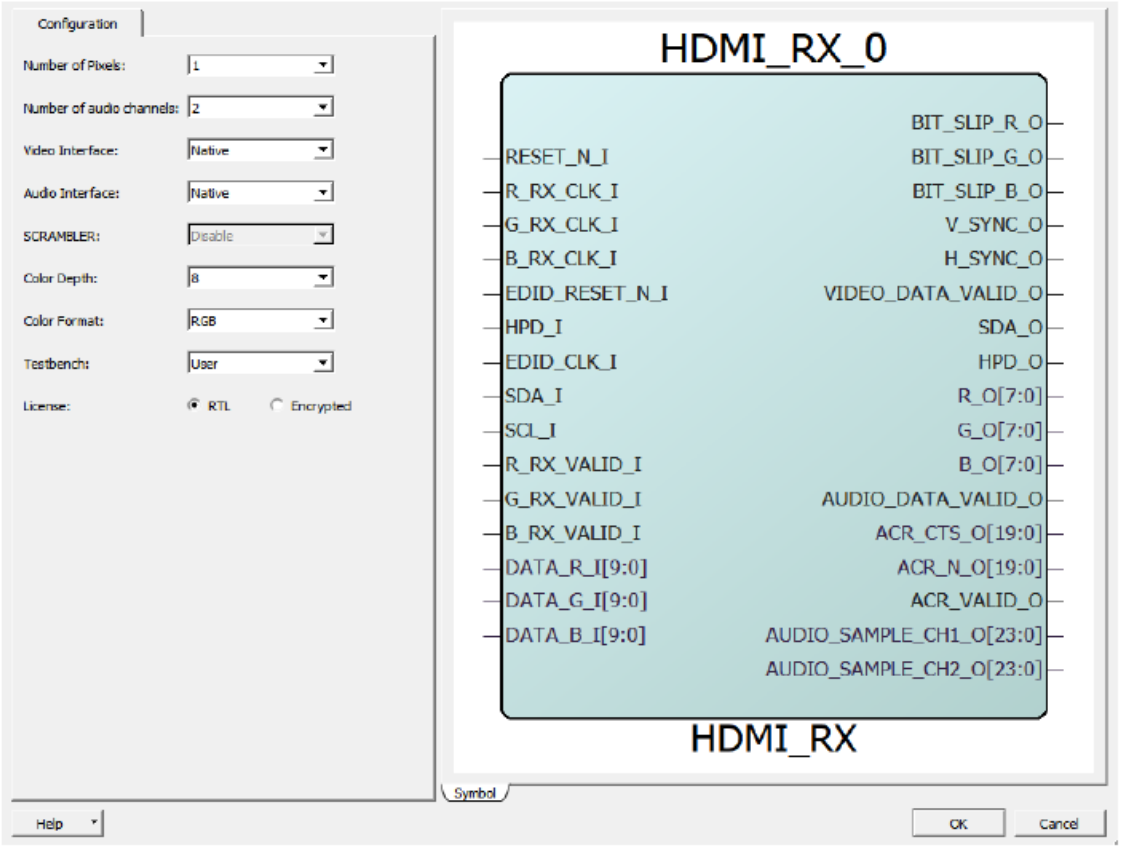
Table 1-1. Tested Sources Devices

Devices	Pixel Mode	Resolutions Tested	Color Depth (Bit)	Color Mode	Audio
quantumdata™ M41h HDMI Analyzer	1	720P 30 FPS, 720P 60 FPS and1080P 60 FPS	8	RGB, YUV444 and YUV422	Yes
		1080P 30 FPS	8, 10, 12 and 16		
	4	720P 30 FPS, 1080P 30 FPS and4K 60 FPS	8		
		1080P 60 FPS	8, 12 and 16		
		4K 30 FPS	8, 10, 12 and 16		
Lenovo™ 20U1A007IG	1	1080P 60 FPS	8	RGB	Yes
	4	1080P 60 FPS and 4K 30 FPS			
Dell Latitude 3420	1	1080P 60 FPS	8	RGB	Yes
	4	4K 30 FPS and 4K 60 FPS			
Astro VA-1844A HDMI® Tester	1	720P 30 FPS, 720P 60 FPS and1080P 60 FPS	8	RGB, YUV444 and YUV422	Yes
		1080P 30 FPS	8, 10, 12 and 16		
	4	720P 30 FPS, 1080P 30 FPS and4K 30 FPS	8		
		1080P 30 FPS	8, 12 and 16		
NVIDIA® Jetson AGX Orin 32 GB H01 Kit	1	1080P 30 FPS	8	RGB	No
	4	4K 60 FPS			

HDMI RX IP Configuration (Ask a Question)

This section provides an overview of the HDMI RX IP Configurator interface and its components. The HDMI RX IP Configurator provides a graphical interface to set up the HDMI RX core. This configurator allows the user to select parameters such as Number of Pixels, Number of audio channels, Video Interface, Audio Interface, SCRAMBLER, Color Depth, Color Format, Testbench and License. The Configurator interface includes dropdown menus and options to customize the settings. The key configurations are described in Table 4-1. The following figure provides a detailed view of the HDMI RX IP Configurator interface.

Figure 2-1. HDMI RX IP Configurator



The interface also includes OK and Cancel buttons to confirm or discard the configurations.

Hardware Implementation (Ask a Question)

The following figures describe the HDMI RX IP interface with transceiver (XCVR).

Figure 3-1. HDMI RX Block Diagram

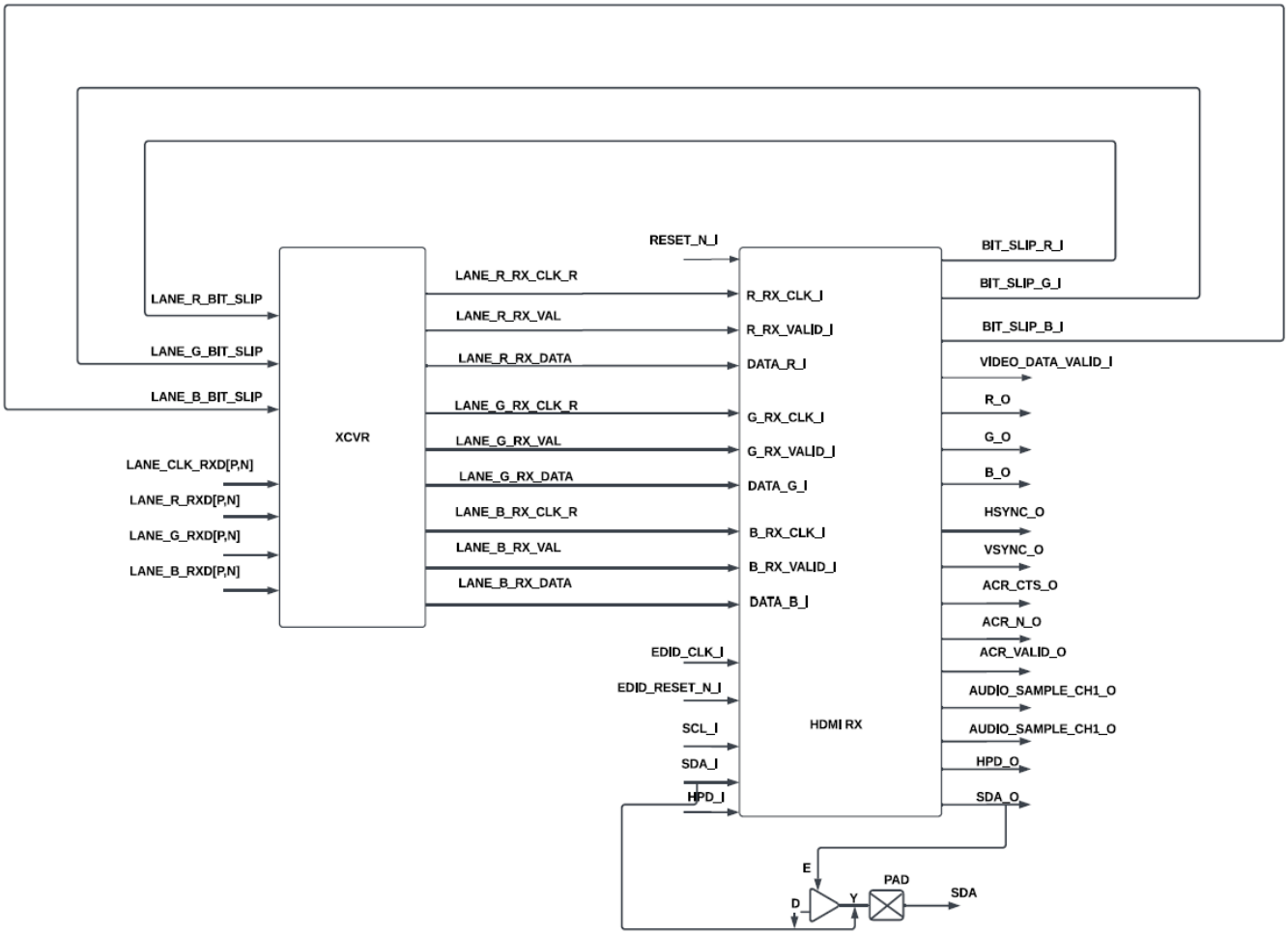
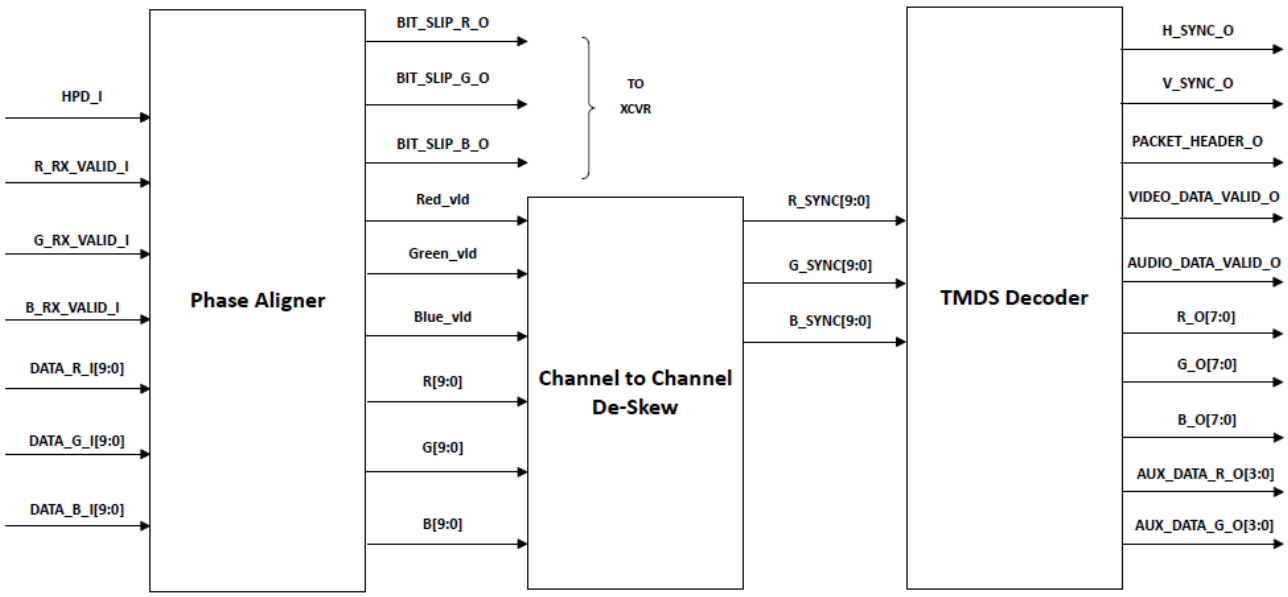


Figure 3-2. Receiver Detailed Block Diagram



HDMI RX consists of three stages:

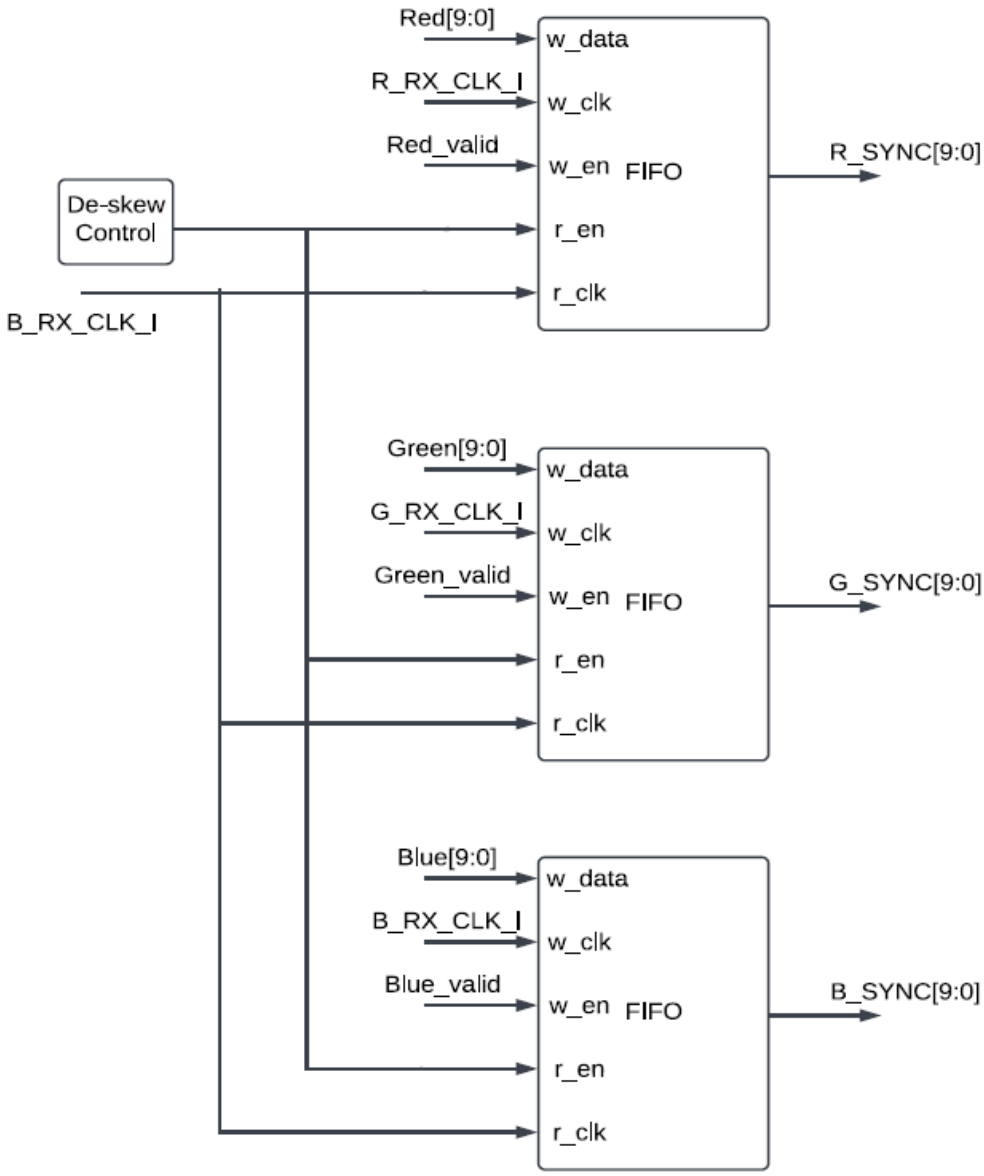
- The phase aligner aligns the parallel data with respect to control token boundaries using transceiver bit slip.
- The TMDS decoder converts the 10-bit encoded data into 8-bit video pixel data, 4-bit audio packet data and 2-bit control signals.
- The FIFOs remove the skew between the clocks of R, G and B lanes.

Phase Aligner (Ask a Question)
The 10-bit parallel data from the XCVR is not always aligned with respect to the TMDS encoded word boundaries. The parallel data needs to be bit shifted and aligned in order to decode the data. Phase aligner aligns the incoming parallel data to word boundaries using the bit-slip feature in the XCVR. XCVR in the Per-Monitor DPI Awareness (PMA) mode allows bit-slip feature, where it adjusts the alignment of the 10-bit deserialized word by 1-bit. Each time, after adjusting the 10-bit word by 1 bit slip position, it is compared with any one of the four control tokens of the HDMI protocol to lock the position during control period. The 10-bit word is correctly aligned and considered valid for the next stages. Each color channel has its own phase aligner, the TMDS decoder starts decoding only when all the phase aligners are locked to correct the word boundaries.

TMDS Decoder (Ask a Question)
TMDS decoder decodes the 10-bit deserialized from the transceiver into 8-bit pixel data during video period. HSYNC, VSYNC and PACKET HEADER are generated during the control period from the 10-bit blue channel data. The audio packet data is decoded on to the R and G channel each with four bits. The TMDS decoder of each channel operates on its own clock. Hence, it can have a certain skew between the channels.

Channel to Channel De-Skew (Ask a Question)
A FIFO based de-skew logic is used to remove the skew between the channels. Each channel receives a valid signal from the phase alignment units to indicate if the incoming 10-bit data from phase aligner are valid. If all channels are valid (have achieved phase alignment), FIFO module starts passing data through FIFO module using read and write enable signals (continuously writing in and reading out). When a control token is detected in any of the FIFO outputs, the read out flow is suspended, and a marker detected signal is generated to indicate the arrival of a particular marker in the video stream. The read out flow resumes only when this marker has arrived on all the three channels. As a result, the relevant skew is removed. The dual-clock FIFOs synchronize all three data streams to the blue channel clock to remove the relevant skew. The following figure describes the channel to channel de-skew technique.

Figure 3-3. Channel to Channel De-Skew



DDC (Ask a Question)

The DDC is a communication channel based on the I2C bus specification. The source uses I2C commands to read information from a sink's E-EDID with a slave address. The HDMI RX IP uses predefined EDID with multiple resolution supports resolutions up to 1920 × 1080 at 60 Hz in One Pixel mode and up to 3840 × 2160 at 60 Hz in Four Pixel mode.

The EDID represents the display name as Microchip HDMI display.

HDMI RX Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the HDMI RX GUI configurator and I/O signals.

Configuration Parameters (Ask a Question)

The following table lists the configuration parameters in the HDMI RX IP.

Table 4-1. Configuration Parameters

Parameter Name	Description
Color Format	Defines the color space. Supports the following color formats: • RGB • YCbCr422 • YCbCr444
Color Depth	Specifies the number of bits per color component. Supports 8, 10, 12 and 16 bits per component.
Number of Pixels	Indicates the number of pixels per clock input: • Pixel per clock = 1 • Pixel per clock = 4
SCRAMBLER	Support for 4K resolution at 60 frames per second: • When 1, Scrambler support is enabled • When 0, Scrambler support is disabled
Number of audio channels	Supports number of audio channels: • 2 audio channels • 8 audio channels
Video Interface	Native and AXI stream
Audio Interface	Native and AXI stream
Test bench	Allows the selection of a test bench environment. Supports the following test bench options: • User • None
License	Specifies the type of license. Provides the following two license options: • RTL • Encrypted

Ports (Ask a Question)
The following table lists the input and output ports of the HDMI RX IP for Native interface when Color Format is RGB.

Table 4-2. Input and Output for Native Interface

Signal Name	Direction	Width (Bits)	Description
RESET_N_I	Input	1	Active-low asynchronous reset signal
R_RX_CLK_I	Input	1	Parallel clock for “R” channel from XCVR
G_RX_CLK_I	Input	1	Parallel clock for “G” channel from XCVR
B_RX_CLK_I	Input	1	Parallel clock for “B” channel from XCVR
EDID_RESET_N_I	Input	1	Active-low asynchronous edid reset signal
R_RX_VALID_I	Input	1	Valid signal from XCVR for “R” channel parallel data
G_RX_VALID_I	Input	1	Valid signal from XCVR for “G” channel parallel data
B_RX_VALID_I	Input	1	Valid signal from XCVR for “B” channel parallel data

Signal Name	Direction	Width (Bits)	Description
DATA_R_I	Input	NUMBER OF PIXELS × 10 bits	Received “R” channel parallel data from XCVR
DATA_G_I	Input	NUMBER OF PIXELS × 10 bits	Received “G” channel parallel data from XCVR
DATA_B_I	Input	NUMBER OF PIXELS × 10 bits	Received “B” channel parallel data from XCVR
SCL_I	Input	1	I2C serial clock input for DDC
HPD_I	Input	1	Hot plug detect input signal. Source is connected to sink HPD signal should be high.
SDA_I	Input	1	I2C serial data input for DDC
EDID_CLK_I	Input	1	System clock for I2C module
BIT_SLIP_R_O	Output	1	Bit slip signal to “R” channel of transceiver
BIT_SLIP_G_O	Output	1	Bit slip signal to “G” channel of transceiver
BIT_SLIP_B_O	Output	1	Bit slip signal to “B” channel of transceiver
VIDEO_DATA_VALID_O	Output	1	Video data valid output
AUDIO_DATA_VALID_O	Output	1	Audio data valid output
H_SYNC_O	Output	1	Horizontal sync pulse
V_SYNC_O	Output	1	Active vertical sync pulse

R_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “R” data
G_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “G” data
B_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “B” data
SDA_O	Output	1	I2C serial data output for DDC
HPD_O	Output	1	Hot plug detect output signal
ACR_CTS_O	Output	20	Audio Clock Regeneration Cycle Timestamp value
ACR_N_O	Output	20	Audio Clock Regeneration value (N) parameter
ACR_VALID_O	Output	1	Audio Clock Regeneration valid signal
AUDIO_SAMPLE_CH1_O	Output	24	Channel 1 audio sample data
AUDIO_SAMPLE_CH2_O	Output	24	Channel 2 audio sample data
AUDIO_SAMPLE_CH3_O	Output	24	Channel 3 audio sample data
AUDIO_SAMPLE_CH4_O	Output	24	Channel 4 audio sample data
AUDIO_SAMPLE_CH5_O	Output	24	Channel 5 audio sample data
AUDIO_SAMPLE_CH6_O	Output	24	Channel 6 audio sample data
AUDIO_SAMPLE_CH7_O	Output	24	Channel 7 audio sample data
AUDIO_SAMPLE_CH8_O	Output	24	Channel 8 audio sample data
HDMI_DVI_MODE_O	Output	1	The following are the two modes: • 1: HDMI mode • 0: DVI mode

The following table describes the input and output ports of HDMI RX IP for AXI4 Stream Video Interface.
Table 4-3. Input and Output Ports for AXI4 Stream Video Interface

Port Name	Direction	Width (Bits)	Description
TDATA_O	Output	NUMBER OF PIXELS × Color Depth × 3 bits	Output video data [R, G, B]
TVALID_O	Output	1	Output video valid

Port Name	Direction	Width (Bits)	Description
TLAST_O	Output	1	Output frame end signal
TUSER_O	Output	3	• bit 0 = VSYNC • bit 1 = Hsync • bit 2 = 0 • bit 3 = 0
TSTRB_O	Output	3	Output video data strobe
TKEEP_O	Output	3	Output video data keep

The following table describes the input and output ports of HDMI RX IP for AXI4 Stream Audio Interface.

Table 4-4. Input and Output Ports for AXI4 Stream Audio Interface

Port Name	Direction	Width (Bits)	Description
AUDIO_TDATA_O	Output	24	Output audio data
AUDIO_TID_O	Output	3	Output audio channel
AUDIO_TVALID_O	Output	1	Output audio valid signal

The following table lists the input and output ports of the HDMI RX IP for Native interface when Color Format is YUV444.

Table 4-5. Input and Output for Native Interface

Port Name	Direction	Width (Bits)	Description
RESET_N_I	Input	1	Active-low asynchronous reset signal
LANE3_RX_CLK_I	Input	1	Parallel clock for Lane 3 channel from XCVR
LANE2_RX_CLK_I	Input	1	Parallel clock for Lane 2 channel from XCVR
LANE1_RX_CLK_I	Input	1	Parallel clock for Lane 1 channel from XCVR
EDID_RESET_N_I	Input	1	Active-low asynchronous edid reset signal

LANE3_RX_VALID_I	Input	1	Valid signal from XCVR for Lane 3 parallel data
LANE2_RX_VALID_I	Input	1	Valid signal from XCVR for Lane 2 parallel data
LANE1_RX_VALID_I	Input	1	Valid signal from XCVR for Lane 1 parallel data
DATA_LANE3_I	Input	NUMBER OF PIXELS × 10 bits	Received Lane 3 parallel data from XCVR
DATA_LANE2_I	Input	NUMBER OF PIXELS × 10 bits	Received Lane 2 parallel data from XCVR
DATA_LANE1_I	Input	NUMBER OF PIXELS × 10 bits	Received Lane 1 parallel data from XCVR
SCL_I	Input	1	I2C serial clock input for DDC
HPD_I	Input	1	Hot plug detect input signal. Source is connected to sin k HPD signal should be high.
SDA_I	Input	1	I2C serial data input for DDC
EDID_CLK_I	Input	1	System clock for I2C module
BIT_SLIP_LANE3_O	Output	1	Bit slip signal to Lane 3 of transceiver
BIT_SLIP_LANE2_O	Output	1	Bit slip signal to Lane 2 of transceiver
BIT_SLIP_LANE1_O	Output	1	Bit slip signal to Lane 1 of transceiver
VIDEO_DATA_VALID_O	Output	1	Video data valid output
AUDIO_DATA_VALID_O	Output	1	Audio data valid output
H_SYNC_O	Output	1	Horizontal sync pulse
V_SYNC_O	Output	1	Active vertical sync pulse

Port Name	Direction	Width (Bits)	Description
Y_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “Y” data
Cb_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “Cb” data
Cr_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “Cr” data
SDA_O	Output	1	I2C serial data output for DDC
HPD_O	Output	1	Hot plug detect output signal
ACR_CTS_O	Output	20	Audio Clock Regeneration Cycle timestamp value
ACR_N_O	Output	20	Audio Clock Regeneration value (N) parameter
ACR_VALID_O	Output	1	Audio Clock Regeneration valid signal
AUDIO_SAMPLE_CH1_O	Output	24	Channel 1 audio sample data
AUDIO_SAMPLE_CH2_O	Output	24	Channel 2 audio sample data
AUDIO_SAMPLE_CH3_O	Output	24	Channel 3 audio sample data
AUDIO_SAMPLE_CH4_O	Output	24	Channel 4 audio sample data
AUDIO_SAMPLE_CH5_O	Output	24	Channel 5 audio sample data
AUDIO_SAMPLE_CH6_O	Output	24	Channel 6 audio sample data
AUDIO_SAMPLE_CH7_O	Output	24	Channel 7 audio sample data
AUDIO_SAMPLE_CH8_O	Output	24	Channel 8 audio sample data

The following table lists the input and output ports of the HDMI RX IP for Native interface when Color Format is YUV422.

Table 4-6. Input and Output for Native Interface

Port Name	Direction	Width (Bits)	Description
RESET_N_I	Input	1	Active-low asynchronous reset signal
LANE3_RX_CLK_I	Input	1	Parallel clock for Lane 3 channel from XCVR
LANE2_RX_CLK_I	Input	1	Parallel clock for Lane 2 channel from XCVR
LANE1_RX_CLK_I	Input	1	Parallel clock for Lane 1 channel from XCVR
EDID_RESET_N_I	Input	1	Active-low asynchronous edid reset signal
LANE3_RX_VALID_I	Input	1	Valid signal from XCVR for Lane 3 parallel data
LANE2_RX_VALID_I	Input	1	Valid signal from XCVR for Lane 2 parallel data
LANE1_RX_VALID_I	Input	1	Valid signal from XCVR for Lane 1 parallel data
DATA_LANE3_I	Input	NUMBER OF PIXELS × 10 bits	Received Lane 3 parallel data from XCVR
DATA_LANE2_I	Input	NUMBER OF PIXELS × 10 bits	Received Lane 2 parallel data from XCVR
DATA_LANE1_I	Input	NUMBER OF PIXELS × 10 bits	Received Lane 1 parallel data from XCVR
SCL_I	Input	1	I2C serial clock input for DDC
HPD_I	Input	1	Hot plug detect input signal. Source is connected to sink HPD signal should be high.
SDA_I	Input	1	I2C serial data input for DDC
EDID_CLK_I	Input	1	System clock for I2C module
BIT_SLIP_LANE3_O	Output	1	Bit slip signal to Lane 3 of transceiver
BIT_SLIP_LANE2_O	Output	1	Bit slip signal to Lane 2 of transceiver
BIT_SLIP_LANE1_O	Output	1	Bit slip signal to Lane 1 of transceiver
VIDEO_DATA_VALID_O	Output	1	Video data valid output

Port Name	Direction	Width (Bits)	Description
AUDIO_DATA_VALID_O	Output	1	Audio data valid output
H_SYNC_O	Output	1	Horizontal sync pulse
V_SYNC_O	Output	1	Active vertical sync pulse
Y_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “Y” data
C_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “C” data
SDA_O	Output	1	I2C serial data output for DDC
HPD_O	Output	1	Hot plug detect output signal
ACR_CTS_O	Output	20	Audio Clock Regeneration Cycle timestamp value
ACR_N_O	Output	20	Audio Clock Regeneration value (N) parameter
ACR_VALID_O	Output	1	Audio Clock Regeneration valid signal
AUDIO_SAMPLE_CH1_O	Output	24	Channel 1 audio sample data
AUDIO_SAMPLE_CH2_O	Output	24	Channel 2 audio sample data
AUDIO_SAMPLE_CH3_O	Output	24	Channel 3 audio sample data
AUDIO_SAMPLE_CH4_O	Output	24	Channel 4 audio sample data
AUDIO_SAMPLE_CH5_O	Output	24	Channel 5 audio sample data
AUDIO_SAMPLE_CH6_O	Output	24	Channel 6 audio sample data
AUDIO_SAMPLE_CH7_O	Output	24	Channel 7 audio sample data
AUDIO_SAMPLE_CH8_O	Output	24	Channel 8 audio sample data

The following table lists the input and output ports of the HDMI RX IP for Native interface when SCRAMBLER is Enabled.

Table 4-7. Input and Output for Native Interface

Port Name	Direction	Width (Bits)	Description
RESET_N_I	Input	1	Active-low asynchronous reset signal
R_RX_CLK_I	Input	1	Parallel clock for “R” channel from XCVR
G_RX_CLK_I	Input	1	Parallel clock for “G” channel from XCVR
B_RX_CLK_I	Input	1	Parallel clock for “B” channel from XCVR
EDID_RESET_N_I	Input	1	Active-low asynchronous edid reset signal
HDMI_CABLE_CLK_I	Input	1	Cable clock from the HDMI source
R_RX_VALID_I	Input	1	Valid signal from XCVR for “R” channel parallel data
G_RX_VALID_I	Input	1	Valid signal from XCVR for “G” channel parallel data
B_RX_VALID_I	Input	1	Valid signal from XCVR for “B” channel parallel data
DATA_R_I	Input	NUMBER OF PIXELS × 10 bits	Received “R” channel parallel data from XCVR
DATA_G_I	Input	NUMBER OF PIXELS × 10 bits	Received “G” channel parallel data from XCVR
DATA_B_I	Input	NUMBER OF PIXELS × 10 bits	Received “B” channel parallel data from XCVR
SCL_I	Input	1	I2C serial clock input for DDC
HPD_I	Input	1	Hot plug detect input signal. The source is connected to the sink, and the HPD signal should be high.
SDA_I	Input	1	I2C serial data input for DDC
EDID_CLK_I	Input	1	System clock for I2C module
BIT_SLIP_R_O	Output	1	Bit slip signal to “R” channel of transceiver
BIT_SLIP_G_O	Output	1	Bit slip signal to “G” channel of transceiver

Port Name	Direction	Width (Bits)	Description
BIT_SLIP_B_O	Output	1	Bit slip signal to “B” channel of transceiver
VIDEO_DATA_VALID_O	Output	1	Video data valid output
AUDIO_DATA_VALID_O	Output 1	1	Audio data valid output
H_SYNC_O	Output	1	Horizontal sync pulse
V_SYNC_O	Output	1	Active vertical sync pulse

DATA_ RATE_O	Output	16	Rx data rate. The following are the data rate values: • x1734 = 5940 Mbps • x0B9A = 2960 Mbps • x05CD = 1485 Mbps • x2E6 = 742.5 Mbps
R_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “R” data
G_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “G” data
B_O	Output	NUMBER OF PIXELS × Color Depth bits	Decoded “B” data
SDA_O	Output	1	I2C serial data output for DDC
HPD_O	Output	1	Hot plug detect output signal
ACR_CTS_O	Output	20	Audio Clock Regeneration Cycle timestamp value
ACR_N_O	Output	20	Audio Clock Regeneration value (N) parameter
ACR_VALID_O	Output	1	Audio Clock Regeneration valid signal
AUDIO_SAMPLE_CH1_O	Output	24	Channel 1 audio sample data
AUDIO_SAMPLE_CH2_O	Output	24	Channel 2 audio sample data
AUDIO_SAMPLE_CH3_O	Output	24	Channel 3 audio sample data
AUDIO_SAMPLE_CH4_O	Output	24	Channel 4 audio sample data
AUDIO_SAMPLE_CH5_O	Output	24	Channel 5 audio sample data
AUDIO_SAMPLE_CH6_O	Output	24	Channel 6 audio sample data
AUDIO_SAMPLE_CH7_O	Output	24	Channel 7 audio sample data
AUDIO_SAMPLE_CH8_O	Output	24	Channel 8 audio sample data

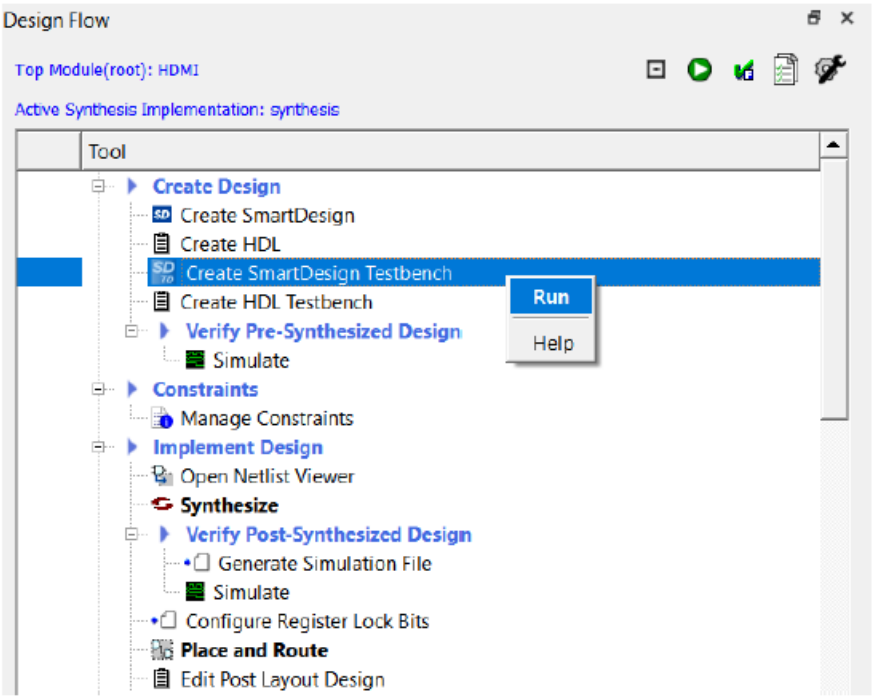
Testbench Simulation (Ask a Question)

Testbench is provided to check the functionality of HDMI RX core. Testbench works only in Native Interface when the number of pixels is one.

To simulate the core using the testbench, perform the following steps:

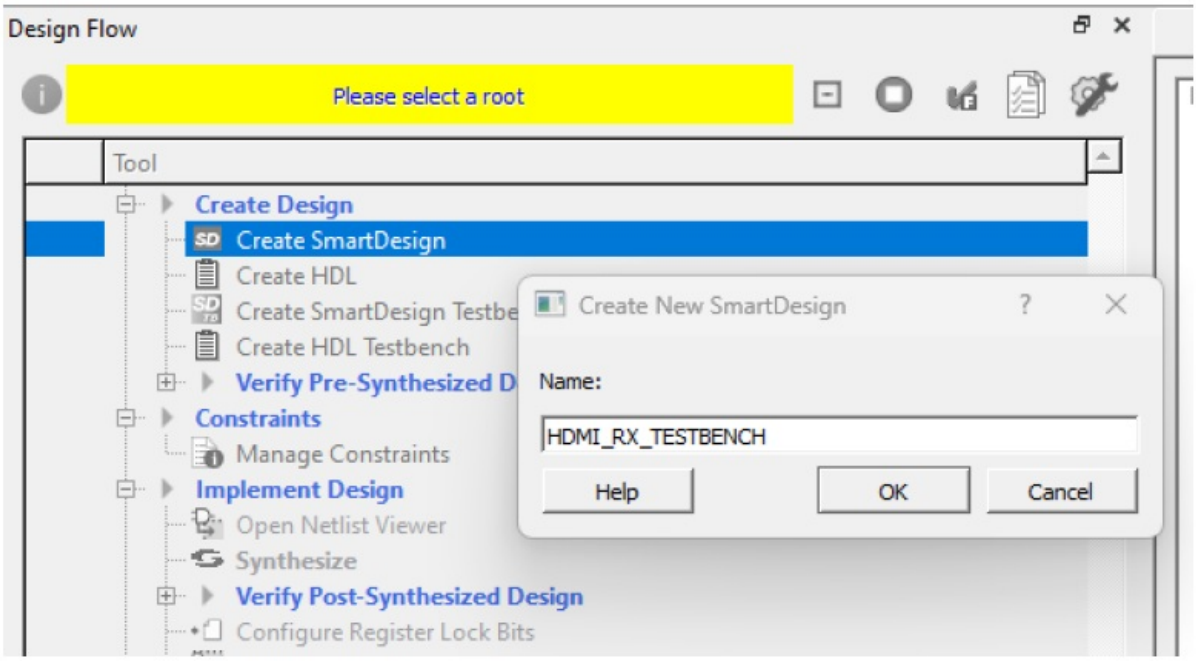
1. In the Design Flow window, expand Create Design.
2. Right-click Create SmartDesign Testbench, and then click Run, as shown in the following figure.

   Figure 5-1. Creating SmartDesign Testbench



3. Enter a name for the SmartDesign testbench, and then click OK.

   Figure 5-2. Naming SmartDesign Testbench



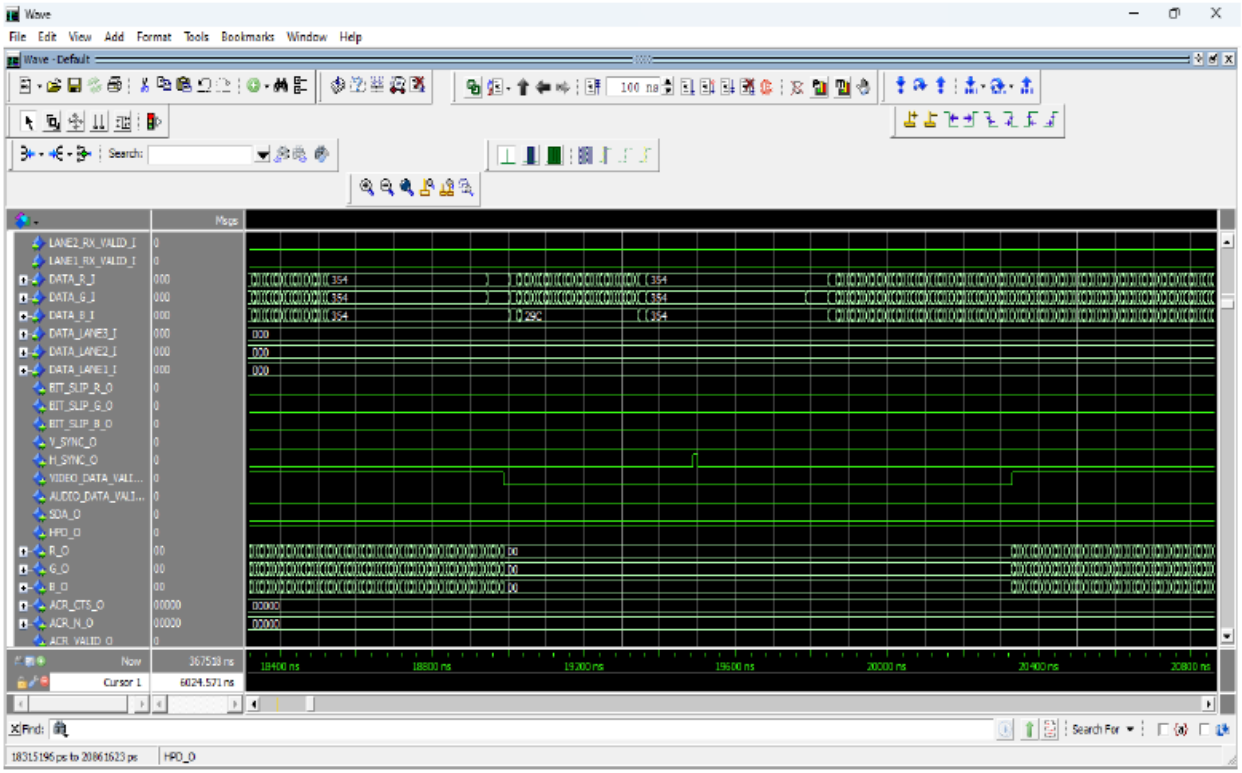
   SmartDesign testbench is created, and a canvas appears to the right of the Design Flow pane.

4. Navigate to Libero® SoC Catalog, select View > Windows > IP Catalog, and then expand Solutions-Video. Double-click HDMI RX IP (v5.4.0) and then click OK.
5. Select all the ports, right-click and select Promote to Top Level.
6. On the SmartDesign tool bar, click Generate Component.

7. On the Stimulus Hierarchy tab, right-click HDMI_RX_TB testbench file, and then click Simulate Pre-Synth Design > Open Interactively.

The ModelSim® tool opens with the testbench, as shown in the following figure.

Figure 5-3. ModelSim Tool with HDMI RX Testbench File



Important: If the simulation is interrupted due to the run time limit specified in the DO file, use the run -all command to complete the simulation.

License (Ask a Question)

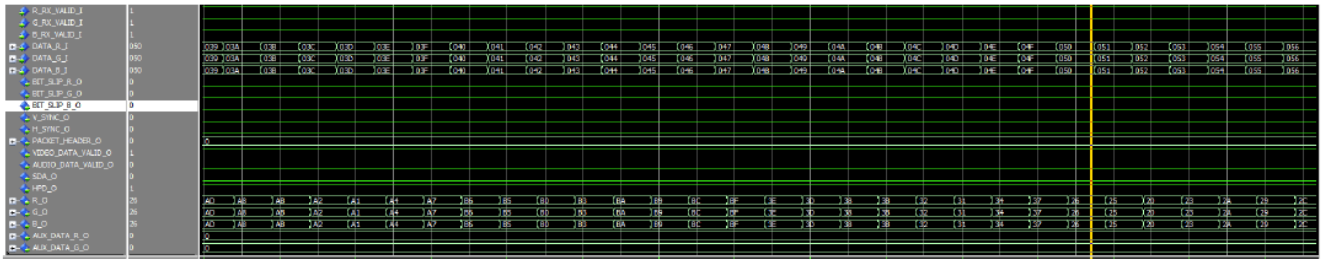
HDMI RX IP is provided with the following two license options:

- Encrypted: Complete encrypted RTL code is provided for the core. It is available for free with any of the Libero license, enabling the core to be instantiated with SmartDesign. You can perform Simulation, Synthesis, Layout, and program the FPGA silicon using the Libero design suite.
- RTL: Complete RTL source code is license locked, which needs to be purchased separately.

Simulation Results (Ask a Question)

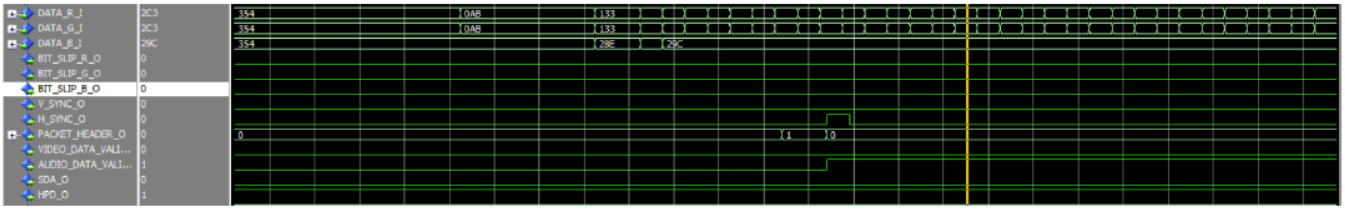
The following timing diagram for HDMI RX IP shows video data and control data periods.

Figure 6-1. Video Data



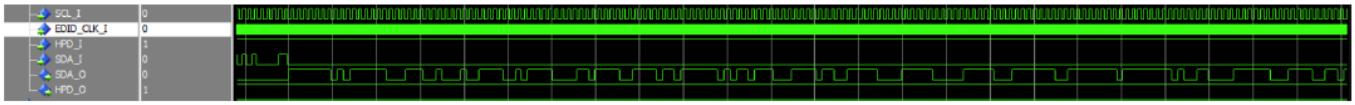
The following diagram shows the hsync and vsync outputs for the corresponding control data inputs.

Figure 6-2. Horizontal Sync and Vertical Sync Signals



The following diagram shows EDID part.

Figure 6-3. EDID Signals



Resource Utilization (Ask a Question)

HDMI RX IP is implemented in PolarFire® FPGA (MPF300T – 1FCG1152I Package). The following table lists the resources utilized when Number of Pixels = 1 pixel.

Table 7-1. Resource Utilization for 1 Pixel Mode

Color Format	Color Depth	SCRAMBLER	Fabric 4LUT	Fabric DFF	Interface 4LUT	Interface DFF	uSRAM (64×12)	LSRAM (20k)
RGB	8	Disable	987	1867	360	360	0	10
	10	Disable	1585	1325	456	456	11	9
	12	Disable	1544	1323	456	456	11	9
	16	Disable	1599	1331	492	492	14	9
YCbCr422	8	Disable	1136	758	360	360	3	9
YCbCr444	8	Disable	1105	782	360	360	3	9
	10	Disable	1574	1321	456	456	11	9
	12	Disable	1517	1319	456	456	11	9
	16	Disable	1585	1327	492	492	14	9

The following table lists the resources utilized when Number of Pixels = 4 pixel.

Table 7-2. Resource Utilization for 4 Pixel Mode

Color Format	Color Depth	SCRAMBLER	Fabric 4LUT	Fabric DFF	Interface 4LUT	Interface DFF	uSRAM (64×12)	LSRAM (20k)
RGB	8	Disable	1559	1631	1080	1080	9	27
	12	Disable	1975	2191	1344	1344	31	27
	16	Disable	1880	2462	1428	1428	38	27
RGB	10	Enable	4231	3306	1008	1008	3	27
	12	Enable	4253	3302	1008	1008	3	27
	16	Enable	3764	3374	1416	1416	37	27
YCbCr422	8	Disable	1485	1433	912	912	7	23
YCbCr444	8	Disable	1513	1694	1080	1080	9	27
	12	Disable	2001	2099	1344	1344	31	27
	16	Disable	1988	2555	1437	1437	38	27

The following table lists the resources utilized when Number of Pixels = 4 pixel and SCRAMBLER is enabled.

Table 7-3. Resource Utilization for 4 Pixel Mode and SCRAMBLER is Enabled

Color Format	Color Depth	SCRAMBLER	Fabric 4LUT	Fabric DFF	Interface 4LUT	Interface DFF	uSRAM (64×12)	LSRAM (20k)
RGB	8	Enable	5029	5243	1126	1126	9	28
YCbCr422	8	Enable	4566	3625	1128	1128	13	27
YCbCr444	8	Enable	4762	3844	1176	1176	17	27

System Integration (Ask a Question)

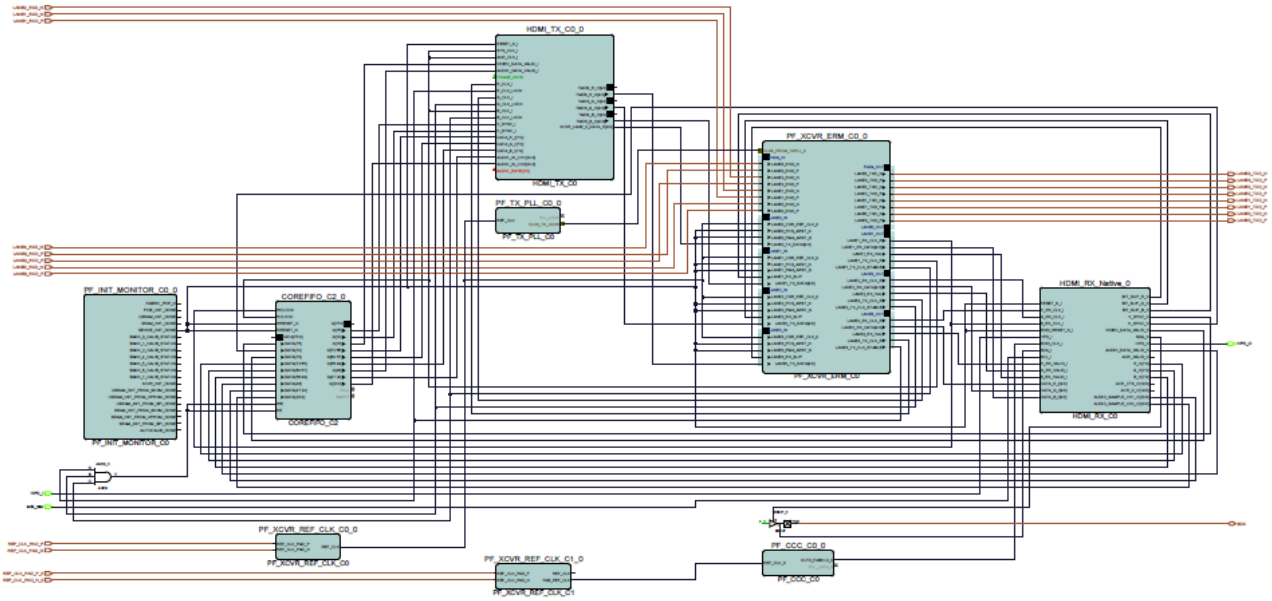
This section shows how to integrate the IP into Libero design.
The following table lists the configurations of PF XCVR, PF TX PLL and PF CCC required for different resolutions and bit widths.

Table 8-1. PF XCVR, PF TX PLL and PF CCC Configurations

Resolution	Bit Width	PF XCVR Configuration			CDR REF CLOCK PADS	PF CCC Configuration	
		RX Data Rate	RX CDR Ref Clock Frequency	RX PCS Fabric Width		Input Frequency	Output Frequency
1 PXL (1080p60)	8	1485	148.5	10	AE27, AE28	NA	NA
1 PXL (1080p30)	10	1485	148.5	10	AE27, AE28	92.5	74
	12	1485	148.5	10	AE27, AE28	74.25	111.375
	16	1485	148.5	10	AE27, AE28	74.25	148.5
4 PXL (1080p60)	8	1485	148.5	40	AE27, AE28	NA	NA
	12	1485	148.5	40	AE27, AE28	55.725	37.15
	16	1485	148.5	40	AE27, AE28	74.25	37.125
4 PXL (4kp30)	8	1485	148.5	40	AE27, AE28	NA	NA
	10	3712.5	148.5	40	AE29, AE30	92.81	74.248
	12	4455	148.5	40	AE29, AE30	111.375	74.25
	16	5940	148.5	40	AE29, AE30	148.5	74.25
4 PXL (4Kp60)	8	5940	148.5	40	AE29, AE30	NA	NA

HDMI RX Sample Design 1: When configured in Color Depth = 8-bit and Number of Pixels = 1 Pixel mode, is shown in the following figure.

Figure 8-1. HDMI RX Sample Design 1

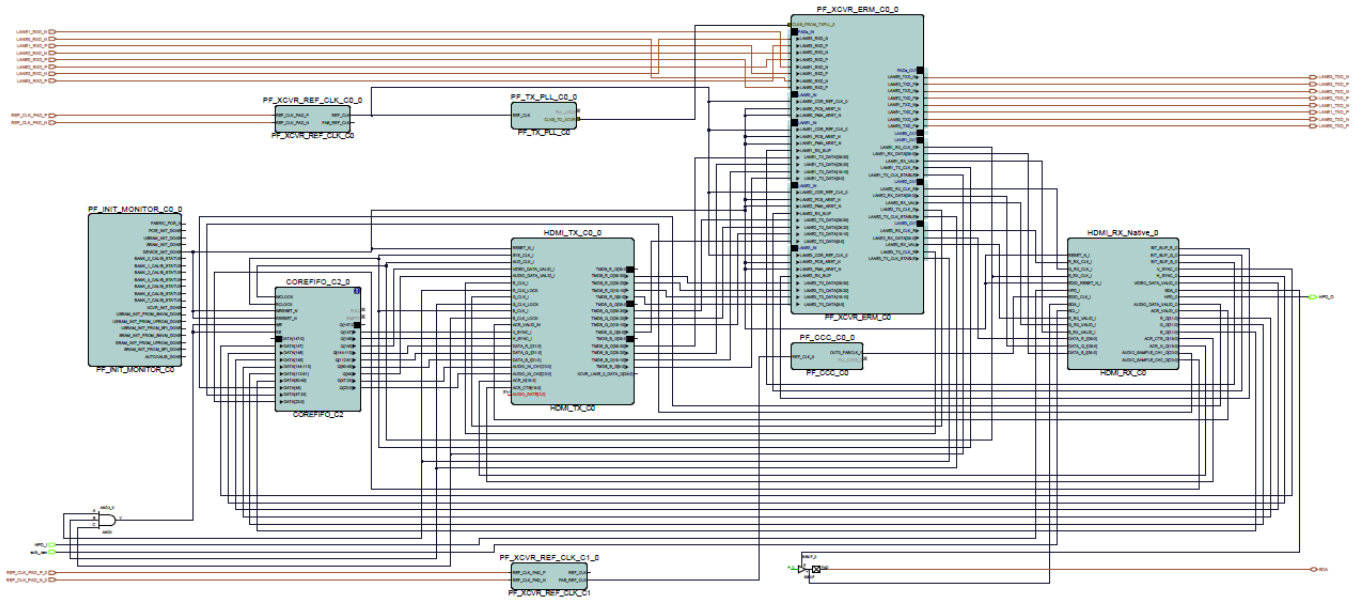


For example, in 8-bit configurations, the following components are the part of the design:

- PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for TX and RX full duplex mode. RX data rate of 1485 Mbps in PMA mode, with the data width configured as 10 bit for 1 PXL mode and 148.5 MHz CDR reference clock. TX data rate of 1485 Mbps in PMA mode, with the data width configured as 10 bit with clock division factor 4.
- LANE0_CDR_REF_CLK, LANE1_CDR_REF_CLK, LANE2_CDR_REF_CLK and LANE3_CDR_REF_CLK are driven from the PF_XCVR_REF_CLK with AE27, AE28 Pad pins.
- EDID CLK_I pin should driven with 150 MHz clock with CCC.
- R_RX_CLK_I, G_RX_CLK_I and B_RX_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R and LANE1_TX_CLK_R, respectively.
- R_RX_VALID_I, G_RX_VALID_I and B_RX_VALID_I are driven by LANE3_RX_VAL, LANE2_RX_VAL and LANE1_RX_VAL, respectively.
- DATA_R_I, DATA_G_I and DATA_B_I are driven by LANE3_RX_DATA, LANE2_RX_DATA and LANE1_RX_DATA, respectively.

HDMI RX Sample Design 2: When configured in Color Depth = 8-bit and Number of Pixels = 4 Pixel mode, is shown in the following figure.

Figure 8-2. HDMI RX Sample Design 2

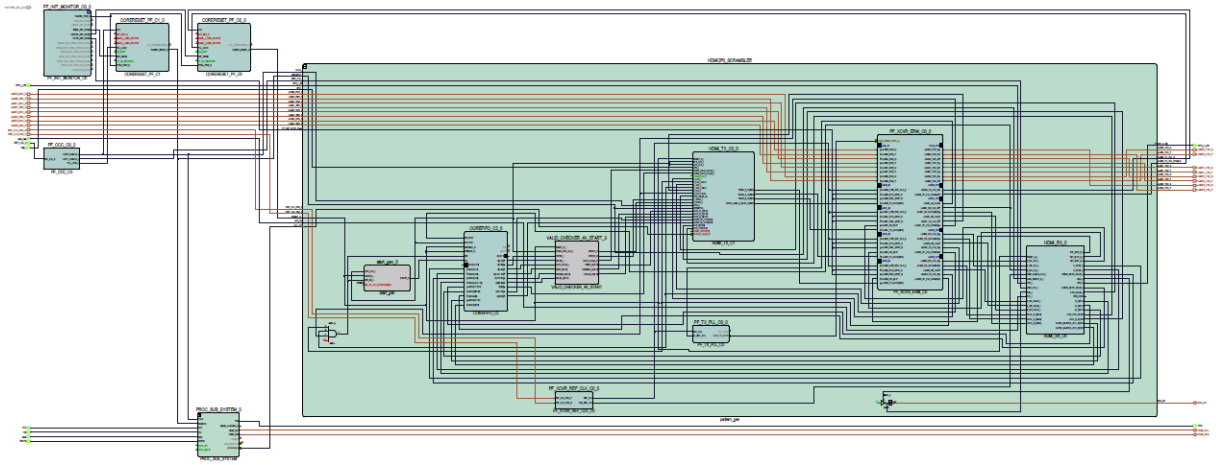


For example, in 8-bit configurations, the following components are the part of the design:

- PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for TX and RX full duplex mode. RX data rate of 1485 Mbps in PMA mode, with the data width configured as 40 bit for 4 PXL mode and 148.5 MHz CDR reference clock. TX data rate of 1485 Mbps in PMA mode, with the data width configured as 40 bit with clock division factor 4.
- LANE0_CDR_REF_CLK, LANE1_CDR_REF_CLK, LANE2_CDR_REF_CLK and LANE3_CDR_REF_CLK are driven from the PF_XCVR_REF_CLK with AE27, AE28 Pad pins.
- EDID CLK_I pin should driven with 150 MHz clock with CCC.
- R_RX_CLK_I, G_RX_CLK_I and B_RX_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R and LANE1_TX_CLK_R, respectively.
- R_RX_VALID_I, G_RX_VALID_I and B_RX_VALID_I are driven by LANE3_RX_VAL, LANE2_RX_VAL and LANE1_RX_VAL, respectively.
- DATA_R_I, DATA_G_I and DATA_B_I are driven by LANE3_RX_DATA, LANE2_RX_DATA and LANE1_RX_DATA, respectively.

HDMI RX Sample Design 3: When configured in Color Depth = 8-bit and Number of Pixels = 4 Pixel mode and SCRAMBLER = Enabled, is shown in the following figure.

Figure 8-3. HDMI RX Sample Design 3

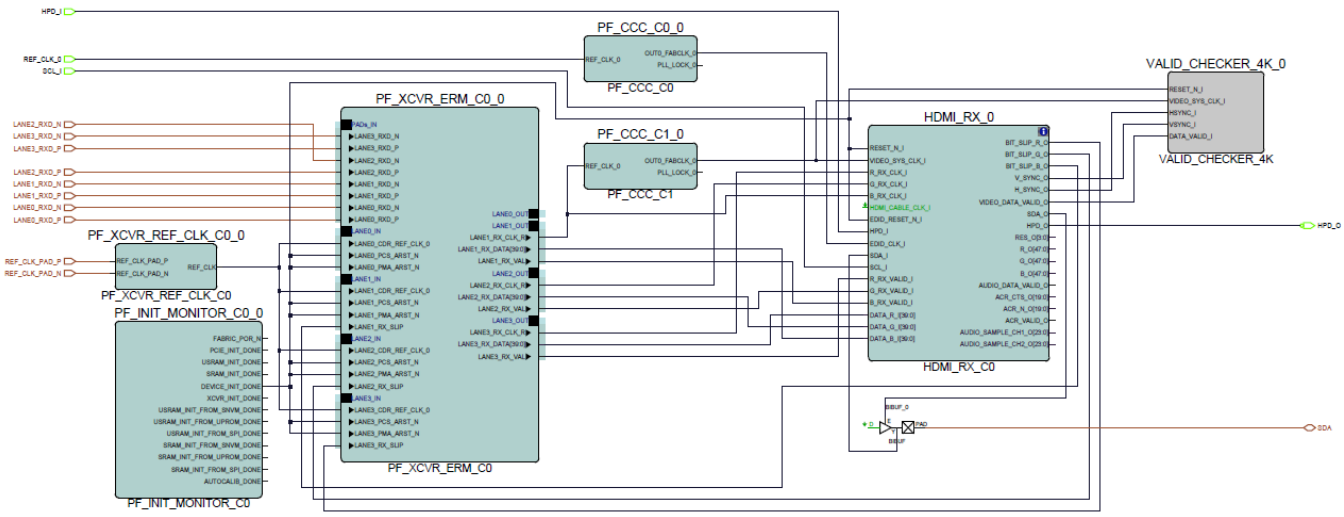


For example, in 8-bit configurations, the following components are the part of the design:

- PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for TX and RX Independent mode. RX data rate of 5940 Mbps in PMA mode, with the data width configured as 40 bit for 4 PXL mode and 148.5 MHz CDR reference clock. TX data rate of 5940 Mbps in PMA mode, with the data width configured as 40 bit with clock division factor 4.
- LANE0_CDR_REF_CLK, LANE1_CDR_REF_CLK, LANE2_CDR_REF_CLK and LANE3_CDR_REF_CLK are driven from the PF_XCVR_REF_CLK with AF29, AF30 Pad pins.
- EDID CLK_I pin should drive with 150 MHz clock with CCC.
- R_RX_CLK_I, G_RX_CLK_I and B_RX_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R and LANE1_TX_CLK_R, respectively.
- R_RX_VALID_I, G_RX_VALID_I and B_RX_VALID_I are driven by LANE3_RX_VAL, LANE2_RX_VAL and LANE1_RX_VAL, respectively.
- DATA_R_I, DATA_G_I and DATA_B_I are driven by LANE3_RX_DATA, LANE2_RX_DATA and LANE1_RX_DATA, respectively.

HDMI RX Sample Design 4: When configured in Color Depth = 12-bit and Number of Pixels = 4 Pixel mode and SCRAMBLER = Enabled, is shown in the following figure.

Figure 8-4. HDMI RX Sample Design 4



For example, in 12-bit configurations, the following components are the part of the design:

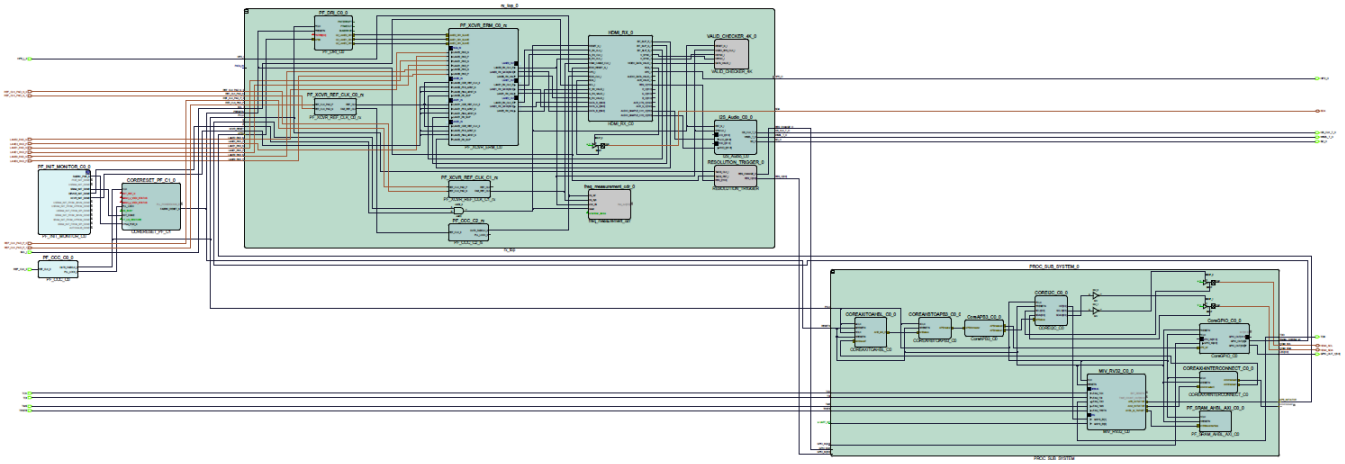
- PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for RX Only mode. RX data rate of 4455 Mbps in PMA mode, with the data width configured as 40 bit for 4 PXL mode and 148.5 MHz CDR reference clock.
- LANE0_CDR_REF_CLK, LANE1_CDR_REF_CLK, LANE2_CDR_REF_CLK and LANE3_CDR_REF_CLK are driven from the PF_XCVR_REF_CLK with AF29, AF30 Pad pins.
- EDID CLK_I pin should drive with 150 MHz clock with CCC.
- R_RX_CLK_I, G_RX_CLK_I and B_RX_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R and LANE1_TX_CLK_R, respectively.
- R_RX_VALID_I, G_RX_VALID_I and B_RX_VALID_I are driven by LANE3_RX_VAL, LANE2_RX_VAL and LANE1_RX_VAL, respectively.
- DATA_R_I, DATA_G_I and DATA_B_I are driven by LANE3_RX_DATA, LANE2_RX_DATA and

LANE1_RX_DATA, respectively.

- The PF_CCC_C0 module generates a clock named OUT0_FABCLK_0 with a frequency of 74.25 MHz, derived from an input clock of 111.375 MHz, which is driven by LANE1_RX_CLK_R.

HDMI RX Sample Design 5: When configured in Color Depth = 8-bit, Number of Pixels = 4 Pixel mode and SCRAMBLER = Enabled is shown in the following figure. This design is dynamic data rate with DRI.

Figure 8-5. HDMI RX Sample Design 5



For example, in 8-bit configurations, the following components are the part of the design:

- PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for RX Only mode with enabled dynamic reconfiguration interface. RX data rate of 5940 Mbps in PMA mode, with the data width configured as 40 bit for 4 PXL mode and 148.5 MHz CDR reference clock.
- LANE0_CDR_REF_CLK, LANE1_CDR_REF_CLK, LANE2_CDR_REF_CLK and LANE3_CDR_REF_CLK are driven from the PF_XCVR_REF_CLK with AF29, AF30 Pad pins.
- EDID CLK_I pin should drive with 150 MHz clock with CCC.
- R_RX_CLK_I, G_RX_CLK_I and B_RX_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R and LANE1_TX_CLK_R, respectively.
- R_RX_VALID_I, G_RX_VALID_I and B_RX_VALID_I are driven by LANE3_RX_VAL, LANE2_RX_VAL and LANE1_RX_VAL, respectively.
- DATA_R_I, DATA_G_I and DATA_B_I are driven by LANE3_RX_DATA, LANE2_RX_DATA and LANE1_RX_DATA, respectively.

Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description

D	02/2025	The following is the list of changes made in revision C of th e document: • Updated the HDMI RX IP version to 5.4. • Updated Introduction with features and unsupported feat ures. • Added Tested Source Devices section. • Updated Figure 3-1 and Figure 3-3 in the Hardware Impl ementation section. • Added Configuration Parameters section. • Updated Table 4-2, Table 4-4, Table 4-5, Table 4-6 and T able 4-7 in the Ports section. • Updated Figure 5-2 in the Testbench Simulation section. • Updated Table 7-1 and Table 7-2 added Table 7-3 in the Resource Utilization section. • Updated Figure 8-1, Figure 8-2, Figure 8-3 and Figure 8-4 in the System Integration section. • Added dynamic data rate with DRI design example in the System Integration section.
C	02/2023	The following is the list of changes made in revision C of th e document: • Updated the HDMI RX IP version to 5.2 • Updated the supported resolution in four pixel mode thro ughout the document • Updated Figure 2-1
B	09/2022	The following is the list of changes made in revision B of the document: • Updated the document for v5.1 • Updated Table 4-2 and Table 4-3
A	04/2022	The following is the list of changes in revision A of the docu ment: • The document was migrated to the Microchip template • The document number was updated to DS50003298A fr om 50200863 • Updated section TMDS Decoder • Updated tables Table 4-2 and Table 4-3 • Updated Figure 5-3, Figure 6-1, Figure 6-2

2.0	—	The following is a summary of the changes made in this revision. • Added Table 4-3 • Updated Resource Utilization tables
1.0	08/2021	Initial Revision.

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FAQ

- **Q: How do I update the HDMI RX IP core?**
  A: The IP core can be updated through Libero SoC software or manually downloaded from the catalog. Once installed in Libero SoC software IP Catalog, it can be configured, generated, and instantiated within SmartDesign for inclusion in the project.

Documents / Resources

	MICROCHIP PolarFire FPGA High Definition Multimedia Interface HDMI Receiver [pdf] User Guide PolarFire FPGA, PolarFire FPGA High Definition Multimedia Interface HDMI Receiver, High Definition Multimedia Interface HDMI Receiver, Multimedia Interface HDMI Receiver, Interface HDMI Receiver, HDMI Receiver

References

- User Manual