MICROCHIP MPFS250T CoreSmartBERT Core Provides A Broad Based Evaluation User Guide

Contents

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Product Information

Specifications

- **Core Version:** CoreSmartBERT v2.10
- **Supported Tool Flow:** N/A
- **Licensing:** No license required. Complete Verilog RTL source code provided.
- Features:
  - Device Utilization and Performance

Device Utilization and Performance

The CoreSmartBERT IP core is designed to be used with Field Programmable Gate Array (FPGA) devices. The following FPGA device families are supported:

Family	Device	LUTs	DFF	Logic Elements	Performance (MHz)
PolarFire	MPFS250T	2860	1082	3050	125
PolarFire	MPF300T	2860	1082	3050	125

Product Usage Instructions

Functional Description

- The CoreSmartBERT IP core is designed to add test features for the transceiver, allowing the end user to evaluate the Physical
- Media Attachment (PMA) functionality of the transceiver on a board.
- The SmartDebug tool interfaces with this core, providing an interactive Graphical User Interface (GUI) control.

Implementation of IP Core in Libero Design Suite

To implement the CoreSmartBERT IP core in the Libero Design Suite, follow these steps:

1. Open the Libero Design Suite.
2. Select the project where you want to implement the IP core.
3. Import the CoreSmartBERT IP core into the project.
4. Configure the IP core settings according to your requirements.
5. Generate the necessary output files for synthesis and implementation.
6. Proceed with synthesis and implementation using the generated files.

CoreSmartBERT Register Summary

The CoreSmartBERT IP core includes various registers for configuration and control. The register summary is as follows:

- SLE_DEBUG Marco: This register provides debug information and control options for the CoreSmartBERT IP core.

CoreSmartBERT Additional References

For additional references and information on CoreSmartBERT, refer to the following:

- CoreSmartBERT Known Issues Workarounds: This document provides workarounds for known issues related to CoreSmartBERT.

FAQ

Q: Is a license required for CoreSmartBERT?

- **A:** No, CoreSmartBERT does not require any license.

Q: What version of CoreSmartBERT does this user guide apply to?

- **A:** This user guide applies to CoreSmartBERT v2.10.

Q: What FPGA device families are supported by CoreSmartBERT?

- **A:** CoreSmartBERT supports the PolarFire FPGA device families, specifically MPFS250T and MPF300T.

Q: What is the purpose of the SmartDebug tool?

- **A:** The SmartDebug tool interfaces with the CoreSmartBERT IP core and provides an interactive GUI control for the user.

Introduction

(Ask a Question)

- The CoreSmartBERT core provides a broad-based evaluation and demonstration platform for PolarFire® and PolarFire SoC transceivers. CoreSmartBERT is configurable to use different transceivers, clocking topologies, line rates, and reference clock rates.
- Data pattern generators and checkers are included for each transceiver, giving several different Pseudo Random Binary Sequences (PRBS) (27, 29, 223, and 231). The pattern generator sends data out through the transmitter. The pattern checker accepts data through the receiver and checks it against an internally generated pattern. These patterns are optimized for the logic width that has been selected at run time. SmartDebug provides the user interface to this core.
- This user guide provides information on the CoreSmartBERT IP core and the features it supports.
- The purpose of this IP core is to add more test features for the transceiver so that the end user can evaluate the Physical Media Attachment (PMA) functionality of the transceiver on a board.
- The SmartDebug tool interfaces with this core, which allows the user to have an interactive Graphical User Interface (GUI) control.

Summary

Core Version	This document applies to CoreSmartBERT v2.10.
Supported Device Families	PolarFire® and PolarFire SoC
Supported Tool Flow	Requires Libero® SoC v12.6 or later releases.
Licensing	CoreSmartBERT does not require any license. Complete Verilog RTL source code is provided for the core and testbench.

Features

CoreSmartBERT has the following features:

- Supports PolarFire and PolarFire SoC Transceiver built-in PRBS Generator or Checker
- Generates a List of Patterns
- Inserts an Error into the Transmit Pattern
- Checking of Errors in the Receive Pattern
- Instantiating the Pattern Functionality Several Times to Support Multiple Lanes Simultaneously

Device Utilization and Performance

(Ask a Question)

The following Field Programmable Gate Array (FPGA) device families implement CoreSmartBERT. The following table lists the summary of the implementation date for CoreSmartBERT.

Table 1. CoreSmartBERT Utilization

Device Details		Resources			Performance (MHz)
Family	**Device**	**LUTs**	**DFF**	**Logic Elements**	
PolarFire® SoC	MPFS250T	2860	1082	3050	125
PolarFire	MPF300T	2860	1082	3050	125

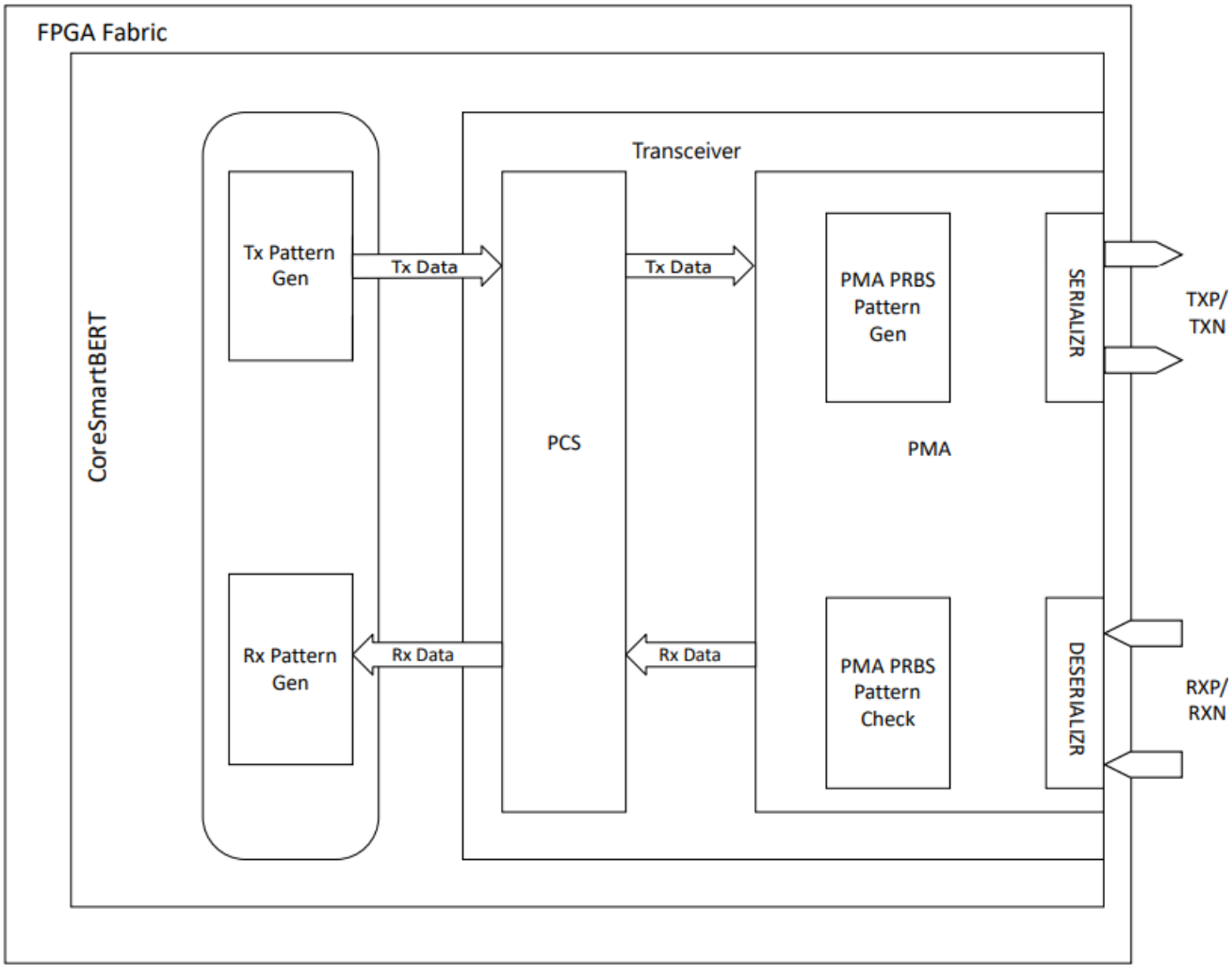
Important: We get the data in the preceding table using typical synthesis and layout settings: CDR reference clock source as Dedicated and unchanged other configurator values.

Functional Description

(Ask a Question)

- CoreSmartBERT includes the transceiver, which interfaces with the SmartDEBUG tool through a user control GUI, to run the hardened PRBS generator and checkers.
- It also has fabric pattern generators and checkers with more features (for example, error injection) than the ones included in a transceiver. The following figure shows the block diagram of CoreSmartBERT.

Figure 1-1. CoreSmartBERT Block Diagram



CoreSmartBERT IP consists of the following blocks:

- TX Pattern Gen This transmitter block generates the following pattern:
- PRBS 7, 9, 23, 31 with error insertion logic
- RX Pattern CHK The receiver block checks the following patterns:
- PRBS 7, 9, 23, 31
- Transceiver The transceiver is PolarFire/PolarFire SoC's transceiver macro in Physical Media Attachment (PMA) mode.
- PRBS Pseudo Random Binary Sequence (PRBS) test patterns generate deterministic sequences with the properties of highly random signals, for example: white noise.
- CoreSmartBERT supports the built-in PBRS pattern generators and checkers in the transceiver and adds support for the fabric PRBS pattern generators and checkers with the ability to inject errors into the transmitter path.

These include support for the following:

- PRBS 7
- PRBS 9
- PRBS 23
- PRBS 31

Smart Debug Tool

- The transceiver is PolarFire/PolarFire SoC's transceiver macro in Physical Media Attachment (PMA) mode. SmartDebug provides the user interface to control the CoreSmartBERT core to use its features.

SmartDebug has the following capabilities:

- Ability to control CoreSmartBERT and have the signal integrity controls on the screen at the same time
- Automatic detection of the presence of CoreSmartBERT in the design
- Ability to select the particular transceiver lane associated with CoreSmartBERT
- Availability of several pattern options
- An ability to enable to start of the pattern transmitter
- An ability to enable to start of the pattern receiver
- A button to insert a single error
- An error counter with a clear button

Interface (Ask a Question)

- This section discusses the parameters in the CoreSmartBERT GUI configurator and I/O signals.

Configuration GUI Parameters (Ask a Question)

- The following table describes the UI parameters for configuring the CoreSmartBERT core.

- **Important:** The Name column shows the actual parameter name used in RTL. The Description column starts with the parameter name as it appears in the CoreSmartBERT configurator (GUI interface).
- These two names are used interchangeably throughout the document.

Table 2-1. CoreSmartBERT Parameters Descriptions

Name	Range	Default	Description
UI_PATTERN_PRBS7	0 or 1	1	**PRBS7** Pattern Enable
UI_PATTERN_PRBS9	0 or 1	1	**PRBS9** Pattern Enable
UI_PATTERN_PRBS23	0 or 1	1	**PRBS23** Pattern Enable
UI_PATTERN_PRBS31	0 or 1	1	**PRBS31** Pattern Enable
UI_NUMBER_OF_LANES	1-4	1	**Number of lanes** Number of lanes this IP core has enabled.
UI_DATA_RATE	250 – 10000	5000	**Transceiver data rate** Supported rates: • 250 Mbps • 1000 Mbps • 1250 Mbps • 2500 Mbps • 3125 Mbps • 5000 Mbps • 6250 Mbps • 8000 Mbps • 10000 Mbps • 10312.5 Mbps
UI_TX_CLK_DIV_FACTOR	1, 2, 4, 8 & 11	1	**TX clock division factor**
UI_CDR_REFERENCE_CLK_SOURCE	Dedicated or Fabric	Fabric	**CDR reference clock source**

……..continued			
Name	**Range**	**Default**	**Description**
UI_CDR_REFERENCE_CLK_FREQ	0-312.5	125	**CDR reference clock frequency** Supported frequencies: • 25.00 MHz • 31.25 MHz • 50.00 MHz • 62.50 MHz • 75.00 MHz • 100.00 MHz • 125.00 MHz • 150.00 MHz • 156.25 MHz • 312.50 MHz

I/O Signals (Ask a Question)

- This section describes the various I/O signal descriptions of CoreSmartBERT.
- The following table describes the port signals for CoreSmartBERT.
- **Important:** In the following tables, n represents a range of 0 to 3 depending on the number of configured lanes.

Table 2-2. CoreSmartBERT I/O Signal Descriptions

Name	Width	Direction	Description
SYS_RESET_N	1	Input	Active low system reset
LANE[n]_CDR_REF_CLK_FAB	1	Input	CDR reference clock from fabric, only exposed when **Fabric** is selected as CDR reference clock source.
LANE[n]_CDR_REF_CLK_0	1	Input	CDR reference clock from the dedicated pin, is only exposed when the **Dedicated** is selected as the CDR reference clock source.
LANE[n]_TX_BIT_CLK_0	1	Input	Tx Bit Clock
LANE[n]_TX_PLL_REF_CLK_0	1	Input	PLL Reference Clock
LANE[n]_TX_PLL_LOCK_0	1	Input	PLL Lock

The following table describes the pad signals for CoreSmartBERT.
Table 2-3. CoreSmartBERT PAD Signal Descriptions

Name	Direction	Description
LANE[n]_TXD_P	Output	Transmitter Serial Data
LANE[n]_TXD_N	Output	
LANE[n]_RXD_P	Input	Receiver Serial Data
Lane[n]_RXD_N	Input	

Implementation of IP Core in Libero Design Suite

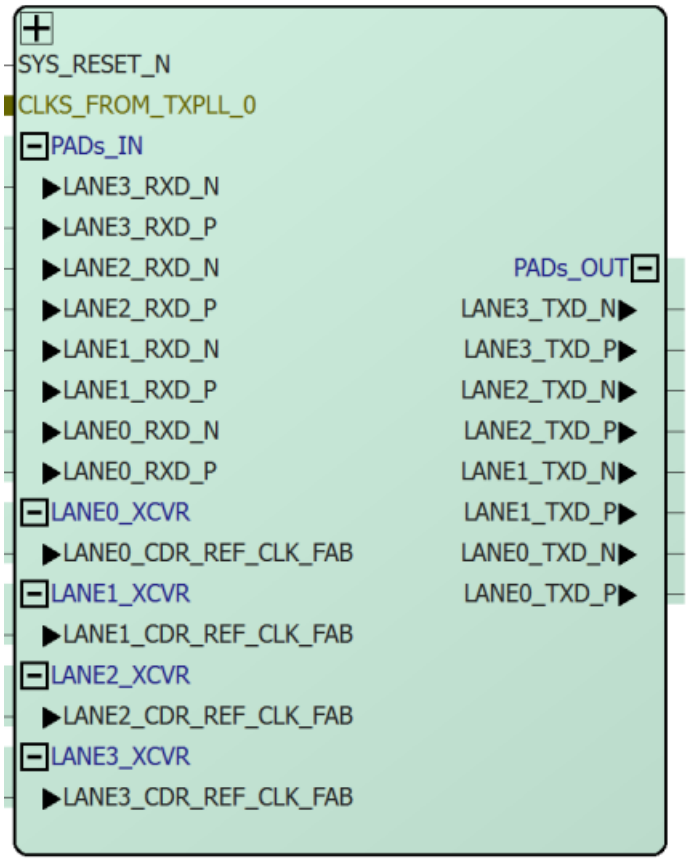
(Ask a Question)

- This section describes an implementation of the CoreSmartBERT in the Libero Design Suite.

SmartDesign (Ask a Question)

- CoreSmartBERT is available for download to the SmartDesign IP catalog through the Libero SOC web repository.
- To know how to create a SmartDesign project, see the SmartDesign User Guide.
- The following figure shows an example of an instantiated view of CoreSmartBERT on the SmartDesign canvas.

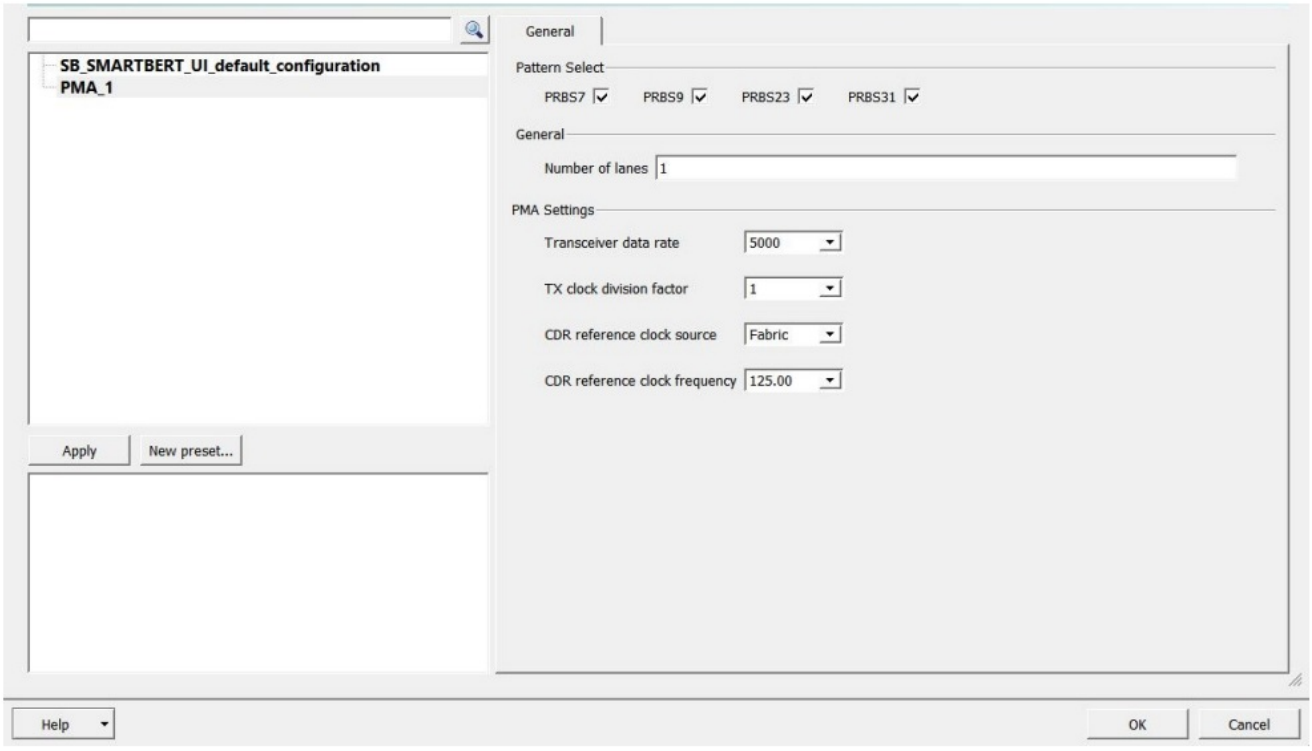
Figure 3-1. Instantiation of CoreSmartBERT on SmartDesign Canvas



Configuring the CoreSmartBERT (Ask a Question)

- The following figure shows how the core instance can be configured using its configuration GUI.

Figure 3-2. CoreSmartBERT SmartDesign Configuration GUI



For more information on the CoreSmartBERT configurator, see 2.1. Configuration GUI Parameters.

Synthesizing in Libero SoC (Ask a Question)

To run synthesis with the configuration selected in the configuration GUI, perform the following steps

1. Set the design root appropriately.
2. Under Implement Design, in the Design Flow tab, right-click Synthesize, and then click Run.

Running Place-and-Route in Libero SoC (Ask a Question)

To run the place and route, perform the following steps:

- On the Design Flow tab, select Implement Design, right-click Place and Route, and then from the context menu, select Run.

CoreSmartBERT Register Summary

(Ask a Question)

- This section describes the register description of CoreSmartBERT IP.

SLE_DEBUG Marco (Ask a Question)

- SLE_DEBUG Marco is used to communicate with SmartDebug. The SLE_DEBUG mechanism gives the ability to run synthesis while preserving a set of registers.
- It provides the ability to identify, rename, and classify registers for SmartDebug.
- CoreSmartBERT has SLE_DEBUG write and read registers that are used to inform the Smart Debug tool of parameters settings chosen, IP core versions number, and control various functions (for example, error injection, read errors, and so on.).
- The following table describes the SLE_DEBUG registers that are used in CoreSmartBERT.

Table 4-1. SLE_DEBUG Registers

Bits	Function	Type	Description

14	SLE_DATA_RATE	R	Reads data rate selected from the GUI. 1: 250 Mbps 2: 1000 Mbps 3: 1250 Mbps 4: 2500 Mbps 5: 3125 Mbps 6: 5000 Mbps 7: 6250 Mbps 8: 8000 Mbps 9: 10000 Mbps 10: 10312.5Mbps
4	SLE_TX_CLK_DIV_FACTOR	R	Reads **Tx Clock Divide Factor** selected from the GUI.
1	SLE_CDR_REFERENCE_CLK_SOURCE	R	Reads the CDR Reference Clock Source selected from the GUI: 0: Dedicated 1: Fabric
4	SLE_CDR_REFERENCE_CLK_FREQ	R	Reads the CDR Reference Clock Frequency selected from the GUI: 0: 25.00 1: 31.25 2: 50.00 3: 62.50 4: 75.00 5: 100.00 6: 125.00 7: 150.00 8: 156.25 9: 312.50
2	SLE_NUMBER_OF_LANES	R	Reads the number of lanes this IP core has enabled from the GUI.
1	SLE_PATTERN_PRBS7	R	Reads the PRBS7 pattern enabled from the GUI.
1	SLE_PATTERN_PRBS9	R	Reads the PRBS9 pattern enabled from the GUI.
1	SLE_PATTERN_PRBS23	R	Reads the PRBS23 pattern enabled from the GUI.
1	SLE_PATTERN_PRBS31	R	Reads the PRBS31 pattern enabled from the GUI.

16	SLE_CPZ_VERSION	R	Reads the CPZ Version number. This register represents 8bit major and 8bit minor version numbers. For example, v2.1 = {8'd2, 8'd1}

……..continued

Bits	Function	Type	Description
4	SLE_TX_LANE[n]_PATTEN_GEN	RW	Transmitter Pattern Generator: 0: PRBS7 1: PRBS 9 1: PRBS23 2: PRBS31 **Note:** The default value is set to 0.
1	SLE_TX_LANE[n]_GEN_EN	RW	Transmitter Pattern Generator Enable: 0: Disabled 1: Enabled **Note:** The default value is set to 0.
4	SLE_RX_LANE[n]_PATTEN_CHK	RW	Receiver Pattern Checker: 0: PRBS7 1: PRBS9 2: PRBS23 3: PRBS31 **Note:** The default value is set to 0.
1	SLE_RX_LANE[n]_CHR_EN	RW	Receiver Pattern Checker Enable: 0: Disabled 1: Enabled **Note:** The default value is set to 0.
32	SLE_RX_LANE[n]_ERR_CNT	R	Receiver error counter.
1	SLE_ RX_LANE[n]_ERR_CNT_CLR	RW	Receiver error counters clear button.
1	SLE_ RX_LANE[n]_ALIGN	R	The receiver channel is aligned to the pattern.

CoreSmartBERT Additional References

(Ask a Question)

- For updates and additional information about the software, devices, and hardware, visit the
- Intellectual Property pages on the Microchip FPGAs and PLDs website.

CoreSmartBERT Known Issues Workarounds (Ask a Question)

- There are no known limitations and workarounds for CoreSmartBERT v2.10.

Resolved Issues

(Ask a Question)

- The following table lists the issues that were resolved in the CoreSmartBERT releases.

Table 6-1. Resolved Issues

Version	Changes
2.10	Repackaged CoreSmartBERT with Transceiver Interface (PF_XCVR) IP v2.1.109
2.9	Added support for 10.3125 Gbps data rate
2.8	Repackaged CoreSmartBERT with PF_XCVR v2.1.101
2.7	12500 Mbps and 12700 Mbps data rates were removed from the CoreSmartBERT user interface
2.6	Repackaged CoreSmartBERT with support for PF_XCVR v2.0.110
2.5	Repackaged CoreSmartBERT with support for PF_XCVR v2.0.109
2.4	Repackaged CoreSmartBERT with support for PF_XCVR v2.0.107
2.3	Repackaged CoreSmartBERT with support for PF_XCVR v2.0.100
2.2	Repackaged CoreSmartBERT with support for PF_XCVR
2.0	Initial release

Revision History

(Ask a Question)

- The revision history describes the changes that were implemented in the document.
- The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	08/2023	The following is the list of changes in revision B of the document: • Updated for CoreSmartBERT v2.10. • Added 6. Resolved Issues section for all CoreSmartBERT IP versions.
A	07/2022	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template • Updated for CoreSmartBERT v2.9 • The document number was updated to DS50003362A from 50200788
9.0	03/2021	Updated for CoreSmartBERT v2.8
8.0	06/2020	Updated for CoreSmartBERT v2.7
7.0	03/2020	Updated for CoreSmartBERT v2.6
6.0	08/2019	Updated for CoreSmartBERT v2.5
5.0	03/2019	Updated for CoreSmartBERT v2.4
4.0	12/2018	Updated for CoreSmartBERT v2.3
3.0	08/2018	Updated for CoreSmartBERT v2.2
2.0	05/2018	Updated for CoreSmartBERT v2.1
1.0	08/2017	Initial release

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Documents / Resources

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