MICROCHIP Median Filter App User Guide

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Introduction

The Median Filter is a nonlinear digital filtering technique, often used to remove glitches from an analog signal.

The Median Filter is used to remove the noise from a signal. It forms a window of N (this IP supports N = 5, 7, and 9) adjacent samples and finds the median of these samples.

Examples:

- If N = 9 and {15, 13, 25, 18, 35, 46, 61, 26, 9} is a set of input samples, then median is 25
- If N = 7 and {12, 11, 27, 19, 9, 6, 3} is a set of input samples, then median is 11
- If N = 5 and {15, 15, 12, 11, 10} is a set of input samples, then median is 12

SummaryThe following table provides a summary of the Median filter characteristics.

Table 1. Median Filter Characteristics

Core Version	This document applies to Median Filter v4.2.
Supported DevicFamilies	• PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v11.8 or later releases.
Licensing	Complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout are performed with Libero software. Median Filter is licensed with encrypted RTL that must be purchased separately. For more information, see **Median Filter**.

Features

Median Filter has the following key features:

- Finds the median of a set of input samples
- Window sizes are adjustable (5, 7, and 9)

Implementation of IP Core in Libero Design Suite

IP core must be installed to the IP Catalog of the Libero SoC software. This is done automatically through the IP Catalog update function in the Libero SoC software, or the IP core is manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, the core is configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero project list.

Contents

Device Utilization and Performance

The following table lists the device utilization used for Median Filter.

Device Details			Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	Window Size	LUTs	DFF		LSRAM	µSRAM		
		Window-5	630	240	200	0	0	0	0
PolarFire® SoC	MPFS250T	Window-7	999	294	200	0	0	0	0
		Window-9	1161	384	200	0	0	0	0
		Window-5	630	240	200	0	0	0	0
PolarFire	MPF300T	Window-7	1067	294	200	0	0	0	0
		Window-9	1190	384	200	0	0	0	0
		Window-5	630	240	200	0	0	0	0
SmartFusion® 2	M2S150	Window-7	1084	294	200	0	0	0	0
		Window-9	1222	384	200	0	0	0	0

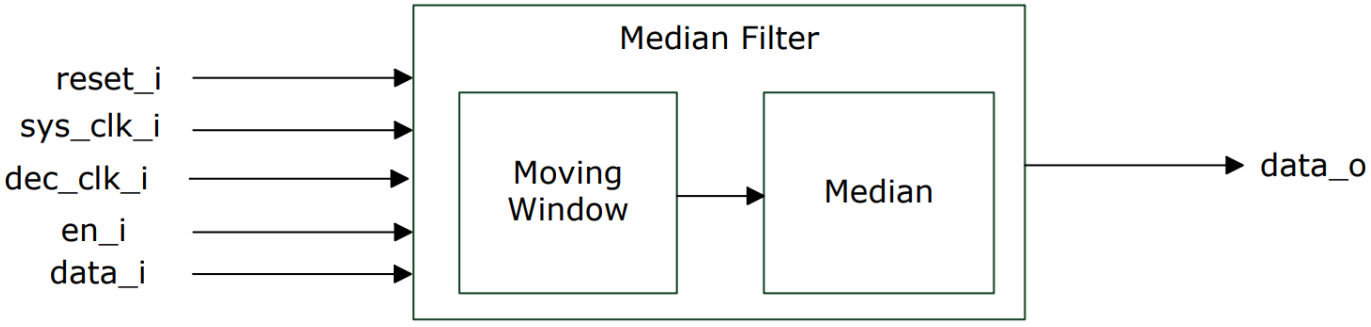
Important:

1. The data in this table is captured using typical synthesis and layout settings. CDR reference clock source was set to Dedicated with other configurator values unchanged.
2. Clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers

Functional Description

This section describes the implementation details of the Median Filter block. The following figure shows the system level block diagram of the Median Filter

Figure 1-1. System-Level Block Diagram of Median Filter



Moving Window

The input data is sampled at every rising edge of dec_clk_i. This submodule takes the input samples and creates windows of fixed length (5 or 7 or 9 samples each). The window size depends on the configuration parameter g_WINDOW_SIZE. If we consider g_WINDOW_SIZE as 7, then {1st, 2nd, 3rd, 4th, 5th, 6th, 7th} samples will form a window, {2nd, 3rd, 4th, 5th, 6th, 7th, 8th} samples will form the next window and so on. These windows are connected as the input to median submodule.

After the reset signal is de-asserted, the window will have all zeros. The input data_i is sampled at rising edge of dec_clk_i.

Median

The median submodule finds the median value of each window and gives it as the output. At every rising edge of dec_clk_i the median output is updated.

Median Filter Parameters and Interface Signals

This section discusses the parameters in the Median Filter GUI configurator and I/O signals.

Configuration Settings

The following table lists the description of the configuration parameters used in the hardware implementation of Median Filter. These are generic parameters and can be varied as per the requirement of the application.

Table 2-1. Configuration Parameters

Signal Name	Range	Description
g_WINDOW_SIZE	5, 7, 9	Describes the size of the window
g_DATA_WIDTH	—	Describes the input and output data width

Inputs and Outputs Signals (Ask a Question)

The following table lists the input and output ports of Median Filter.

Table 2-2. Inputs and Outputs of Median Filter

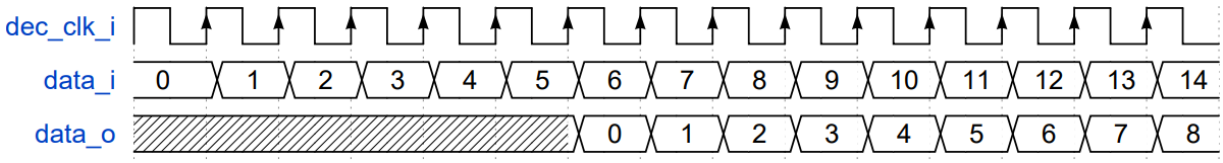
Signal Name	Direction	Width	Description
reset_i	Input	1bit	Active low asynchronous reset signal to design
sys_clk_i	Input	1bit	System clock
dec_clk_i	Input	1bit	Decimated clock input – data is sampled at the rising edge of this signal
en_i	Input	1bit	Enables signal
data_i	Input	g_DATA_WIDTH bits	Data input
data_o	Output	g_DATA_WIDTH bits	Median data output

Timing Diagrams

This section discusses Median Filter timing diagrams.

The following figure shows the timing diagram of Median Filter.

Figure 3-1. Median Filter Timing Diagram



After the reset signal is de-asserted, the window will have all zeros. The first input sample will enter the window at the first rising edge of dec_clk_i, the second sample will enter the window at the second rising edge of dec_clk_i and so on.

For the timing diagram shown in the above-mentioned figure, after the reset signal is de-asserted, the window will be {0,0,0,0,0,0,0,0,0}

At first rising edge of dec_clk_i , data_i is 0, the window will be{0,0,0,0,0,0,0,0,0}

At second rising edge of dec_clk_i,data_i is 1,the window will be{0,0,0,0,0,0,0,0,1}

At third rising edge of dec_clk_i,data_i is 2,the window will be{0,0,0,0,0,0,0,0,1,2} and so on.

Testbench

A unified test-bench is used to verify and test Median Filter called as user test-bench. Testbench is provided to check the functionality of the Median Filter IP

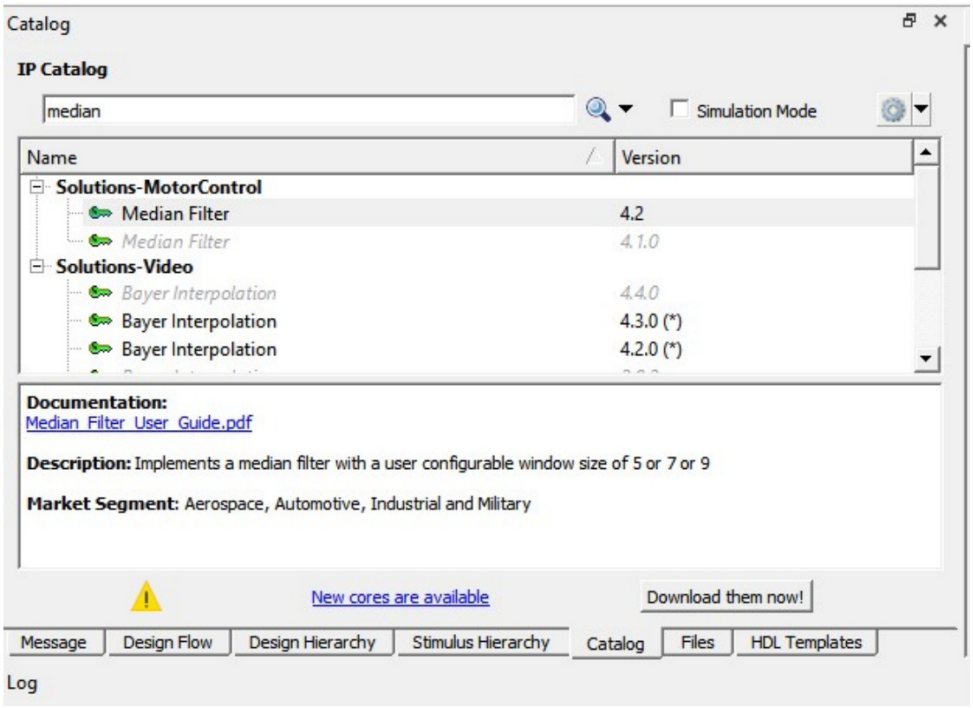
Simulation

The following steps describe how to simulate the core using the testbench:

1. Open the Libero SoC application, click Libero SoC Catalog tab, expand Solutions-MotorControl
2. Double-click Median Filter, and then click OK. The documentation associated with the IP are listed under Documentation

Important: If you do not see the Catalog tab, navigate to View Windows menu and click Catalog to make it visible.

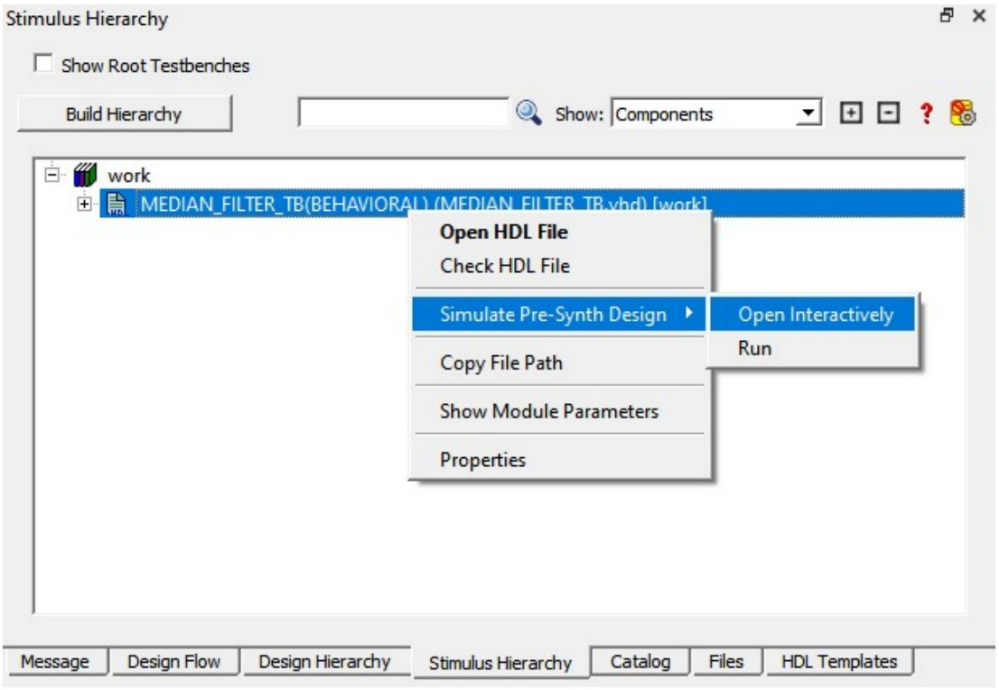
Figure 4-2. Simulating Pre-Synthesis Design



3. On the Stimulus Hierarchy tab, right-click testbench (median_filter_tb.v), point to Simulate Pre-Synth Design , and then click Open Interactively.

Important: If you do not see the Stimulus Hierarchy tab, navigate to View > Windows menu and click Stimulus Hierarchy to make it visible.

Figure 4-2. Simulating Pre-Synthesis Design



Important: If the simulation is interrupted due to the runtime limit specified in the .do file, use the run -all command to complete the simulation.

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	03/2023	The following is the list of changes in revision A of the document: • Migrated the document to the Microchip template. • Updated the document number to DS50003502A from 50200845. • Added 3. Timing Diagrams. • Added 4. Testbench.
1.0	11/2018	Revision 1.0 was the first publication of this document.

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