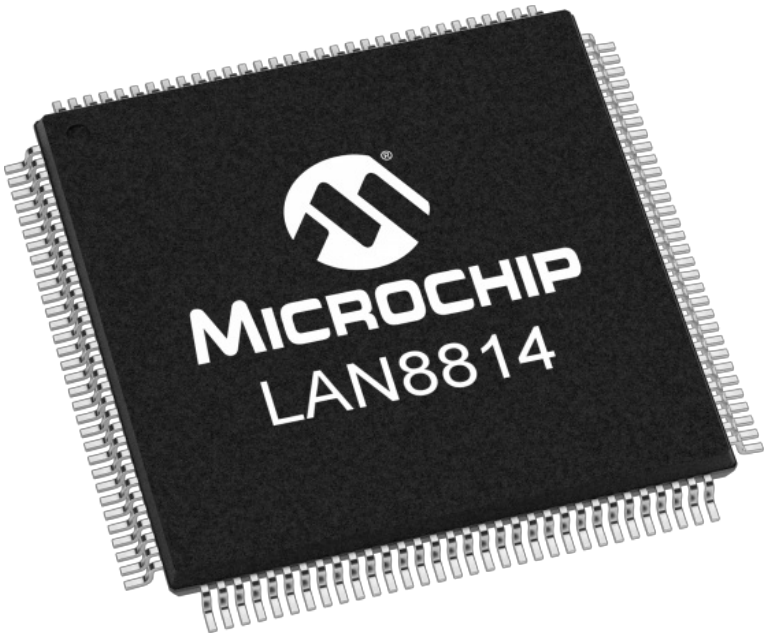
Manuals+ — User Manuals Simplified.

MICROCHIP LAN8814 Hardware Design Checklist User Guide

Contents

MICROCHIP LAN8814 Hardware Design Checklist



INTRODUCTION

This document provides a hardware design checklist for the Microchip LAN8814 product family. It is meant to help cus-tomers achieve first-pass design success. These checklist items should be followed when utilizing the LAN8814 in a new design. A summary of these items is provided in Section 11.0, “Hardware Checklist Summary”. Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, “General Considerations”
- Section 3.0, “Power”
- Section 4.0, “Twisted Pair Media Interface”
- Section 5.0, “QSGMII/Q-USGMII MAC Interface”
- Section 6.0, “Device Clocks”
- Section 7.0, “Media Recovered Clock Output”
- Section 8.0, “1588 Support”
- Section 9.0, “Digital Interface and I/O”
- Section 10.0, “Miscellaneous”

GENERAL CONSIDERATIONS

Required References

The LAN8814 implementor should have the following documents on hand:

- LAN8814 4-Port Gigabit Ethernet Transceiver with QSGMII/Q-USGMII, IEEE 1588, SyncE and TSN Support Data Sheet
- LAN8814 EVB documents, including the schematics, PCB file, BOM, etc at **www.microcip.com**.

Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and the RJ45 connector at line side for better EMI and ESD.

POWER

Table 3-1 shows the power supply pins for LAN8814.

Name	Pin	Description	Comments
+2.5/3.3V Analog I/O Power Supply	VDDAH 4 VDDAH_P[3:0] 113, 100, 24, 11 VDDAH_SERDES 49, 51 VDDAH_PLL_PTP 65 VDDAH_ABPVT 66	+2.5/3.3V analog I/O power supply	Power
+2.5/3.3V Analog Power Supply	VDD33REF 3	+2.5/3.3V analog power supply	Power
+1.1V Analog Power Sup- ply	VDDAL_ADC_A_P[3:0] 109, 96, 20, 7 VDDAL_ADC_B_P[3:0] 110, 97, 21, 8 VDDAL_ADC_C_P[3:0] 116, 103, 27, 14 VDDAL_ADC_D_P[3:0] 117, 104, 28, 15 VDDAL_PLL 1 VDDAL_SERDES 43 VDDTXL_SERDES 46 VDDAL_CK125 41, 121	+1.1V analog power supply	Power

+3.3/2.5/1.8V Variable I/O Power Supply Input	VDDIO 53, 59, 64, 71, 76, 87, 93 VDDIO_1 34	+3.3/2.5/1.8V variable I/O digital power supply input	Power
+1.1V Digital Core Power Supply Input	VDDCORE 39, 54, 63, 81, 124	+1.1V digital core power supply input	Power
Paddle Ground	P_VSS	Common ground. This exposed paddle must be connected to the ground plane with a via array.	GND
Ground	VSS_CK125 40, 120	Ground	GND

Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support the current require-ments specified for each power rail in the power consumption section of the device data sheet. (See the LAN8814 Data Sheet for the different system configurations.)
- The Operational Characteristics section of the LAN8814 Data Sheet contains the details of the power consump-tion of the device as measured during different modes of operation at various operating voltages. Power dissipa-tion is impacted by temperature, supply voltage, and external source/sink requirements.
- All worst-case measurements were taken at +6% power supply and +125°C case temperature. Refer to Table 6-4, Table 6-5, and Table 6-6 in the LAN8814 Data Sheet.
- Power consumption data is split into Table 6-1, Table 6-2, and Table 6-3 in the LAN8814 Data Sheet for typical operation and Table 6-4, Table 6-5, and Table 6-6 in the LAN8814 Data Sheet for worst-case operation (listed as VDDCore, VDDAL_x, and VDDIO_x).
- **Four-port Operation:**
  - Four Port (1.17V, 3.5V, and 3.5V) Power Consumption
  - Four Port (1.17V, 2.65V, and 2.65V) Power Consumption
  - Four Port (1.17V, 2.65V, and 1.91V) Power Consumption

Power Supply Planes
The LAN8814 integrates an optional LDO controller to be used with an external P-channel MOSFET when generating the 1.1V supply from an existing 2.5V or 3.3V source. Using the LDO controller and MOSFET is not required. An external 1.1V supply can be alternatively utilized.

MOSFET SELECTION

- The most important minimum PCB design and layout requirements or considerations for MOSFET selection are the:
    - P-channel
    - 500 mA continuous current
    - 3.3V or 2.5V source – input voltage
    - 1.1V drain – output voltage
- The VGS for the MOSFET must be operating in the constant current saturated region and not towards the thresh-old voltage for the cut-off region of the MOSFET, VGS(th).
- A 220 µF electrolytic capacitor between 1.1V and ground is required for proper LDO operation.

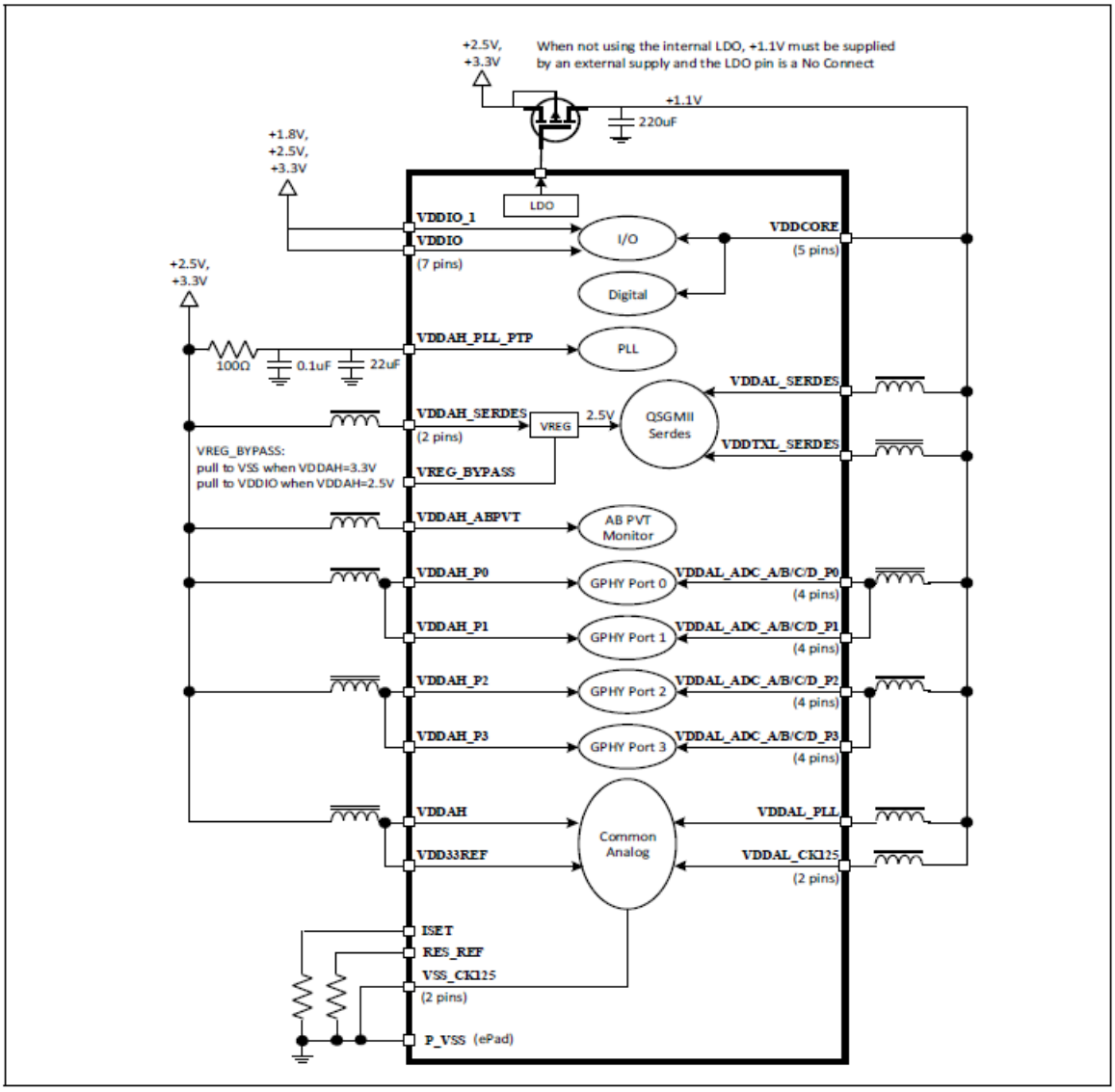
LDO DISABLE

The LDO controller is enabled by default. It may be alternatively disabled via internal register settings. An external source of 1.1V is necessary if the LDO is disabled.

Power Circuit Connection and Analog Power Plane Filtering

- Refer to Figure 3-1, which shows the power and ground connections for LAN8814.
- The 1.1 V power rail is not optional. However, the user has the option to select either 2.5V or 3.3V power rail. The filtered analog 1.1V and 2.5V or 3.3V supplies should not be shorted to any other digital supply at the package or PCB level.
- The most important PCB design and layout considerations are as follows:
    - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
    - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
    - Minimize resistive drop while efficiently conducting away heat from the device using 1 oz copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent ran-dom system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power the pins of the device with correctly positioned local decoupling.
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.
    - A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
    - Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.

POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



Bulk Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and be placed as close as possible to every LAN8814 power pin.
- Make sure that bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail of the power supply.

TWISTED PAIR MEDIA INTERFACE

10/100/1000 Mbps Interface Connection
The LAN8814 has four GPHY ports from PHY 0 to PHY 3 for Port 1, Port 2, Port 3, and Port 4. Detailed pin numbers from PHY 0 to PHY 3 sequence and descriptions as follows:

- **TX_RXP_A_[0:3] (pins 5, 18, 94, 107):** These pins are the transmit/receive positive (+) connection from Pair A of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TX_RXN_A_[0:3] (pins 6, 19, 95, 108):** These pins are the transmit/receive negative (–) connection from Pair A of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TX_RXP_B_[0:3] (pins 9, 22, 98, 111)** : These pins are the transmit/receive positive (+) connection from Pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and

bias are needed.

- **TX_RXN_B_[0:3] (pins 10, 23, 99, 112):** These pins are the transmit/receive negative (–) connection from Pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TX_RXP_C_[0:3] (pins 12, 25, 101, 114):** These pins are the transmit/receive positive (+) connection from Pair C of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TX_RXN_C_[0:3] (pins 13, 26, 102, 115):** These pins are the transmit/receive negative (–) connection from Pair C of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TX_RXP_D_[0:3] (pins 16, 29, 105, 118):** These pins are the transmit/receive positive (+) connection from Pair D of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TX_RXN_D_[0:3] (pins 17, 30, 106, 119):** These pins are the transmit/receive positive (+) connection from pair D of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.

Magnetics Connection and RJ45 Connection

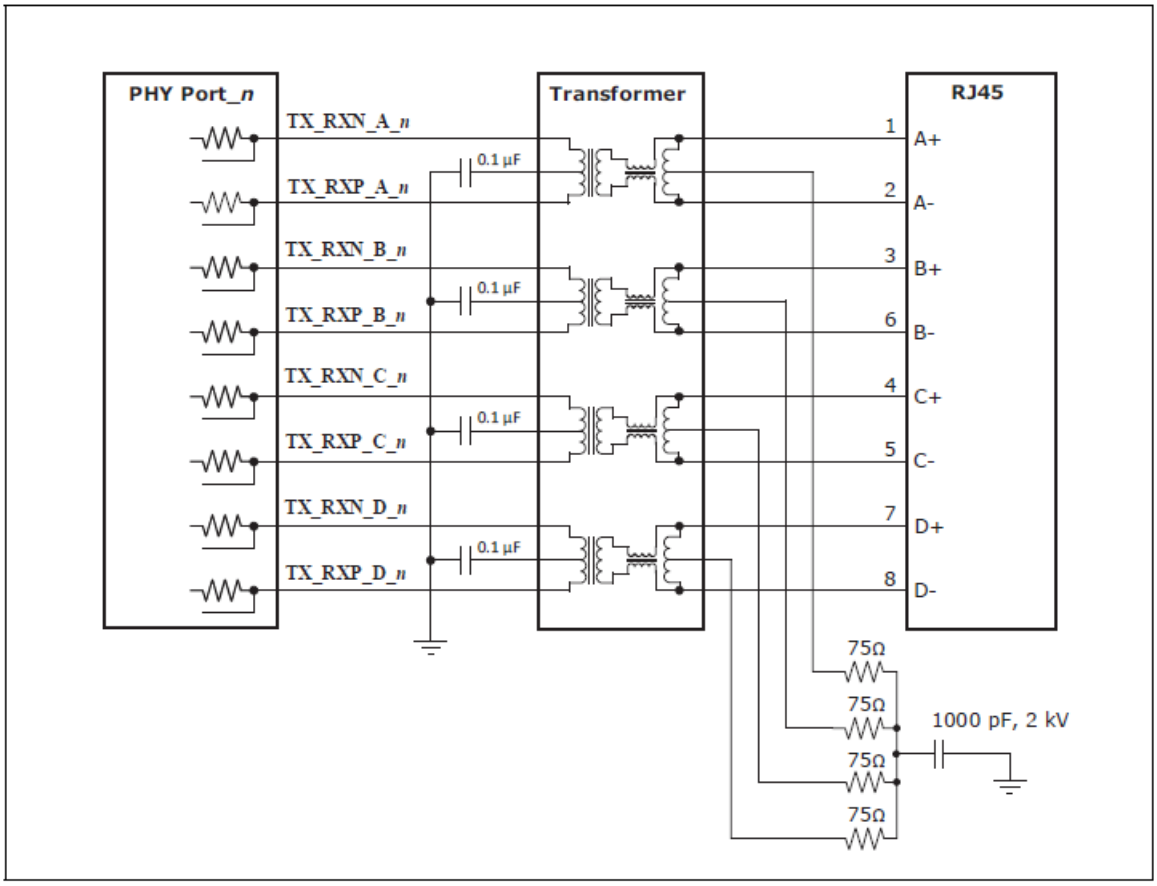
- The center tap connection on the LAN8814 side for Pair A channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the LAN8814 side for Pair B channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the LAN8814 side for Pair C channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the LAN8814 side for Pair D channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center taps of the magnetics of all four pairs are recommended to be isolated with separate 0.1 µF capacitors to ground. The reason is the common-mode voltage can be different between pairs, especially for 10/100 opera-tion. (Pairs A and B are active, while Pairs C and D are inactive.) However, for integrated connector magnetics with ganged center taps, a workaround script to address this analog front-end limitation is available in the soft-ware. See LAN8814 Errata.
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to the chassis ground.
- Only one 1000 pF, 2 kV capacitor to the chassis ground is required for each PHY. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2 kV capacitor or a ferrite bead to be connected between the chassis ground and the system ground is required. It is shared by PHY 0, PHY 1, PHY 2, and PHY 3 for Port 1, Port 2, Port 3, and Port 4.
- The RJ45 shield should connect to the chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 4.3, “PCB Layout Considerations” for guidance on how the chassis ground should be cre-ated from system ground.

PCB Layout Considerations

- All differential pairs of the MDI interface traces should have a characteristic impedance of 100Ω to the GND plane. This is a strict requirement to minimize return loss. This requirement is placed upon the PCB Designer and the FAB house.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI and crosstalk. Each port of pairs A, B, C, and D should match in length to prevent delay mismatch that would cause common-mode noise.
- Ideally, there should be no crossover or via on the signal paths.
- Incorporate a 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor or ferrite bead far away from the LAN8814 device or other sensitive devices in the PCB layout placement for better ESD.

Ethernet Media Interface
Figure 4-1 illustrates the device Ethernet media interface connections. Note that the device supports integrated connec-tor magnetics with ganged center taps.

ETHERNET MEDIA INTERFACE CONNECTIONS



QSGMII/Q-USGMII MAC INTERFACE

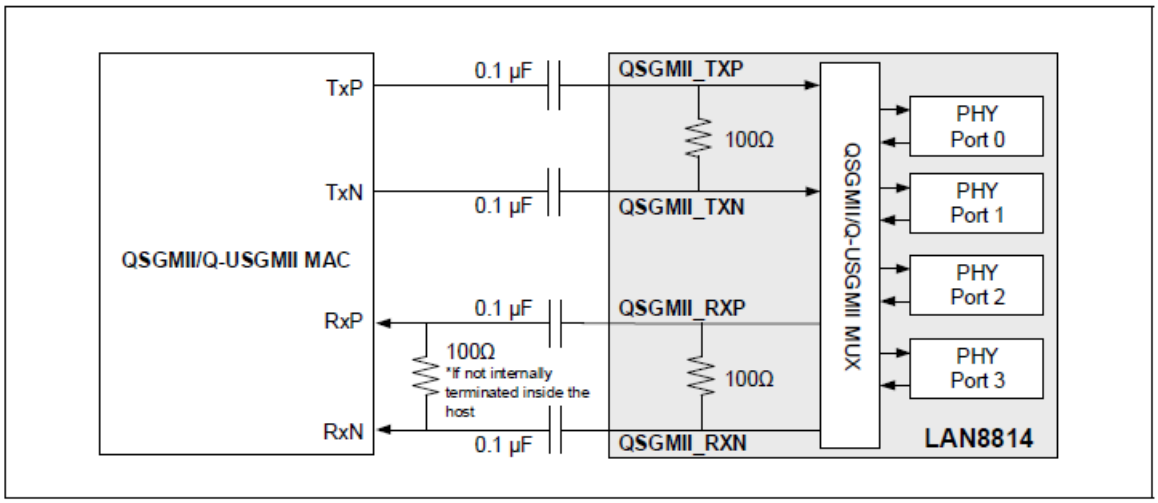
- The LAN8814 device supports QSGMII/Q-USGMII MAC interface to convey four ports of network data and port speeds of 10/100/1000 Mbps.
- Detailed pin numbers and pin descriptions of the QSGMII MAC interface are described in the following subsec-tions. Figure 5-1 shows the device QSGMII/Q-USGMII MAC interface connections.

QSGMII/Q-USGMII Pins and Connection
The LAN8814 supports the QSGMII/Q-USGMII MAC interface to convey four GPHY ports from PHY 0 to PHY 3. Detailed pin numbers and descriptions on the QSGMII MAC Interface are as follows:

- **QSGMII_TXP (pin 47):** This pin is the transmit positive (+) signal connection for a differential pair for QSGMII/Q-USGMII Transmitter Output Positive.
- **QSGMII_TXN (pin 45):** This pin is the transmit negative (–) signal connection for a differential pair for QSGMII/Q-USGMII Transmitter Output Negative.
- **QSGMII_RXP (pin 42):** This pin is the receive positive (+) signal connection for a differential pair for QSGMII/Q-USGMII Transmitter Input Positive.
- **QSGMII_RXN (pin 44):** This pin is the receive negative (–) signal connection for a differential pair for QSGMII/Q-USGMII Transmitter Input Negative.
- **REF_PAD_CLK_P (pin 50):** This is the positive (+) signal connection of differential pair for QSGMII/Q-USGMII External Reference Clock Input Positive.
- **REF_PAD_CLK_M (pin 48):** This is the negative (–) signal connection of differential pair for QSGMII/Q-USGMII External Reference Clock Input Negative.

QSGMII MAC
The LAN8814 device supports a QSGMII MAC to convey four ports of network data and port speed from 10/100/1000 Mbps. If the QSGMII MAC which the LAN8814 is connecting to support this functionality configures the device for QSGMII MAC mode, set register 19G, bits 15:14 = 01. In addition, set register 18G as desired.

QSGMII MAC INTERFACE CONNECTIONS



QSGMII MAC Design Rules

- Use AC coupling with 0.1 µF capacitors for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or strip-line).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce crosstalk

between differential pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.

DEVICE CLOCKS

Reference Clock
The device reference clock supports both 25 MHz and 125 MHz clock signals. The 1588 differential input clock supports frequencies of 10 MHz, 25 MHz, and 125 MHz. Both reference clocks can be either differential or single-ended. If dif-ferential, they must be capacitively coupled and LVDS compatible.

System Clock and Synchronous Ethernet Connections
The LAN8814 system reference clock supports a crystal input/system reference clock input interface with the following pin details:

- **XI (pin 128):** Crystal Input/System Reference Clock Input. When using a 25 MHz crystal, this input is connected to one lead of the crystal. Refer to REF_CLK_SEL[1:0] for additional information. When using a 25 MHz system ref-erence clock, this is the input from the external 25 MHz oscillator.
- **XO (pin 127):** Crystal Output. When using a 25 MHz crystal, this output is connected to one lead of the crystal. Refer to REF_CLK_SEL[1:0] for additional information. When using a 25 MHz system reference clock source, this pin is not connected.
- **CK125_REF_INP (pin 123):** System Reference Clock Input Positive. This pin is the positive (+) signal connection of a differential pair. When using a 125 MHz system reference clock source, this is connected to the 125 MHz external oscillator. Refer to REF_CLK_SEL[1:0] for additional information.
- **CK125_REF_INM (pin 122):** System Reference Clock Input Negative. This pin is the negative (–) signal connec-tion of a differential pair. When using a 125 MHz system reference clock source, this is connected to the 125 MHz external oscillator. Refer to REF_CLK_SEL[1:0] for additional information.
- **CK25OUT (pin 126):** System Clock Output. Buffered copy of the internal 25 MHz reference clock. This output clock is powered by VDDAH.

When reference clocks are used, ensure that:

- The jitter requirements in the LAN8814 Data Sheet are met.
- The traces are routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- AC coupling with 0.1 µF capacitors is used. Capacitors are best placed close to the reference clock input pins.
- For some clock drivers, the termination resistors are placed on the clock driver side. Termination resistors are not typically needed on the LAN8814 side of the capacitors.
- All reference clocks must be free from glitches or must be hitless.
- Unused reference clocks can be left floating (No Connect).

Single-Ended REFCLK Input
To use a single-ended reference clock, an external resistor (Rs) is required. The purpose of the Rs is to limit the drain on the oscillator output. The configurations for a single-ended REFCLK are referenced to VDDAH in accordance with the diagram on power connections in Figure 3-1. The ICLK Type Input Buffer’s non-variable I/O

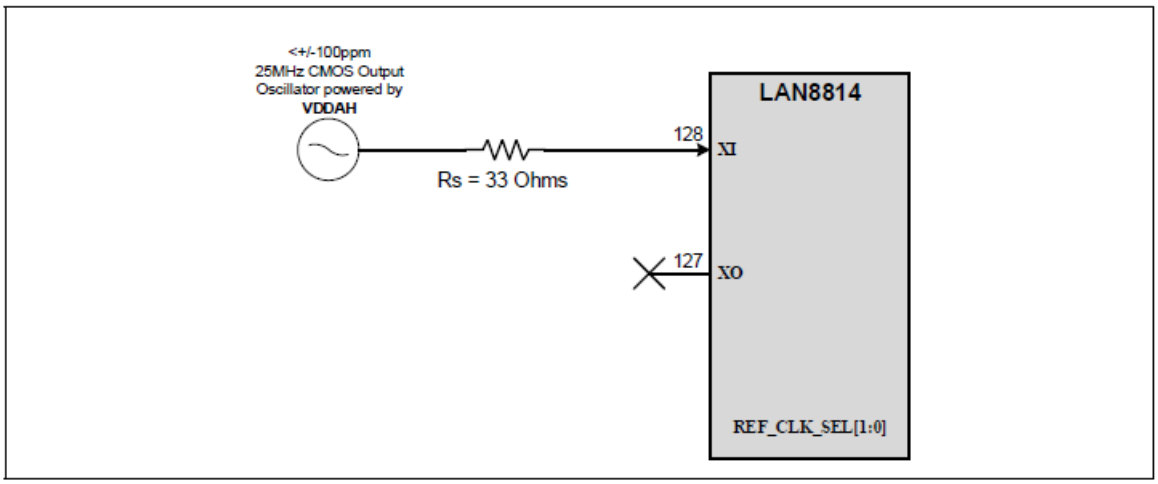
DC electrical characteristics are specified in Table 6-1 and the Single-Ended REFCLK Input diagram is shown in Figure 6-1.

TABLE 6-1: ICLK TYPE INPUT BUFFER NON-VARIABLE I/O DC ELECTRICAL CHARACTERISTICS

ICLK Type Input Buffer	Symbol	Minimum	Maximum	Unit	Note
Low Input Level	VIL	—	0.5	V	
High Input Level	VIH	2.0	—	V	Note 1
Input Leakage	IIH	–10	10	µA	

Note 1: XI can optionally be driven from a 25 MHz single-ended clock oscillator to which these specifications apply.

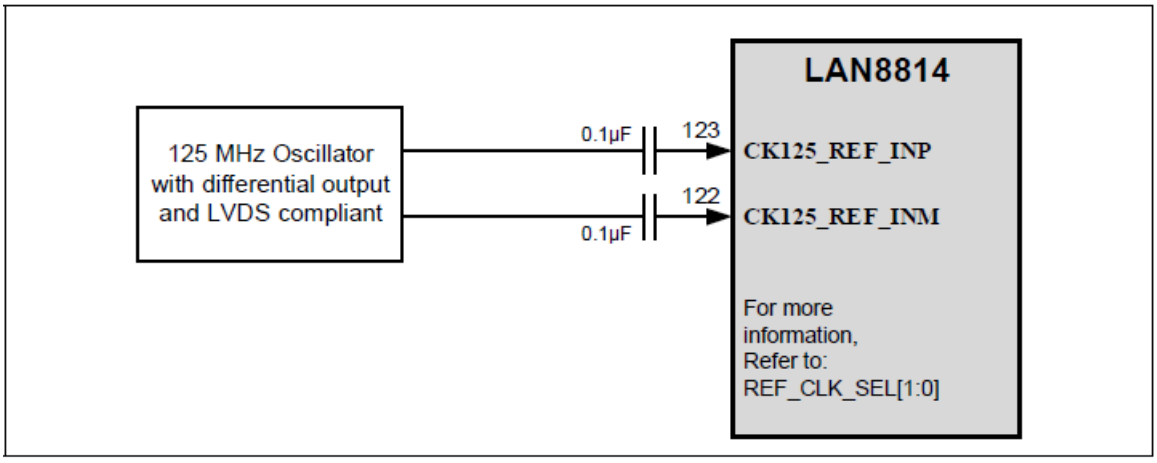
SINGLE-ENDED REFCLK INPUT



Differential REFCLK Input

AC coupling is required when using a differential REFCLK. Differential clocks must be capacitively coupled and LVDS compatible. Figure 6-2 shows the configuration.

AC COUPLING FOR REFCLK DIFFERENTIAL INPUT



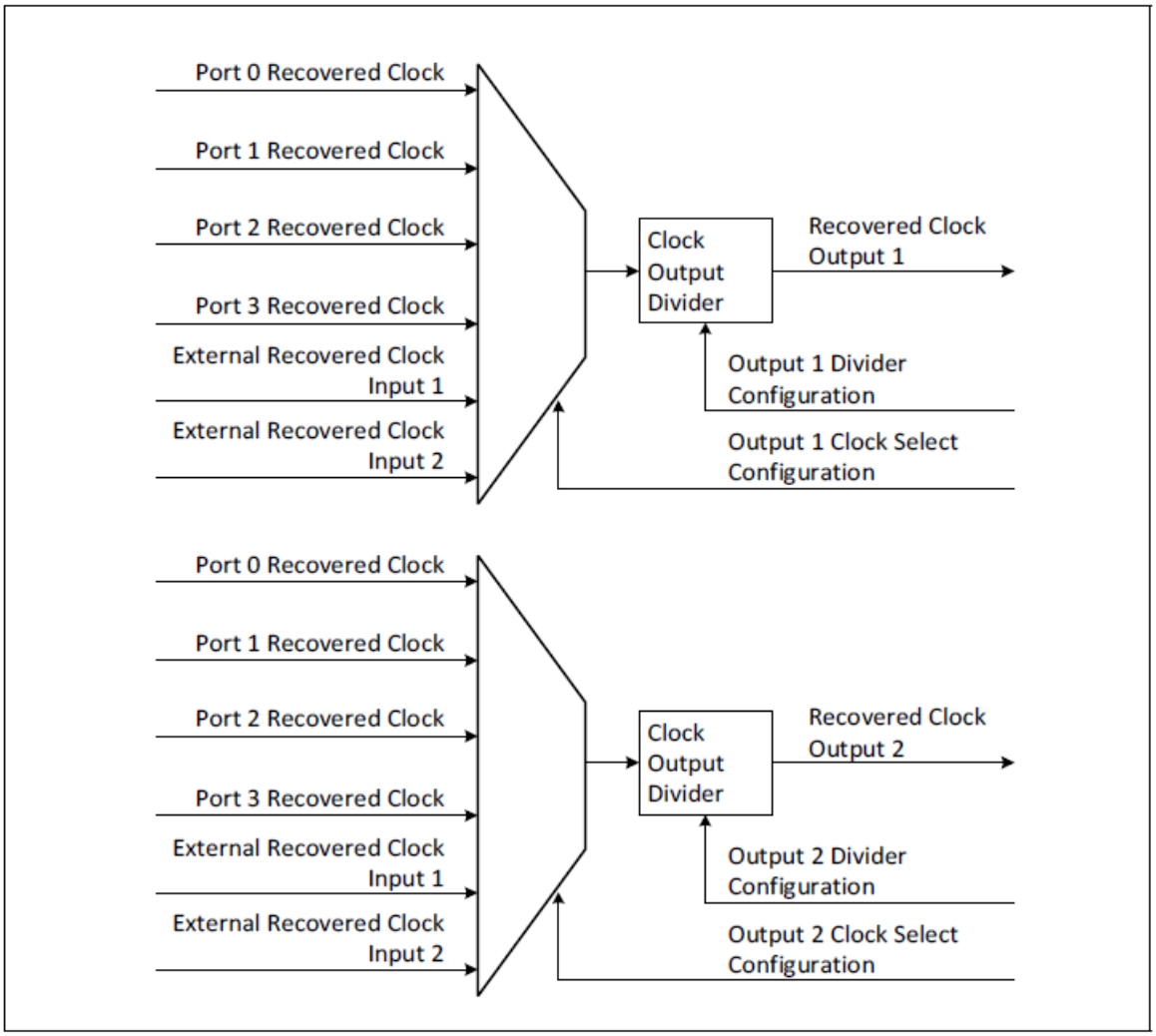
MEDIA RECOVERED CLOCK OUTPUT

For Synchronous Ethernet applications, the LAN8814 includes two recovered clock output pins and two recovered clock input pins.

- **RCVRD_CLK_OUT1 (pin 79):** Recovered Clock Output 1 (GPIO_9/TCK). Recovered Clock Output 2.5 MHz, 25 MHz, or 125 MHz. This pin can be configured to always output 2.5 MHz regardless of PHY speed.
- **RCVRD_CLK_OUT2 (pin 80):** Recovered Clock Output 2 (GPIO_10/TMS). Recovered Clock Output 2.5 MHz, 25 MHz, or 125 MHz. This pin can be configured to always output 2.5 MHz regardless of PHY speed.
- **RCVRD_CLK_IN1 (pin 77):** Recovered Clock Input 1 (GPIO_7/TDI). Recovered Clock Input 2.5 MHz, 25 MHz, or 125 MHz.
- **RCVRD_CLK_IN2 (pin 78):** Recovered Clock Input 2(GPIO_8/TDO). Recovered Clock Input 2.5 MHz, 25 MHz, or 125 MHz.

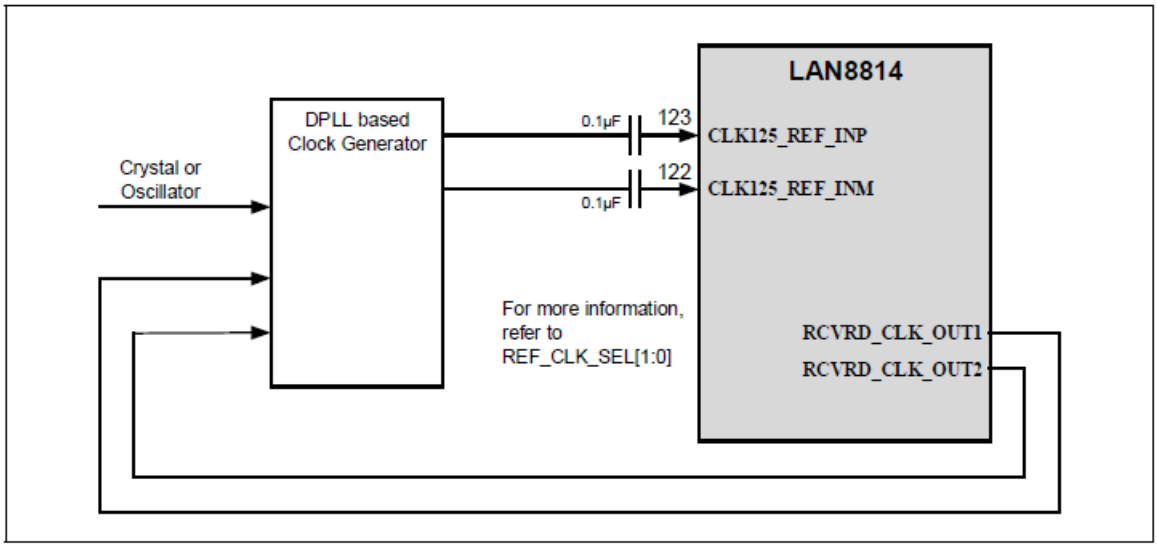
Refer to Figure 7-1 for the functional diagram of the RCVRD_CLK_OUT output operation which indicates the recovered clock options available.

SYNCE-RECOVERED CLOCK OUTPUTS

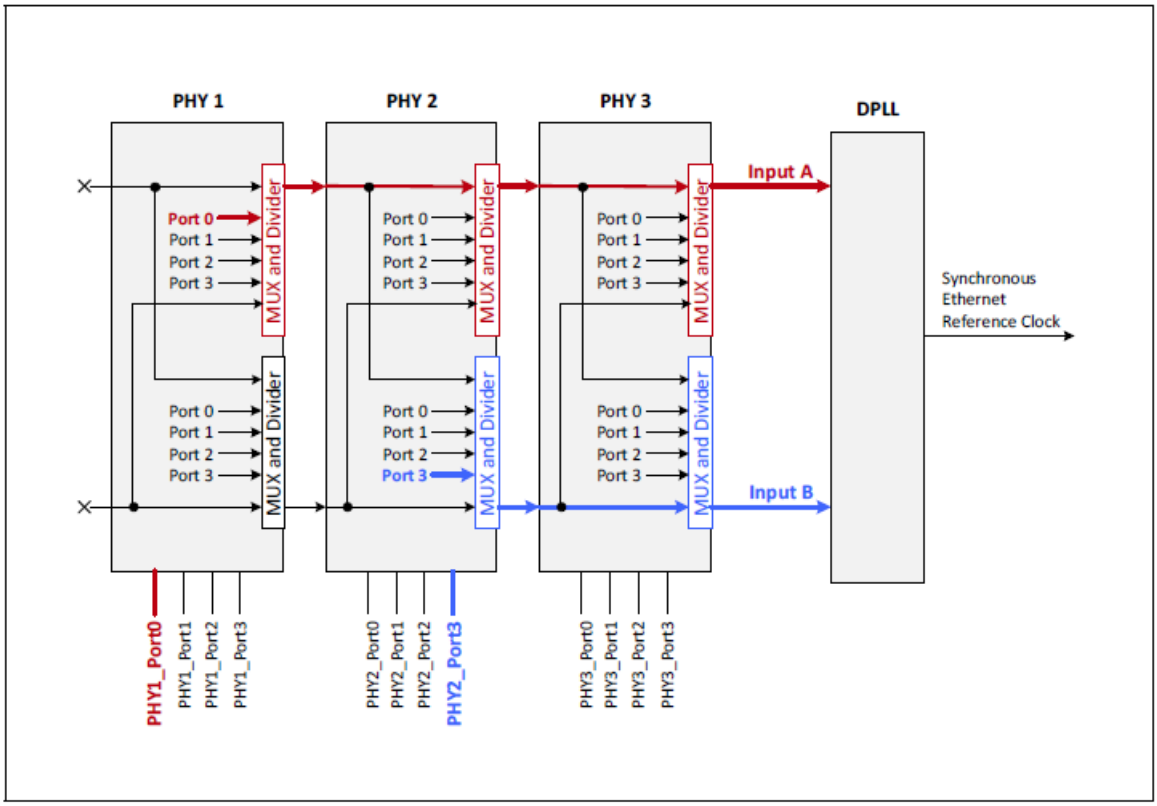


Refer to Figure 7-2 and Figure 7-3 when using Synchronous Ethernet applications.

TYPICAL SYNCHRONOUS ETHERNET CLOCK CONFIGURATION



SYNCHRONOUS ETHERNET RECOVERED CLOCK DAISY-CHAINING



1588 SUPPORT

IEEE 1588 Pin Connections

The LAN8814 supports IEEE-1588 Timestamping functionality. This functionality is present in and only applies to the device. The IEEE-1588 Timestamping functionality is not available or applicable to the LAN8804. The hardware interface to the IEEE-1588 Timestamping block is shown in Table 8-1.

IEEE-1588 TIMESTAMP HARDWARE INTERFACE

GPIO	Pin#	Alternate Function	Description
GPIO0	68	1588_EVENT_A	1588 LTC Event A
GPIO1	69	1588_EVENT_B	1588 LTC Event B
GPIO2	70	1588_REF_CLK	1588 Reference Clock Input
GPIO3	72	1588_LD_ADJ	1588 Load/Adjust Input
GPIO4	73	1588_STI_CS_N	1588 Serial Timestamp Interface Chip Select
GPIO5	74	1588_STI_CLK	1588 Serial Timestamp Interface Clock Output
GPIO6	75	1588_STI_DO	1588 Serial Timestamp Interface Data Output

- **1588_LD_ADJ (pin 72):** 1588 Load/Adjust Input pin. This input controls loading and adjusting of the 1588 LTC. This pin is shared with other functions.
- **1588_REF_CLK (pin 70):** 1588 Reference Clock Input. Freq: 10, 25, or 125 MHz. This input optionally supports ePPS format, where the PPS is combined with the clock. This pin is shared with other functions.
- **1588_STI_CLK (pin 74):** 1588 Serial Timestamp Interface Clock Output. This pin is shared with other functions.
- **1588_STI_CS_N (pin 73):** 1588 Serial Timestamp Interface Chip Select. This pin is shared with other functions.
- **1588_STI_DO (pin 75)**: 1588 Serial Timestamp Interface Data Output. This pin is shared with other functions.
- **1588_EVENT_A (pin 68):** 1588 LTC Event A. When asserted, this pin signals that 1588 LTC Event A has occurred. This pin can also be configured to provide a PPS Output signal. This pin is shared with other functions.
- **1588_EVENT_B (pin 69)**: 1588 LTC Event B. When asserted, this pin signals that 1588 LTC Event B has occurred. This pin can also be configured to provide a PPS Output signal. This pin is shared with other functions.
- The default configuration of the 1588_REF_CLK pin sets the device to use an internal clock for the Local Time Counter (LTC). Refer to EP4, Reg 514, bits 12:10 which control the reference clock source. The default value of EP4.514 bits 12:10 is 000 (125 MHz clock from internal System PLL). To enable an external clock source, Reg EP4.514, bits 12:10 would need to be changed and set to 010 = External 1588_REF_CLK (can be 10 MHz, 25 MHz, or 125 MHz).
- The local time counter keeps the local time for the device and the time is monitored and synchronized to an exter-nal reference by the CPU. The source clock for the counter is selected externally to be 10 MHz, 25 MHz, and 125 MHz. The clock may also be a line clock or the dedicated 1588_REF_CLK pins. This clock source is selected in register. EP4.514, bits 12:10 have the following options for Reference Clock Source [12:10]:
  - 000 = 125 MHz clock from internal System PLL
  - 001 = 125 MHz QSGMII recovered clock
  - 010 = External 1588_REF_CLK (can be 10 MHz, 25 MHz, or 125 MHz)

    - 011 = RESERVED
    - 100 = Recovered clock from Port 0 Rx (can be 25 MHz or 125 MHz)
    - 101 = Recovered clock from Port 1 Rx (can be 25 MHz or 125 MHz)
    - 110 = Recovered clock from Port 2 Rx (can be 25 MHz or 125 MHz)
    - 111 = Recovered clock from Port 3 Rx (can be 25 MHz or 125 MHz)
- Please be aware that when the link drops while using the Recovered Clock Options, it will result in NO 1588 Ref Clock that causes undesired behavior.

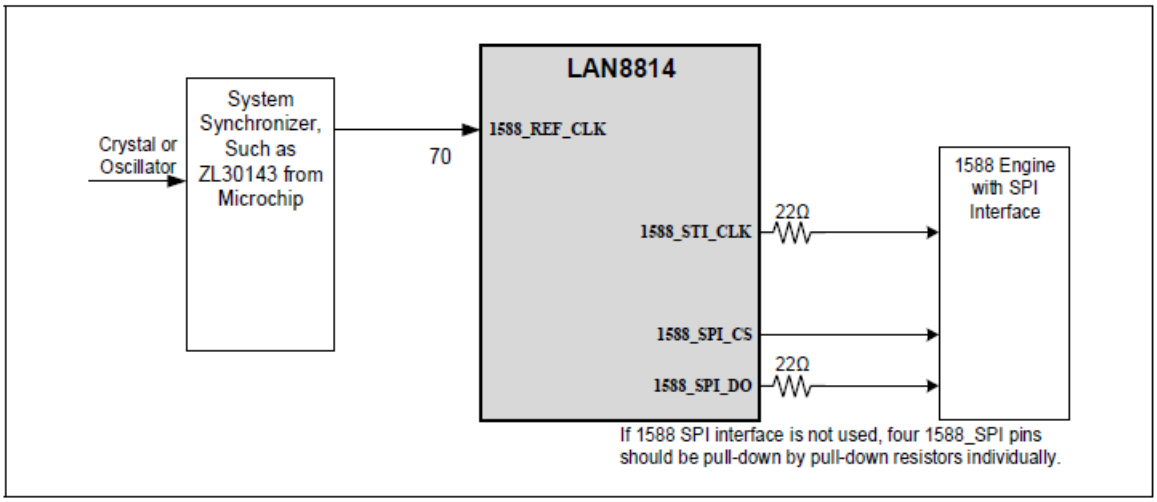
1588 Serial Timestamp Interface

- The format of the 1588 Serial Timestamp Interface is detailed in Section 6.6.13, “1588 Serial Timestamp Interface (STI) Format and Timing” of the LAN8814 Data Sheet.
- The 1588 Serial Timestamp Interface is configurable as follows:
    - 1588_STI_CLK pin frequency is configurable between 13.89 MHz and 62.5 MHz, based on dividing the sys-tem 125 MHz clock by integer values between [2, 8]. This is configured in Register EP4.768. It is also config-urable to the 1588_STI_DO clock output based on rising or falling edge.
    - Number of 1588_STI_CLK periods (1588_STI_CS_N deasserted) between consecutive timestamp outputs.
    - Number of 1588_STI_CLKs between 1588_STI_CS_N assertion and first valid bit of 1588_STI_DO.
- When setting the Enable/Disable of the 1588 STI, egress timestamps and signatures may either be read by soft-ware from internal registers (1588 STI Disabled), or pushed off-chip via the 1588 STI (1588 STI Enabled).
- The ePPS format is detailed in the Section 6.6.10, “1588_REF_CLK Reference Clock Timing” of the LAN8814 Data Sheet.
- To use external 1588 Interface pins, they must be enabled as GPIOs and GPIO Alternate Functions. GPIO Buffer Type and GPIO Direction must also be set appropriately.
- Refer to Table 8-2 and Figure 8-1 for additional pins and using the 1588 serial timestamp interface.

SERIAL TIMESTAMP INTERFACE PINS

Pin Name	Pin Number	Type	Description
GPIO5/1588_STI_CLK	74	I/O, PU	1588 SPI clock
GPIO4/1588_STI_CS	73	I/O,PU	1588 SPI chip select
GPIO6/1588_STI_DO	75	I/O, PU	1588 SPI data output

1588 DIFFERENTIAL CLOCK AND 1588 SPI CONFIGURATION



DIGITAL INTERFACE AND I/O

MIIM (MDIO) Interface

- The LAN8814 device supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the device. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification[1].
- **The MIIM interface consists of the following:**
  - A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
  - A specific protocol that operates across the physical connection which allows an external controller to com-municate with one or more devices. Each device is assigned a unique PHY address between 0h and 1Fh by the PHYAD[4:0] strapping pins.
  - **ALLPHYAD: (pin 68):** GPIO0/1588_EVENT_A/ALLPHYAD – The ALLPHYAD configuration strap sets the default of the All-PHYAD Enable bit in the Common Control register which enables (pulled-down) or disables (pulled-up) the PHY's ability to respond to PHY Address 0 as well as its assigned PHY address.
  - **PHYAD0: (pin 84)**: GPIO12/PORT0LED2/PHYAD0/PORT0_LED2_POL
  - **PHYAD1: (pin 85):** GPIO13/PORT3LED1/PHYAD1/PORT3_LED1_POL
  - **PHYAD2: (pin 86):** GPIO14/PORT3LED2/PHYAD2/PORT3_LED2_POL
  - **PHYAD3: (pin 88):** GPIO15/SOF0/PHYAD3
  - **PHYAD4: (pin 89):** GPIO16/SOF2/PHYAD4
- The ALLPHYAD strap input is inverted as compared to the Register bit value.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indi-rect access to MMD addresses and registers.
- ALL PHYS ADDRESS. Typically, the Ethernet PHYs are accessed at the PHY addresses set by the PHYAD[4:0] strapping pins. PHY Address 0h is optionally supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set the Basic Control register to a value of 0x1940 to set bit[11] to a value of one to enable software power-down).
- PHY Address 0 is enabled (in addition to the PHY address set by the PHYAD[4:0] strapping pins) when the All-PHYAD Enable bit in the Common Control register is set to '1'. The ALLPHYAD configuration strap can also be

used to set the default of the All-PHYAD Enable bit.

- The MDIO Output Pin Drive mode is controlled by two bits defined in EP4.5 and Reg17:
  - the MDIO Buffer Type bit in the Output Control register (EP4.5 – bit 15 for port 0)
  - the test_a1_a2_en_bit (Reg17 – bit 9 for each port of the PHY)
- When set to a '0', the MDIO output is open-drain. When set to '1', the MDIO output is push-pull. To configure MDIO output for push-pull, write a value of 0x8000 on Port 0 to Register EP4.5 (sets bit 15). For each port, write a value of 0x02f4 to Register 17 which sets bit 9 on all ports.

Note: The MDIO pin can only be connected with other Clause 22 MIIM Targets. Connecting any Clause 45 Targets, such as a 10G PHY, will cause undesirable behavior.

GPIO Pins

- The General Purpose I/Os (GPIOs) consist of 24 programmable input/output pins that are shared with other pins.
- These pins are individually configurable via the GPIO registers.
- Extreme care must be taken on strap input pins that may be used for General Purpose Inputs. The General Pur-pose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.
- Many GPIOs have the ability to be used as an alternate function. Once enabled as a GPIO, the alternate function is selected by the bits in the GPIO Alternate Function Select Registers. The alternate function buffer type is still selected via the GPIO Buffer Type registers. If the alternate function is Port LED and the GPIO Buffer Type is open-drain, the output buffer will automatically select between open-source and open-drain based on the applica-ble LED polarity. Alternate function input pins can be read by the software via the GPIO Data register and can gen-erate GPIO Interrupts. Table 9-1 shows the alternate function mapping.

GPIO ALTERNATE FUNCTIONALITY

GPIO	Pin#	Alternate Function	Configuration Strap	Condition
GPIO0	68	1588_EVENT_A	ALLPHYAD	See Note 2.
GPIO1	69	1588_EVENT_B	MODE_SEL0	—
GPIO2	70	1588_REF_CLK	—	—
GPIO3	72	1588_LD_ADJ	MODE_SEL1	—
GPIO4	73	1588_STI_CS_N	MODE_SEL2	—
GPIO5	74	1588_STI_CLK	MODE_SEL3	—

GPIO6	75	1588_STI_DO	MODE_SEL4	—
GPIO7	77	RCVRD_CLK_IN1	(TDI)	—
GPIO8	78	RCVRD_CLK_IN2	(TDO)	—
GPIO9	79	RCVRD_CLK_OUT1	(TMS)	—
GPIO10	80	RCVRD_CLK_OUT2	(TCK)	—
GPIO11	83	PORT0LED1	LED_MODE/PORT0_LED1_POL	See **Note 1**.
GPIO12	84	PORT0LED2	PHYAD0/PORT0_LED2_POL	See **Note 1**.
GPIO13	85	PORT3LED1	PHYAD1/PORT3_LED1_POL	See **Note 1**.
GPIO14	86	PORT3LED2	PHYAD2/PORT3_LED2_POL	See **Note 1**.
GPIO15	88	SOF0	PHYAD3	—
GPIO16	89	SOF2	PHYAD4	—
GPIO17	57	PORT1LED1	PORT1_LED1_POL	See **Note 1**.
GPIO18	58	PORT1LED2	PORT1_LED2_POL	See **Note 1**.
GPIO19	60	PORT2LED1	PORT2_LED1_POL	See **Note 1**.
GPIO20	61	PORT2LED2	PORT2_LED2_POL	See **Note 1**.
GPIO21	62	SOF1	—	—
GPIO22	67	—	—	—
GPIO23	90	SOF3	—	—

Note

1. To enable LED operation with either a pull-up or pull-down, LED Polarity takes on the inverted value of the configuration strap. The following must be considered when using GPIOs:
    1. Configuring a pin as a GPIO input automatically enables an internal pull-up.
    2. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
    3. Configuring a pin as a GPIO output automatically disables the internal pull-up. Open-drain outputs may require an external pull-up depending on the application.
2. ALLPHYAD configures the default support for PHY Broadcast access using PHY Address 0. The ALLPHYAD configuration strap is sampled and latched at power-up/Reset and are defined as 0: Enable PHY Broadcast accessed by default and 1: Disable PHY Broadcast accessed by default.

JTAG Pins

- An IEEE 1149.1-compliant TAP controller supports boundary scan and various test modes. The device includes an integrated JTAG boundary-scan test port for board-level testing. The interface consists of four pins (TDO, TDI, TCK, and TMS) and includes a state machine, data register array, and an instruction register. The JTAG pins are described in Table 9-2. The JTAG interface conforms to the IEEE Standard 1149.1 – 2001 Standard Test Access Port (TAP) and Boundary-Scan Architecture.
- All input and output data are synchronous to the TCK test clock input. TAP input signals TMS and TDI are clocked into the test logic on the rising edge of TCK, while the output signal TDO is clocked on the falling edge.
- JTAG pins are multiplexed with the GPIO pins.
- The JTAG functionality is selected when the TESTMODE (pin 38) is asserted.
- The TESTMODE (pin 38) should be tied to GND when JTAG not in use.

JTAG PIN DESCRIPTION

Pin Symbol	Pin Number	Pin Name
TCK	80	JTAG Test Clock
TDI	77	JTAG Data Input
TDO	78	JTAG Data Output
TMS	79	JTAG Test Mode Select

MISCELLANEOUS

Reset
The LAN8814 provides RESET_N input pin 37. (See Table 10-1.) This pin is used as a hardware Reset of the device and must adhere to the timing requirements detailed in Section 6.6.2, “Power Sequence Timing” and Section 6.6.3, “Reset Pin Configuration Strap Timing” of the LAN8814 Data Sheet. Release from Reset is based on the RESET_N input pin transitioning from low to high.

RESET PIN DESCRIPTION

Pin Name	Pin Number	Description
NRESET	37	Device Reset. This is an active-low input that powers down the device and sets all register bits to their default state.

PLL/Clocks

- **The device provides the following PLLs:**
  - **System PLL:** Generates the internal system clocks and clocks required for the internal PHYs. See Section 5.22.1, “System Clocks” in the LAN8814 Data Sheet for additional information.
  - **1588 PLL**: Generates the internal 1588 clock. See Section 5.22.2, “1588 Clock” in the LAN8814 Data Sheet for additional information.
  - **QSGMII SerDes MPLL:** Generates the clocks needed by the SerDes. See Section 5.22.3, “QSGMII SerDes Clock” in the LAN8814 Data Sheet for additional information.
    The reference clock selection of the System PLL and QSGMII SerDes MPLL are controlled via the REF_CLK_- SEL[1:0] pins. Refer to Table 3-6 of the data sheet for detailed REF_CLK_SEL[1:0] setting information.
- **The System PLL can use any of the following as its input reference clock:**
  - 25 MHz Crystal
  - 25 MHz system single-ended reference clock input
  - 125 MHz system differential clock inputs
- **The System PLL generates the following clocks:**
  - 250 MHz system clock
  - 25 MHz system clock
- The reference clock selection is controlled by the pin configurations shown in Table 10-2.

REFERENCE CLOCK CONTROL

Description	Pin	Selection Control
Reference Clock Select	REF_CLK_SEL_0 pin 33 REF_CLK_SEL_1 pin 35	These pins control the reference clock selection of the System PLL and QSGMII SerDes.
		MPLL. REF_CLK_SEL[1:0]
		00 = SYSPLL Reference 25 MHz from XI/XO QSG MII Reference 25 MHz from XI/XO 01 = RESERVED 10 = SYSPLL Reference 25 MHz from CK125_RE F_INP/M QSGMII Reference 125 MHz from CK12 5_REF_INP/M 11 = RESERVED

Note

1. These are live pins and not configuration straps. They must be permanently tied high or low.
2. XI/XO can be a 25 MHz crystal or a 25 MHz external clock.
3. CK125_REF_INP/M is a 125 MHz external clock.

The 1588 reference clock input options are 10 MHz, 25 MHz, and 125 MHz.

Reference Resistor
Refer to Table 10-3 for reference resistor pin details.

REFERENCE RESISTOR PIN DESCRIPTION

Pin Name	Pin Number	Description
ISET	2	This pin must be connected to ground through a 6.04 kΩ, 1% resistor.
RES_REF	52	This pin must be connected to ground through a 200Ω, 1% 100ppm/°C resistor.

Test Mode
Refer to Table 10-4 for Test mode pin details.

TEST MODE PIN DESCRIPTION

Pin Name	Pin Number	Description
TESTMODE	38	For normal operation, this pin must be pulled down to ground. The JTAG f unctionality is selected when the TESTMODE (pin 38) is asserted.

LED Pins

- The device provides eight programmable LEDs, two per port (PORT[0:3]LED[1:2]), which are configurable to support multiple LED modes. The LED mode is configured by the LED_MODE configuration strap as well as port-specific instances of the LED Control Register 1 and 2. All eight LEDs are configured with identical behavior via the LED_MODE configuration strap. Port-specific LED configuration can be accomplished via the LED Control Register 1 and 2. The supported LED modes are:
    - Individual-LED Mode (LED Control Register 1, bit[6] = ‘1’, LED_MODE pulled-up)
    - Tri-color-LED Mode (LED Control Register 1, bit[6] = ‘1’, LED_MODE pulled-down)
    - Enhanced LED Mode (LED Control Register 1, bit[6] = ‘0’, LED_MODE unused)
- To use LEDs, they must be enabled as GPIOs and GPIO alternate functions. The GPIOs must be configured as outputs, and the proper output driver type must be selected (open-drain or push-pull). If open-drain type is selected, the output driver will automatically choose between open-source and open-drain based on LED polarity. The PORT[3:0]_LED[2:1]_POL configuration straps set the default polarity of the LED pins. Refer to the LAN8814 Data Sheet Section 3.3.5, “LED Polarity (PORT[3:0]_LED[2:1]_POL)” for additional LED polarity information. Refer to Section 3.3.4, “LED Mode Select (LED_MODE)” of the LAN8814 Data Sheet for additional LED_MODE information.

LED MODE SELECT (LED_MODE)

- The LED_MODE configuration strap selects between Individual-LED (pulled-up) or Tri-color-LED (pulled-down) modes. All eight LEDs are configured with identical behavior. (See Table 10-5.) The LED_MODE configuration strap is sampled and latched at power-up/Reset and is defined as follows:
  - **0**: Tri-color-LED mode
  - **1**: Individual-LED mode
- LED operation is described in Section 5.19, “LEDs” of the LAN8814 Data Sheet.

GPIO LED FUNCTIONALITY

GPIO	Pin#	Alternate Function	Configuration Strap
GPIO11	83	PORT0LED1	LED_MODE/PORT0_LED1_POL
GPIO12	84	PORT0LED2	PHYAD0/PORT0_LED2_POL
GPIO17	57	PORT1LED1	PORT1_LED1_POL

Note

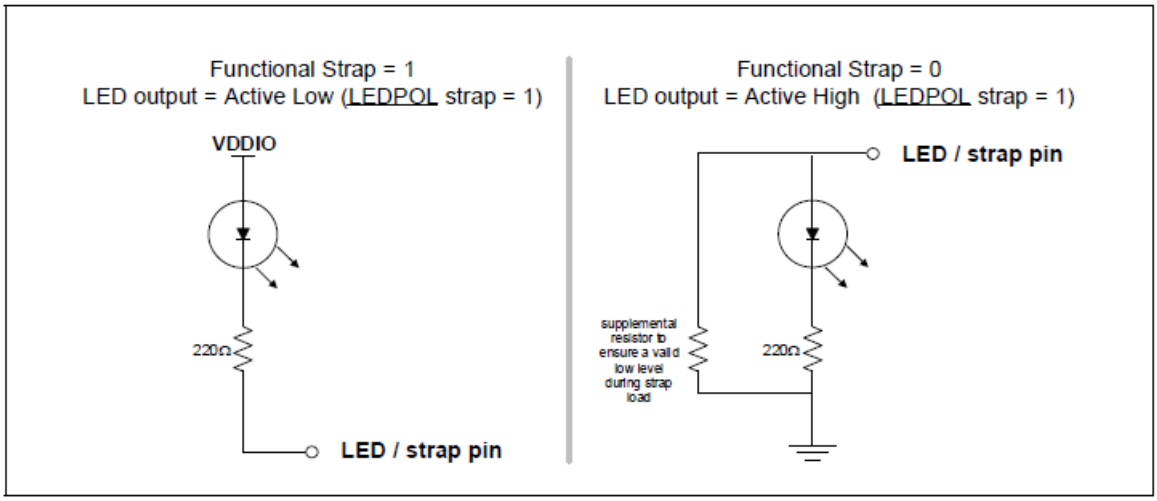
1. To enable LED operation with either a pull-up or pull-down, LED Polarity takes on the inverted value of the register bit.
2. Using 330Ω to 510Ω current limit resistor and VDD25 for LED power are recommended.

GPIO	Pin#	Alternate Function	Configuration Strap
GPIO18	58	PORT1LED2	PORT1_LED2_POL
GPIO19	60	PORT2LED1	PORT2_LED1_POL
GPIO20	61	PORT2LED2	PORT2_LED2_POL
GPIO13	85	PORT3LED1	PHYAD1 / PORT3_LED1_POL
GPIO14	86	PORT3LED2	PHYAD2 / PORT3_LED2_POL

Note

1. To enable LED operation with either a pull-up or pull-down, LED Polarity takes on the inverted value of the register bit.
2. Using 330Ω to 510Ω current limit resistor and VDD25 for LED power are recommended.

PIN LED STRAPPING



Other Pins

- The COMA_MODE (pin 36) is designed to hold the PHY in a suspended state until system initialization is complete. When enabled by driving the COMA_MODE pin high, all the errors, alarms, link up/down notifications, etc. are suppressed until COMA_MODE is driven low. This is useful in designs with multiple PHYs as it allows all errors to be suppressed until the entire board is configured. Coma mode operates as indicated in Table 10-6. There is no Register Control of the COMA mode pin in this device.
- The Auto MDI/MDIX (Pair-Swap). The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the device and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner and assigns the MDI/MDI-X pair mapping of the device accordingly. Table 10-6 shows the device 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

MDI/MDI-X PIN MAPPING

Pin (RJ-45 Pair)	**MDI**			**MDI-X**		
	1000BASE-T	**100BASE-T**	**10BASE-T**	**1000BASE-T**	**100BASE-T**	**10BASE-T**
TXRXP/M_A (1, 2)	A+/–	TX+/–	TX+/–	A+/–	RX+/–	RX+/–
TXRXP/M_B (3, 6)	B+/–	RX+/–	RX+/–	B+/–	TX+/–	TX+/–
TXRXP/M_C (4 ,5)	C+/–	Not Used	Not Used	C+/–	Not Used	Not Used

Pin (RJ-45 Pair)	**MDI**			**MDI-X**		
	1000BASE-T	**100BASE-T**	**10BASE-T**	**1000BASE-T**	**100BASE-T**	**10BASE-T**
TXRXP/M_D (7 ,8)	D+/–	Not Used	Not Used	D+/–	Not Used	Not Used

Unused and No-Connection Pins
The NC pins (pins 91 and 92) are unconnected pins. They must be left floating.

General External Pull-Up and Pull-Down Resistors

- If there is no pull-up resistor value specified, a 4.7 kΩ resistor is recommended.
- If there is no pull-down resistor value specified, a 1 kΩ or 4.7 kΩ resistor is recommended.

HARDWARE CHECKLIST SUMMARY

HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, “General Considerations”	Section 2.1, “Required References”	All necessary documents are on hand.		
	Section 2.2, “Pin Check”	The pins match the data sheet.		
	Section 2.3, “Ground”	Verify if a single ground reference as a system ground is used for all ground pins. Check if there is a chassis ground for the line-side ground.		
	Section 3.1, “Current Requirements”	Refer to Table 3-1 to ensure that the power pins are correct. Select the correct power supply components with at least about 25 % to 30% margin based on worst case for the system power design.		

Section 3.0, “Power”	Section 3.2, “Power Supply Planes”	When creating a PCB layout, refer to this section for power sup- ply pl ane design.		
	Section 3.3, “Power Circuit Connection and Analog Power Plane Filtering”	Refer to Figure 3-1 to check the p ower circuit connection, decoupling capacitors, and filtering .		
	Section 3.4, “Bulk Decoupling Capaci- tors”	When creating a PCB layout, refer to this section for the bulk decoupli ng capacitor required.		
Section 4.0, “Twisted Pair Media Interfa ce”	Section 4.1, “10/100/1000 Mbps Inter- face Connecti on”	Verify all analog I/O pin connection s for quad-port circuit design based on product design requirem ents to select the design of Figure 4-1.		
	Section 4.2, “Magn etics Connection a nd RJ45 Connectio n”	Verify the magnetics and the com mon-mode capacitors connec- tion based on Figure 4-1.		
	Section 4.3, “PCB L ayout Consider- ati ons”	Refer to this section for PCB layout design reference to check if the Gi gabit copper port PCB layout requ est is met.		
	Section 5.1, “QSGMII/Q-USGMII Pins and Connection”	Refer to this section for guidelines to ensure that the correct pins for QSGMII MAC interface are used in the design.		

Section 5.0, “QSGMII/Q-USGMII MAC Interface”	Section 5.2, “QSGMII MAC”	Refer to Figure 5-1 for QSGMII MAC interface to connect to four external QSGMII MACs in the design.		
	Section 5.3, “QSGMII MAC Design Rules”	Refer to this section for QSGMII MAC interface PCB design guidelines.		

Section	Check	Explanation	√	Notes
Section 6.0, “Device Clocks”	Section 6.1, “Reference Clock”	Refer to this section when selecting the reference clock fre- quency and the correct reference clock pins in the design. Fol- low the layout required in PCB design.		
	Section 6.2, “System Clock and Syn- chronous Ethernet Connections”	Refer to this section for System Clock and Synchronous Ether- net connections. Verify the correct pin connections and follow the PCB Board layout recommendations.		
	Section 6.3, “Single-Ended REFCLK Input”	Refer to Figure 6-1 for single-ended reference input clock circuit design and use the correct resistor divider in the circuit based on Table 6-1 for correct resistors values.		
	Section 6.4, “Differential REFCLK Input”	Refer to Figure 6-1 for the differential reference input clock cir- cuit design and use the correct capacitor AC coupling in the design.		

Section 7.0, “Media Recovered Clock Output”		Refer to this section and Figure 7-1 for the typical recovered clock circuit design and use the correct recovered clock pins and correct configuration.		
		Refer to Figure 7-2 for the typical Synchronous Ethernet clock circuit design, and use the correct recovered clock pins and cor- rect configuration.		
		Refer to Figure 7-3 for the typical Synchronous Ethernet clock circuit design Daisy Chain configuration, and use the correct recovered clock pins and correct configuration.		
Section 8.0, “1588 Support”	Section 8.1, “IEEE 1588 Pin Connec- tions”	Refer to Table 8-1 to select the correct 1588 differential clock pin pair in the design.		
	Section 8.2, “1588 Serial Timestamp Interface”	Refer to Table 8-2 to use the correct 1588 serial timestamp interface pins in the design. Refer to this section for 1588 serial timestamp interface reference design connection.		
	Section 9.1, “MIIM (MDIO) Interface”	Refer to this section for the MIIM interface circuit design.		

Section 9.0, “Digital Interface and I/O”	Section 9.2, “GPIO Pins”	Check if the correct PHY address pins are used based on Table 9-1 to configure the correct PHY address the design requires.		
	Section 9.3, “JTAG Pins”	Refer to Table 9-2 and the descriptions in this section for all JTAG pins in the circuit design.		

Section	Check	Explanation	√	Notes
Section 10.0, “Miscellaneous”	Section 10.1, “Reset”	Refer to Table 10-1 to use the correct Reset pin and check if the designed Reset circuit meets the Reset time requirement.		
	Section 10.2, “PLL/Clocks”	Refer to Table 10-2 to select the correct Reference Clock con- figuration and ensure that the correct pins are connected.		
	Section 10.3, “Reference Resistor”	Refer to Table 10-3 to select the correct Reference Resistor biasing pins in the design. Make sure to connect a 6.04 kΩ 1% resistor between the **ISET** and **GND**. In addition, make sure to connect a 200 kΩ 1% resistor between **RES_REF** pin and **GND**.		
	Section 10.4, “Test Mode”	Check if correct **TESTMODE** pin setup is used based on Table 10-4.		
	Section 10.5, “LED Pins”	Check if correct LED pins are used based on Table 10-5, cur- rent limit resistors, and LED power.		

	Section 10.7, “Other Pins”	For **COMA_MODE**, check this section for the correct design.		
	Section 10.8, “Unused and No-Con- nection Pins”	Verify if all reserved pins and NC pins are unconnected.		
	Section 10.9, “General External Pull- Up and Pull-Down Resistors”	Generally, it is recommended to use 4.7 kΩ pull-up resistor and 1 kΩ pull-down resistor.		

REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004514A (04-11-22)	Initial release	

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- Product Support – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
- General Technical Support – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- Business of Microchip – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip’s customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest. To register, access the Microchip web site at www.microchip.com. Under “Support”, click on “Customer Change Notification” and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office

- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document. Technical support is available through the web site at: **http://microchip.com/support**

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at **https://www.microchip.com/en-us/support/designhelp/client-support-services**.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WAR- RANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON- INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE. IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDI- RECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE.

TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O,

Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries. AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch

Flashtec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet- Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A. Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, NVM Express

NVMe, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries. SQTP is a service mark of Microchip Technology Incorporated in the U.S.A. The Adaptec logo, Frequency on Demand, Silicon Storage Technology, Symmcom, and Trusted Time are registered trademarks of Microchip Technology Inc. in other countries. GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries. All other trademarks mentioned herein are property of their respective companies. © 2022, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.
ISBN: 978-1-6683-0216-3

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199

- **Tel**: 480-792-7200
- **Fax:** 480-792-7277

Technical Support:

- http://www.microchip.com/support
- **Web Address**: www.microchip.com

Documents / Resources

	[MICROCHIP LAN8814 Hardware Design Checklist](#) [pdf] User Guide LAN8814 Hardware Design Checklist, LAN8814, Hardware Design Checklist, Design Checklist

Manuals+.