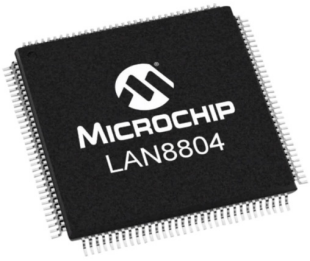

MICROCHIP LAN8804 4-Port Gigabit Ethernet Transceiver User Guide

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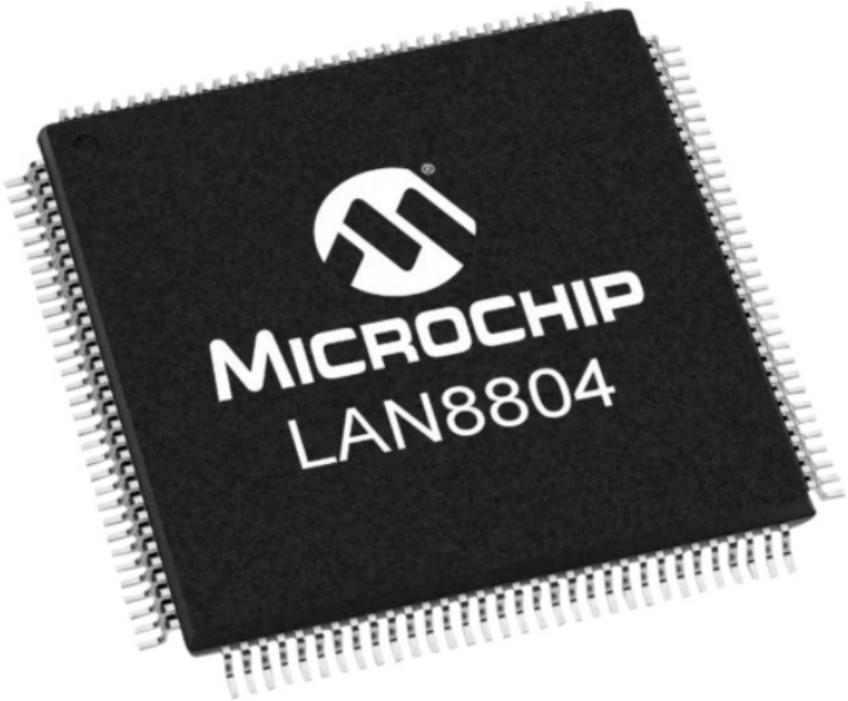


Hardware Design Checklist
LAN8804

Contents

INTRODUCTION

This document provides a hardware design checklist for the Microchip LAN8804 product family. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the LAN8804 in a new design. A summary
of these items is provided in Section 9.0, “HardwareChecklist Summary”. Detailed information on these subjects can be found in the corresponding sections:

- **Section 2.0, “General Considerations”**
- **Section 3.0, “Power”**
- **Section 4.0, “Twisted Pair Media Interface”**
- **Section 5.0, “QSGMII/Q-USGMII MAC Interface”**
- **Section 6.0, “Device Clocks”**
- **Section 7.0, “Digital Interface and I/O”**
- **Section 8.0, “Miscellaneous”**

GENERAL CONSIDERATIONS

2.1 Required References

The LAN8804 implementor should have the following documents on hand:

- LAN8804 4-Port Gigabit Ethernet Transceiver with QSGMII Support Data Sheet
- LAN8804 EVB documents, including the schematics, PCB file, BOM and so on. The documents can be found at www.microchip.com.

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and the RJ45 connector at line side for better EMI and ESD.

POWER

Tab l e 3-1 shows the power supply pins for LAN8804.
TABLE 3-1: POWER SUPPLY PINS

Name	Pin	Description	Comments
+2.5/3.3V Analog I/O Power Supply	VDDAH 4 VDDAH_P[3:0] 113, 100, 24, 11 VDDAH_SERDES 49, 51 VDDAH_PLL_PTP 65 VDDAH_ABPVT 66	+2.5/3.3V analog I/O power supply	Power
+2.5/3.3V Analog Power Supply	VDD33REF 3	+2.5/3.3V analog power supply	Power
+1.1V Analog Power Supply	VDDAL_ADC_A_P[3:0] 109, 96, 20, 7 VDDAL_ADC_B_P[3:0] 110, 97, 21, 8 VDDAL_ADC_C_P[3:0] 116, 103, 27, 14 VDDAL_ADC_D_P[3:0] 117, 104, 28, 15 VDDAL_PLL 1 VDDAL_SERDES 43 VDDTXL_SERDES 46 VDDAL_CK125 41, 121	+1.1V analog power supply	Power
+3.3/2.5/1.8V Variable I/O Power Supply Input	VDDIO 53, 59, 64, 71, 76, 87, 93 VDDIO_1 34	+3.3/2.5/1.8V variable I/O digital power supply input	Power
+1.1V Digital Core Power Supply Input	VDDCORE 39, 54, 63, 81, 124	+1.1V digital core power supply input	Power
Paddle Ground	P_VSS	Common ground. This exposed paddle must be connected to the ground plane with a via array.	GND
Ground	VSS_CK125 40, 120	Ground	GND

3.1 Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support the current

requirements specified for each power rail in the power consumption section of the device data sheet. (See the LAN8804 Data Sheet for the different
system configurations.)

- The “Operational Characteristics” section of the LAN8804 Data Sheet contains the details of the power consumption of the device as measured during different modes of operation at various operating voltages. Power dissipation is impacted by temperature, supply voltage, and external source or sink requirements.
- All worst-case measurements were taken at +6% power supply and +125°C case temperature. Refer to the “Worst-Case Four Port Operation” section of the LAN8804 Data Sheet.
- Power consumption data is split into tables in the “Power Consumption” section of the LAN8804 Data Sheet for typical operation, and the tables in the “Worst-Case Four Port Operation” section of the LAN8804 Data Sheet for worst-case operation (listed as VDDCore, VDDAL_x, and VDDIO_x).
- Four-port operation:
  – Four Port (1.17V, 3.5V, and 3.5V) Power Consumption
  – Four Port (1.17V, 2.65V, and 2.65V) Power Consumption
  – Four Port (1.17V, 2.65V, and 1.91V) Power Consumption

3.2 Power Supply Planes

- The LAN8804 integrates an optional LDO controller to be used with an external P-channel MOSFET when generating the 1.1V supply from an existing 2.5V or 3.3V source. Using the LDO controller and MOSFET is not required. An external 1.1V supply can be alternatively utilized.

3.2.1 MOSFET SELECTION

- The most important minimum PCB design and layout requirements or considerations for MOSFET selection are:
  – P-channel
  – 500 mA continuous current
  – 3.3V or 2.5V source – input voltage
  – 1.1V drain – output voltage for the MOSFET must be operating in the constant current saturated region and not towards the threshold voltage for the cut-off region of the MOSFET, V
- The V GS .
- A 220 µF electrolytic capacitor between 1.1V and ground is required for proper LDO operation.

3.2.2 LDO DISABLE GS(th)

- The LDO controller is enabled by default. It may be alternatively disabled via internal register settings. An external source of 1.1V is necessary if the LDO is disabled.

3.3 Power Circuit Connection and Analog Power Plane Filtering

- Refer to Figure 3-1, which shows the power and ground connections for LAN8804.
- The 1.1V power rail is not optional. However, the user has the option to select either 2.5V or 3.3V power rail. The filtered analog 1.1V and 2.5V or 3.3V supplies should not be shorted to any other digital supply at the

package or PCB level.

- The most important PCB design and layout considerations are as follows:

  – Ensure that the return plane is adjacent to the power plane (without a signal layer in between).

  – Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.

  – Minimize resistive drop while efficiently conducting away heat from the device using 1 oz copper cladding.

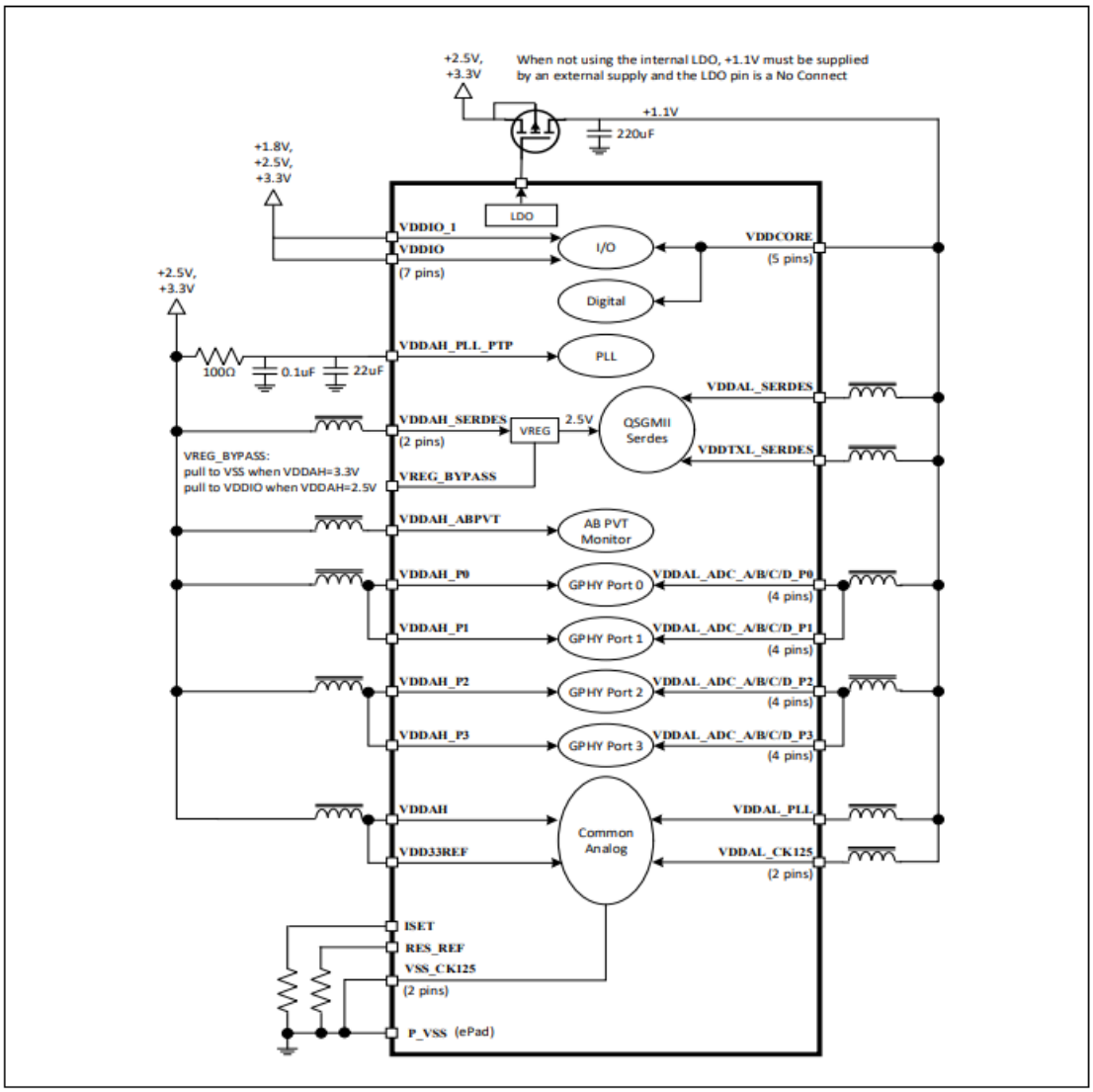
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent ran- dom system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power the pins of the device with correctly positioned local decoupling.

- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or highpower devices.

  – A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.

  – Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Bulk Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and be placed as close as possible to every LAN8804 power pin.
- Make sure that bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail of the power supply.

TWISTED PAIR MEDIA INTERFACE

4.1 10/100/1000 Mbps Interface Connection

The LAN8804 has four GPHY ports from PHY 0 to PHY 3 for Port 1, Port 2, Port 3, and Port 4. Detailed pin numbers from PHY 0 to PHY 3 sequence and descriptions are as follows:

- TX_RXP_A_[0:3] (pins 5, 18, 94, 107): These pins are the transmit/receive positive (+) connection from Pair A of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- TX_RXN_A_[0:3] (pins 6, 19, 95, 108): These pins are the transmit/receive negative (–) connection from Pair A of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- TX_RXP_B_[0:3] (pins 9, 22, 98, 111): These pins are the transmit/receive positive (+) connection from Pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- TX_RXN_B_[0:3] (pins 10, 23, 99, 112): These pins are the transmit/receive negative (–) connection from Pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- TX_RXP_C_[0:3] (pins 12, 25, 101, 114): These pins are the transmit/receive positive (+) connection from Pair C of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- TX_RXN_C_[0:3] (pins 13, 26, 102, 115): These pins are the transmit/receive negative (–) connection from Pair C of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- TX_RXP_D_[0:3] (pins 16, 29, 105, 118): These pins are the transmit/receive positive (+) connection from Pair D of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- TX_RXN_D_[0:3] (pins 17, 30, 106, 119): These p i ns are the transm i t/rece i ve pos i t i ve (+) connection from pair D of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.

4.2 Magnetics Connection and RJ45 Connection

- The center tap connection on the LAN8804 side for Pair A channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the LAN8804 side for Pair B channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the LAN8804 side for Pair C channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the LAN8804 side for Pair D channel only connects a 0.1 µF capacitor to GND.

No bias is needed.

- The center taps of the magnetics of all four pairs are recommended to be isolated with separate 0.1 µF capacitors to ground. The reason is the common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active,
  while Pairs C and D are inactive.) However, for integrated connector magnetics with ganged center taps, a workaround script to address this analog front-end limitation is available in the software. See LAN8804 Errata.
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to the chassis ground.
- Only one 1000 pF, 2 kV capacitor to the chassis ground is required for each PHY. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2vkV capacitor or a ferrite bead to be connected between the chassis ground and the system ground is required. It is shared by PHY 0, PHY 1, PHY 2, and PHY 3 for Port 1, Port 2, Port 3, and Port 4.
- The RJ45 shield should connect to the chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 4.3, “PCB Layout Considerations” for guidance on how the chassis ground should be created from system ground.

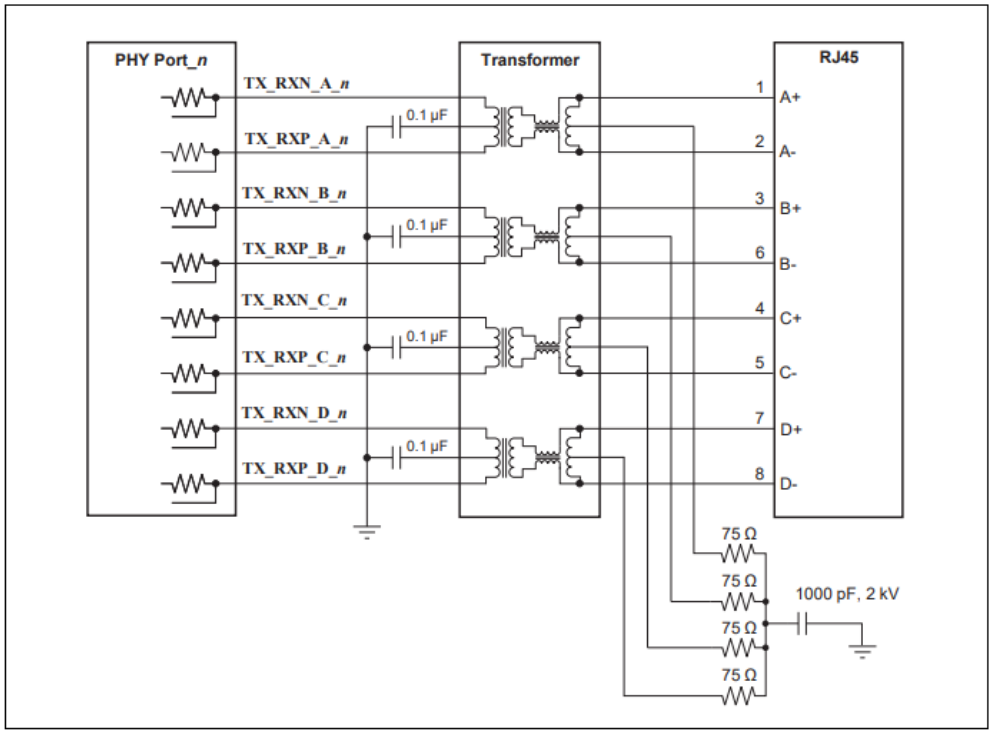
4.3 PCB Layout Considerations

- All differential pairs of the MDI interface traces should have a characteristic impedance of 100Ω to the GND plane. This is a strict requirement to minimize return loss. This requirement is placed upon the PCB designer and the FAB house.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI and crosstalk. Each port of pairs A, B, C, and D should match in length to prevent delay mismatch that would cause common-mode noise.
- Ideally, there should be no crossover or via on the signal paths.
- Incorporate a 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor or ferrite bead far away from the LAN8804 device or other sensitive devices in the PCB layout placement for better ESD.

4.4 Ethernet Media Interface

Figure 4-1 illustrates the device Ethernet media interface connections. Note that the device supports integrated connector magnetics with ganged center taps.

FIGURE 4-1: ETHERNET MEDIA INTERFACE CONNECTIONS



QSGMII/Q-USGMII MAC INTERFACE

- The LAN8804 device supports QSGMII/Q-USGMII MAC interface to convey four ports of network data and port speeds of 10/100/1000 Mbps.
- Detailed pin numbers and pin descriptions of the QSGMII MAC interface are described in the following subsections. Figure 5-1 shows the device QSGMII/Q-USGMII MAC interface connections.

5.1 QSGMII/Q-USGMII Pins and Connection

The LAN8804 supports the QSGMII/Q-USGMII MAC interface to convey four GPHY ports from PHY 0 to PHY 3. Detailed pin numbers and descriptions on the QSGMII MAC interface are as follows:

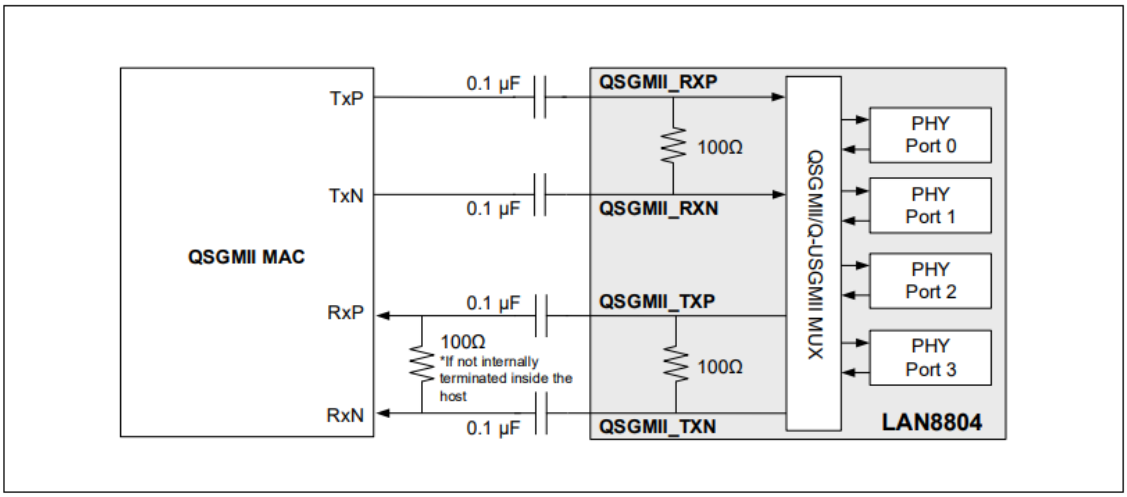
- QSGMII_TXP (pin 47): This pin is the transmit positive (+) signal connection for a differential pair for QSGMII/QUSGMII Transmitter Output Positive.
- QSGMII_TXN (pin 45): This pin is the transmit negative (–) signal connection for a differential pair for QSGMII/QUSGMII Transmitter Output Negative.
- QSGMII_RXP (pin 42): This pin is the receive positive (+) signal connection for a differential pair for QSGMII/QUSGMII Transmitter Input Positive.
- QSGMII_RXN (pin 44): This pin is the receive negative (–) signal connection for a differential pair for QSGMII/QUSGMII Transmitter Input Negative.
- REF_PAD_CLK_P (pin 50): This is the positive (+) signal connection of differential pair for QSGMII/Q-USGMII External Reference Clock Input Positive.
- REF_PAD_CLK_M (pin 48): This is the negative (–) signal connection of differential pair for QSGMII/Q-USGMII External Reference Clock Input Negative.

5.2 QSGMII MAC

- The LAN8804 device supports a QSGMII MAC to convey four ports of network data and port speed from

10/100/ 1000 Mbps. If the QSGMII MAC that the LAN8804 is connecting to supports this functionality, configure the device for QSGMII MAC mode.

FIGURE 5-1: QSGMII MAC INTERFACE CONNECTIONS



5.3 QSGMII MAC Design Rules

- Use AC coupling with 0.1 µF capacitors for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce crosstalk between differential pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.

DEVICE CLOCKS

6.1 Reference Clock

The device reference clock supports both 25 MHz and 125 MHz clock signals. Differential clocks should be LVDS-compatible.

6.2 System Clock and Synchronous Ethernet Connections

The LAN8804 system reference clock supports a crystal input/system reference clock input interface with the following pin details:

- XI (pin 128): Crystal Input/System Reference Clock Input. When using a 25 MHz crystal, this input is connected to one lead of the crystal. Refer to REF_CLK_SEL[1:0] for additional information. When using a 25 MHz system reference clock, this is the input from the external 25MHz oscillator.
- XO (pin 127): Crystal Output. When using a 25 MHz crystal, this output is connected to one lead of the crystal. Refer to REF_CLK_SEL[1:0] for additional information. When using a 25 MHz system reference clock source, this pin is not connected.
- CK125_REF_INP (pin 123): System Reference Clock Input Positive. This pin is the positive (+) signal connection of a differential pair. When using a 125 MHz system reference clock source, this is connected to the

125 MHz external oscillator. Refer to REF_CLK_SEL[1:0] for additional information.

- CK125_REF_INM (pin 122): System Reference Clock Input Negative. This pin is the negative (–) signal connection of a differential pair. When using a 125 MHz system reference clock source, this is connected to the 125 MHz external oscillator. Refer to REF_CLK_SEL[1:0] for additional information.
- CK25OUT (pin 126): System Clock Output. Buffered copy of the internal 25 MHz reference clock. This output clock is powered by VDDAH.

When reference clocks are used, ensure that:

- The jitter requirements in the LAN8804 Data Sheet are met.
- The traces are routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- All reference clocks must be free from glitches or must be hitless.
- Unused reference clocks can be left floating (No Connect).

6.3 Single-Ended REFCLK Input

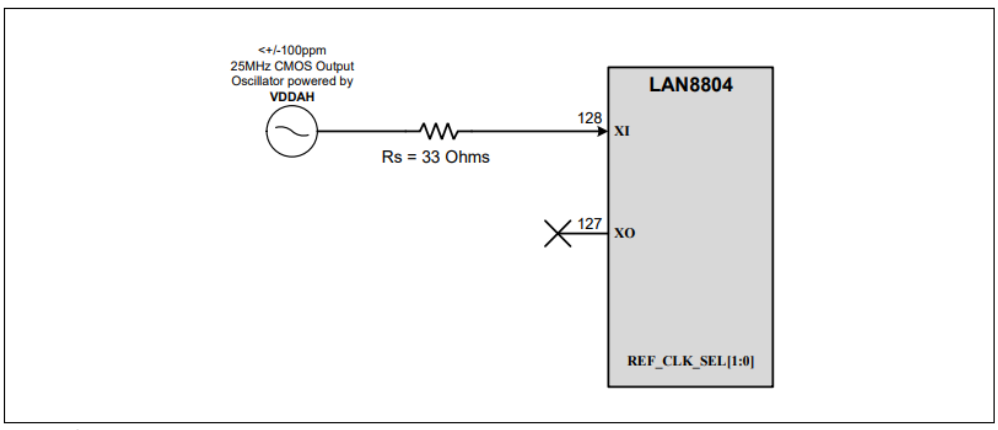
To use a single-ended reference clock, an external resistor (Rs) is required. The purpose of the Rs is to limit the drain on the oscillator output. The configurations for a single-ended REFCLK are referenced to VDDAH in accordance with the diagram on power connections in Figure 3-1.
The ICLK Type Input Buffer's non-variable I/O DC electrical characteristics are specified in Tab l e 6-1 , and the SingleEnded REFCLK Input diagram is shown in Figure6-1.

TABLE 6-1: ICLK TYPE INPUT BUFFER NON-VARIABLE I/O DC ELECTRICAL CHARACTERISTICS

ICLK Type Input Buffer	Symbol	Minimum	Maximum	Unit	Note
Low Input Level	VIL	—	0.5	V	**Note 1**
High Input Level	VIH	2.0	—	V	
Input Leakage	IIH	–10	10	µA	

Note 1: XI can optionally be driven from a 25 MHz single-ended clock oscillator to which these specifications apply.

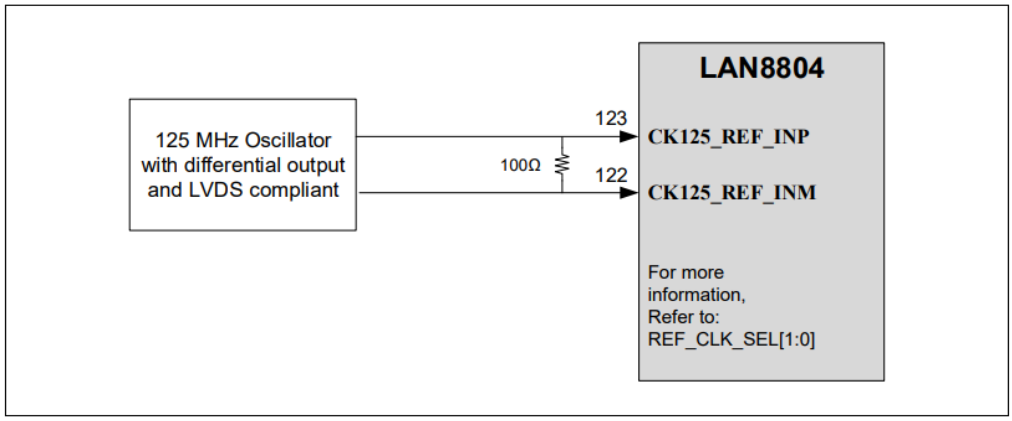
FIGURE 6-1: SINGLE-ENDED REFCLK INPUT



6.4 Differential REFCLK Input

Differential clocks must be LVDS-compatible. Figure 6-2 shows the configuration.

FIGURE 6-2: REFCLK DIFFERENTIAL INPUT



DIGITAL INTERFACE AND I/O

7.1 MIIM (MDIO) Interface

- The LAN8804 device supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the device. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification (see Note).
- The MIIM interface consists of the following:
  – A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
  – A specific protocol that operates across the physical connection that allows an external controller to communicate with one or more devices. Each device is assigned a unique PHY address between 0h and 1Fh by the PHYAD[4:0] strapping pins.
  – ALLPHYAD: (pin 68): GPIO0/1588_EVENT_A/ALLPHYAD – The ALLPHYAD configuration strap sets the default of the All-PHYAD Enable bit in the Common Control register, which enables (pulled-down) or disables (pulled-up) the PHY's ability to respond to PHY Address 0 as well as its assigned PHY address.
  – PHYAD0: (pin 84): GPIO12/PORT0LED2/PHYAD0/PORT0_LED2_POL
  – PHYAD1: (pin 85): GPIO13/PORT3LED1/PHYAD1/PORT3_LED1_POL
  – PHYAD2: (pin 86): GPIO14/PORT3LED2/PHYAD2/PORT3_LED2_POL
  – PHYAD3: (pin 88): GPIO15/SOF0/PHYAD3
  – PHYAD4: (pin 89): GPIO16/SOF2/PHYAD4
- The ALLPHYAD strap input is inverted as compared to the Register bit value.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indi- rect access to MMD addresses and registers.
- ALL PHYS ADDRESS. Typically, the Ethernet PHYs are accessed at the PHY addresses set by the PHYAD[4:0] strapping pins. PHY Address 0h is optionally supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set the Basic Control register to a value of 0x1940 to set bit[11] to a value of one to enable software power-down).
- PHY Address 0 is enabled (in addition to the PHY address set by the PHYAD[4:0] strapping pins) when the AllPHYAD Enable bit inthe Common Control register is set to '1'. The ALLPHYAD configuration strap can also be used to set the default of the All-PHYAD Enable bit.

- The MDIO Output Pin Drive mode is controlled by two bits defined in EP4.5 and Reg17:
  – The MDIO Buffer Type bit in the Output Control register (EP4.5 – bit 15 for port 0)
  – The test_a1_a2_en_bit (Reg17 – bit 9 for each port of the PHY)
- When set to a '0', the MDIO output is open-drain. When set to '1', the MDIO output is push-pull. To configure MDIO output for push-pull, write a value of 0x8000 on Port 0 to Register EP4.5 (sets bit 15). For each port, write a value of 0x02f4 to Register 17 which sets bit 9 on all ports.

Note: The MDIO pin can only be connected with other Clause 22 MIIM Targets. Connecting any Clause 45 Targets, such as a 10G PHY, will cause undesirable behavior.

7.2 GPIO Pins

- The General Purpose I/Os (GPIOs) consist of 24 programmable input/output pins that are shared with other pins. These pins are individually configurable via the GPIO registers.
- Extreme care must be taken on strap input pins that may be used for General Purpose Inputs. The General Purpose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.
- Many GPIOs have the ability to be used as an alternate function. Once enabled as a GPIO, the alternate function is selected by the bits in the GPIO Alternate Function Select registers. The alternate function buffer type is still selected via the GPIO Buffer Type registers. If the alternate function is Port LED and the GPIO Buffer Type is open-drain, the output buffer will automatically select between open-source and open-drain based on the applicable LED polarity. Alternate function input pins can be read by the software via the GPIO Data register and can generate GPIO Interrupts. Table 7-1 shows the alternate function mapping.

TABLE 7-1: GPIO ALTERNATE FUNCTIONALITY

GPIO	Pin#	Alternate Function	Configuration Strap	Condition
GPIO0	68	1588_EVENT_A	ALLPHYAD	See **Note 2**.
GPIO1	69	1588_EVENT_B	MODE_SEL0	—
GPIO2	70	1588_REF_CLK	—	—
GPIO3	72	1588_LD_ADJ	MODE_SEL1	—
GPIO4	73	1588_STI_CS_N	MODE_SEL2	—
GPIO5	74	1588_STI_CLK	MODE_SEL3	—
GPIO6	75	1588_STI_DO	MODE_SEL4	—
GPIO7	77	RCVRD_CLK_IN1	(TDI)	—
GPIO8	78	RCVRD_CLK_IN2	(TDO)	—

GPIO9	79	RCVRD_CLK_OUT1	(TMS)	—
GPIO10	80	RCVRD_CLK_OUT2	(TCK)	—
GPIO11	83	PORT0LED1	LED_MODE/PORT0_LED1_POL	See **Note 1**.
GPIO12	84	PORT0LED2	PHYAD0/PORT0_LED2_POL	See **Note 1**.
GPIO13	85	PORT3LED1	PHYAD1/PORT3_LED1_POL	See **Note 1**.
GPIO14	86	PORT3LED2	PHYAD2/PORT3_LED2_POL	See **Note 1**.
GPIO15	88	SOF0	PHYAD3	—
GPIO16	89	SOF2	PHYAD4	—
GPIO17	57	PORT1LED1	PORT1_LED1_POL	See **Note 1**.
GPIO18	58	PORT1LED2	PORT1_LED2_POL	See **Note 1**.
GPIO19	60	PORT2LED1	PORT2_LED1_POL	See **Note 1**.
GPIO20	61	PORT2LED2	PORT2_LED2_POL	See **Note 1**.
GPIO21	62	SOF1	—	—
GPIO22	67	—	—	—
GPIO23	90	SOF3	—	—

Note

1. To enable LED operation with either a pull-up or pull-down, LED Polarity takes on the inverted value of the configuration strap. The following must be considered when using GPIOs:
   – Configuring a pin as a GPIO input automatically enables an internal pull-up.
   – Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
   – Configuring a pin as a GPIO output automatically disables the internal pull-up. Open-drain outputs may require an external pull-up depending on the application.
2. ALLPHYAD configures the default support for PHY Broadcast access using PHY Address 0. The ALLPHYAD configuration strap is sampled and latched at power-up/Reset and are defined as 0: Enable PHY Broadcast accessed by default and 1: Disable PHY Broadcast accessed by default.

7.3 JTAG Pins

- An IEEE 1149.1-compliant TAP controller supports boundary scan and various test modes. The device includes an integrated JTAG boundary-scan test port for board-level testing. The interface consists of four pins (TDO, TDI, TCK and TMS) and includes a state machine, data register array and an instruction register. The JTAG pins are described in Table 7-2. The JTAG interface conforms to the IEEE Standard 1149.1 – 2001 Standard Test Access Port (TAP) and Boundary-Scan Architecture.
- All input and output data are synchronous to the TCK test clock input. TAP input signals TMS and TDI are clocked into the test logic on the rising edge of TCK, while the output signal TDO is clocked on the falling edge.
- JTAG pins are multiplexed with the GPIO pins.
- The JTAG functionality is selected when the TESTMODE (pin 38) is asserted.
- The TESTMODE (pin 38) should be tied to GND when JTAG not in use.

TABLE 7-2: JTAG PIN DESCRIPTION

Pin Symbol	Pin Number	Pin Name
TCK	80	JTAG Test Clock
TDI	77	JTAG Data Input
TDO	78	JTAG Data Output
TMS	79	JTAG Test Mode Select

MISCELLANEOUS

8.1 Reset

- The LAN8804 provides RESET_N input pin 37. (See Tab l e 8-1 .) This pin is used as a hardware Reset of the device and must adhere to the timing requirements detailed in the “Power Sequence Timing” and “Reset Pin Configuration Strap Timing” sections
  of the LAN8804 Data Sheet. Release from Reset is based on the RESET_N input pin transitioning from low to high.

TABLE 8-1: RESET PIN DESCRIPTION

Pin Name	Pin Number	Description
NRESET	37	Device Reset. This is an active-low input that powers down the device and sets all register bits to their default state.

8.2 PLL/Clocks

- The device provides the following PLLs:
  – System PLL: Generates the internal system clocks and clocks required for the internal See the “Sys- tem Clocks” section of the *LAN8804 Data Sheet* for additional information.

-1588 PLL: Generates the internal 1588 See the “1588 Clock” section of the *LAN8804 Data Sheet* for additional information.

– QSGMII SerDes MPLL: Generates the clocks needed by the See the “QSGMII SerDes Clock” sec- tion of the *LAN8804 Data Sheet* for additional information.

The reference clock selection of the System PLL and QSGMII SerDes MPLL are controlled via the **REF_CLK_SEL[1:0]** pins. Refer to “Miscellaneous Pins” table of the data sheet for detailed **REF_CLK_SEL[1:0]** set- ting information.

- The System PLL can use any of the following as its input reference clock:
  – 25 MHz crystal
  – 25 MHz system single-ended reference clock input
  – 125 MHz system differential clock inputs
- The System PLL generates the following clocks:
  – 250 MHz system clock
  – 25 MHz system clock
- The reference clock selection is controlled by the pin configurations shown in Table 8-2.

TABLE 8-2: REFERENCE CLOCK CONTROL

Description	Pin	Selection Control
Reference Clock Select	REF_CLK_SEL_0 pin 3 3 REF_CLK_SEL_1 pin 3 5	These pins control the reference clock selection of the Syst em PLL and QSGMII SerDes. MPLL. REF_CLK_SEL[1:0] 00 = SYSPLL Reference 25 M Hz from XI/XO, QSGMII Refer- ence 25 MHz from XI/XO 01 = RESERVED 10 = SYSPLL Reference 25 MHz from CK125_REF_INP/M, QSGMII Reference 125 MHz from CK 125_REF_INP/M 11 = RESERVED

Note

1. These are live pins and not configuration straps. They must be permanently tied high or low.
2. XI/XO can be a 25 MHz crystal or a 25 MHz external clock.
3. CK125_REF_INP/M is a 125 MHz external clock.
   • The 1588 reference clock input options are 10 MHz, 25 MHz, and 125 MHz.

8.3 Reference Resistor

Refer to Tab l e 8-3 for reference resistor pin details.

TABLE 8-3: REFERENCE RESISTOR PIN DESCRIPTION

Pin Name	Pin Number	Description
ISET	2	This pin must be connected to ground through a 6.04 kΩ, 1% resistor.
RES_REF	52	This pin must be connected to ground through a 200Ω, 1% 100 ppm/°C resis tor.

8.4 Test Mode

Refer to Tab l e 8-4 for Test mode pin details.

TABLE 8-4: TEST MODE PIN DESCRIPTION

Pin Name	Pin Number	Description
TESTMODE	38	For normal operation, this pin must be pulled down to ground. The JTAG func - tionality is selected when the **TESTMODE** (pin 38) is asserted.

8.5 LED Pins

- The device provides eight programmable LEDs, two per port (PORT[0:3]LED[1:2]), which are configurable to support multiple LED modes. The LED mode is configured by the LED_MODE configuration strap as well as port-specific instances of the LED Control Register 1 and 2. All eight LEDs are configured with identical behavior via the LED_MODE configuration strap. Port-specific LED configuration can be accomplished via the LED Control Register 1 and 2. The supported LED modes are:
  – Individual-LED Mode (LED Control Register 1, bit[6] = ‘1’, LED_MODE pulled-up)
  – Tri-color-LED Mode (LED Control Register 1, bit[6] = ‘1’, LED_MODE pulled-down)
  – Enhanced LED Mode (LED Control Register 1, bit[6] = ‘0’, LED_MODE unused)
- To use LEDs, they must be enabled as GPIOs and GPIO alternate functions. The GPIOs must be configured as outputs, and the proper output driver type must be selected (open-drain or push-pull). If open-drain type is selected, the output driver will automatically choose between open-source and open-drain based on LED polarity. The PORT[3:0]_LED[2:1]_POL configuration straps set the default polarity of the LED pins. Refer to the “LED Polarity (PORT[3:0]_LED[2:1]_POL)” section of the LAN8804 Data Sheet for additional LED polarity information. Refer to the “LED Mode Select (LED_MODE)” section of the LAN8804 Data Sheet for additional LED_MODE information.

8.6 LED MODE SELECT (LED_MODE)

- The LED_MODE configuration strap selects between Individual-LED (pulled-up) or Tri-color-LED (pulled-down) modes. All eight LEDs are configured with identical behavior. (See Ta b l e 8- 5 .) The LED_MODE configuration strap is sampled and latched at power-up/Reset and is defined as follows:
  – 0: Tri-color-LED mode
  – 1: Individual-LED mode
- LED operation is described in the “LEDs” section of the LAN8804 Data Sheet.

TABLE 8-5: GPIO LED FUNCTIONALITY

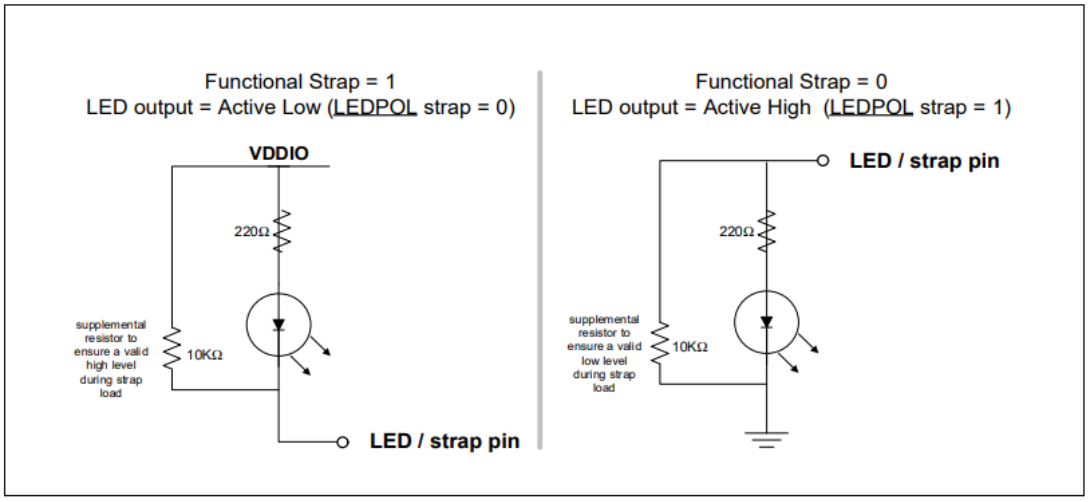
GPIO	Pin Number	Alternate Function	Configuration Strap
GPIO11	83	PORT0LED1	LED_MODE/PORT0_LED1_POL
GPIO12	84	PORT0LED2	PHYAD0/PORT0_LED2_POL
GPIO17	57	PORT1LED1	PORT1_LED1_POL
GPIO18	58	PORT1LED2	PORT1_LED2_POL
GPIO19	60	PORT2LED1	PORT2_LED1_POL
GPIO20	61	PORT2LED2	PORT2_LED2_POL
GPIO13	85	PORT3LED1	PHYAD1/PORT3_LED1_POL
GPIO14	86	PORT3LED2	PHYAD2/PORT3_LED2_POL

Note

1. To enable LED operation with either a pull-up or pull-down, LED Polarity takes on the inverted value of the register bit.
2. Using 330Ω to 510Ω current limit resistor and VDD25 for LED power are recommended.

FIGURE 8-1: PIN LED STRAPPING

FIGURE 8-1: PIN LED STRAPPING



8.7 Other Pins

- The COMA_MODE (pin 36) is designed to hold the PHY in a suspended state until system initialization is complete. When enabled by driving the COMA_MODE pin high, all the errors, alarms, link up/down notifications and more, are suppressed until COMA_MODE is driven low. This is useful in designs with multiple PHYs as it allows all errors to be suppressed until the entire board is configured. Coma mode operates as indicated in Tab l e 8-6 . There is no Register Control of the COMA mode pin in this device.
- Auto MDI/MDIX (Pair-Swap): The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the device and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner and assigns the MDI/MDI-X pair mapping of the device accordingly. Table 8-6 shows the device 10/100/1000 pin configuration assignments for MDI/MDI-X pin

mapping.

TABLE 8-6: MDI/MDI-X PIN MAPPING

Pin (RJ45 Pair)	MDI			MDI-X		
	1000BASE-T	100BASE-T	10BASE-T	1000BASE-T	100BASE-T	10BASE-T
TXRXP/M_A (1,2)	A+/–	TX+/–	TX+/–	A+/–	RX+/–	RX+/–
TXRXP/M_B (3,6)	B+/–	RX+/–	RX+/–	B+/–	TX+/–	TX+/–
TXRXP/M_C (4,5)	C+/–	Not Used	Not Used	C+/–	Not Used	Not Used
TXRXP/M_D (7,8)	D+/–	Not Used	Not Used	D+/–	Not Used	Not Used

8.8 Unused and No-Connection Pins

- The NC pins (pins 91 and 92) are unconnected pins. They must be left floating.

8.9 General External Pull-Up and Pull-Down Resistors

- If there is no pull-up resistor value specified, a 4.7 kΩ resistor is recommended.
- If there is no pull-down resistor value specified, a 1 kΩ or 4.7 kΩ resistor is recommended.

HARDW ARE CHECKLIST SUMMAR Y

TABLE 9-1:HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, “G eneral Con- si derations”	Section 2.1, “Required Reference s”	All necessary documents are on hand.		
	Section 2.2, “Pin Ch eck”	The pins match the data sheet.		
	Section 2.3, “Ground ”	Verify if a single ground reference as a system ground is used for all ground pins. Check if there is a ch assis ground for the line-side groun d.		
	Section 3.1, “Current Requirements”	Refer to Table 3-1 to ensure that th e power pins are correct. Select th e correct power supply components with at least about 25 % to 30% margin based on worst c ase for the system power design.		

Section 3.0, “Power”	Section 3.2, “Power Supply Planes”	When creating a PCB layout, refer to this section for power sup- ply plane design.		
	Section 3.3, “Power Circuit Connection and Analog Power Plane Filtering”	Refer to Figure 3-1 to check the power circuit connection, decoupling capacitors, and filtering.		
	Section 3.4, “Bulk Decoupling Capaci- tors”	When creating a PCB layout, refer to this section for the bulk decoupling capacitor required.		
Section 4.0, “Twisted Pair Media Interface”	Section 4.1, “10/100/1000 Mbps Inter- face Connection”	Verify all analog I/O pin connections for quad-port circuit design based on product design requirements to select the design of Figure 4-1.		
	Section 4.2, “Magnetics Connection and RJ45 Connection”	Verify the magnetics and the common-mode capacitors connec- tion based on Figure 4-1.		
	Section 4.3, “PCB Layout Considerations”	Refer to this section for PCB layout design reference to check if the Gigabit copper port PCB layout request is met.		
Section 5.0, “QSGMII/Q-USGMII MAC Interface”	Section 5.1, “QSGMII/Q-USGMII Pins and Connection”	Refer to this section for guidelines to ensure that the correct pins for QSGMII MAC interface are used in the design.		
	Section 5.2, “QSGMII MAC”	Refer to Figure 5-1 for QSGMII MAC interface to connect to four external QSGMII MACs in the design.		
	Section 5.3, “QSGMII MAC Design Rules”	Refer to this section for QSGMII MAC interface PCB design guidelines.		

Section 6.0, “Device Clocks”	Section 6.1, “Reference Clock”	Refer to this section when selecting the reference clock fre- quency and the correct reference clock pins in the design. Follow the layout required in PCB design.		
	Section 6.2, “System Clock and Syn- chronous Ethernet Connections”	Refer to this section for System Clock and Synchronous Ether- net connections. Verify the correct pin connections and follow the PCB Board layout recommendations.		

	Section 6.3, “Single-Ended REFCLK Input”	Refer to Figure 6-1 for single-ended reference input clock circuit design and use the correct resistor divider in the circuit based on Table 6-1 for correct resistor values.		
	Section 6.4, “Differential REFCLK Input”	Refer to Figure 6-2 for the differential reference input clock cir- cuit design.		
Section 7.0, “Digital Inter- face and I/O”	Section 7.1, “MIIM (MDIO) Interface”	Refer to this section for the MIIM interface circuit design.		
	Section 7.2, “GPIO Pins”	Check if the correct PHY address pins are used based on Table 7-1 to configure the correct PHY address the design requires.		
	Section 7.3, “JTAG Pins”	Refer to Table 7-2 and the descriptions in this section for all JTAG pins in the circuit design.		
Section 8.0, “Miscellaneous”	Section 8.1, “Reset”	Refer to Table 8-1 to use the correct Reset pin and check if the designed Reset circuit meets the Reset time requirement.		
	Section 8.2, “PLL/Clocks”	Refer to Table 8-2 to select the correct Reference Clock config- uration and ensure that the correct pins are connected.		
	Section 8.3, “Reference Resistor”	Refer to Table 8-3 to select the correct Reference Resistor bias- ing pins in the design. Make sure to connect a 6.04 kΩ 1% resistor between the **ISET** and **GND**. In addition, make sure to connect a 200 kΩ 1% resistor between **RES_REF** pin and **GND**.		
	Section 8.4, “Test Mode”	Check if correct **TESTMODE** pin setup is used based on Table 8-4.		
	Section 8.5, “LED Pins”	Check if correct LED pins are used based on Table 8-5, current limit resistors, and LED power.		
	Section 8.7, “Other Pins”	For **COMA_MODE**, check this section for the correct design.		
	Section 8.8, “Unused and No-Connec- tion Pins”	Verify if all reserved pins and NC pins are unconnected.		

	Section 8.9, “General External Pull-Up and Pull-Down Resistors”	Generally, it is recommended to us e 4.7 kΩ pull-up resistor and 1 kΩ pull-down resistor.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004536C (05-06-24)	Figure 5-1	Corrected the input and output pins.
	Section 6.2, “System Clock and Synchronous Ethernet Connections”	Removed the following statements from the section: •AC coupling with 0.1 pF capacitors is used. Capacito rs are best placed close to the reference clock input p ins. •For some clock drivers, the termination resistors are placed on the clock driver side. Termination resistors are not typically needed on the LAN8804 side of the c apacitors.
	Section 6.4, “Differential RE F- CLK Input”	Changed part of the introductory statement to “Differ ential clocks must be LVDS-compatible.”
	Figure 6-2	Changed figure title touREFCLK Differential Input.” C orrected the diagram by removing capacitors and add ing a 1000 differential resistor.
	Table 9-1	Changed figure cross-reference to Figure 6-2. Chang ed explanation on Section 6.4, “Differential REFCLK I nput” to “Refer to Figure 6-1 for the differential refere nce input clock circuit design.”
DS000045366 ,(05-22-2 3)	Section 5.2, “QSGMII MAC”	Updated the first bullet item in the section.
	Figure 8-1	Updated the figure.
	All	Very minor text changes throughout.
DS00004536A (04-29-22)	Initial release	

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	MICROCHIP LAN8804 4-Port Gigabit Ethernet Transceiver [pdf] User Guide LAN8804, LAN8804 4-Port Gigabit Ethernet Transceiver, 4-Port Gigabit Ethernet Transceiver, Gigabit Ethernet Transceiver, Ethernet Transceiver, Transceiver

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- User Manual