MICROCHIP IP RX DisplayPort Tx Sources User Guide

Contents

IP RX DisplayPort Tx Sources

Display Port RX IP User Guide

Introduction (Ask a Question)

DisplayPort Rx IP is designed to receive video from DisplayPort Tx sources. It is targeted for the PolarFire® FPGA applications and implemented based-on the Video Electronics Standards Association (VESA) DisplayPort Standard 1.4 protocol. For more information on VESA protocol, see VESA. It supports standard rates of 1.62, 2.7, 5.4, and 8.1 Gbps for displays.

Summary (Ask a Question)

The following table provides a summary of the DisplayPort Rx IP characteristics.

Table 1. Summary

Core Version	This document applies to DisplayPort Rx v2.1.
Supported Device Families	PolarFire® SoC PolarFire
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Licensing	The core is license-locked for clear text RTL. It supports the generation of encrypted RTL for the Verilog version of core with no license.

Features (Ask a Question)

The key features of DisplayPort Rx are listed as follows:

- Support 1, 2, or 4 Lanes
- Support 6, 8, and 10 Bits Per Component
- Support Up to 8.1 Gbps Per Lane
- Support DisplayPort 1.4 Protocol
- Only Support a Single Video Stream or SST Mode, and the MST Mode is not Supported
- Audio Transmission is not Supported

Device Utilization and Performance (Ask a Question)

The following table lists the utilization and performance of the device.

Table 2. Device Utilization and Performance

Family	Device	LUTs	DFF	Performance (MHz)	LSRAM	µSRAM	Math Blocks	Chip Global
PolarFire®	MPF300T	30652	14123	200	28	32	0	2

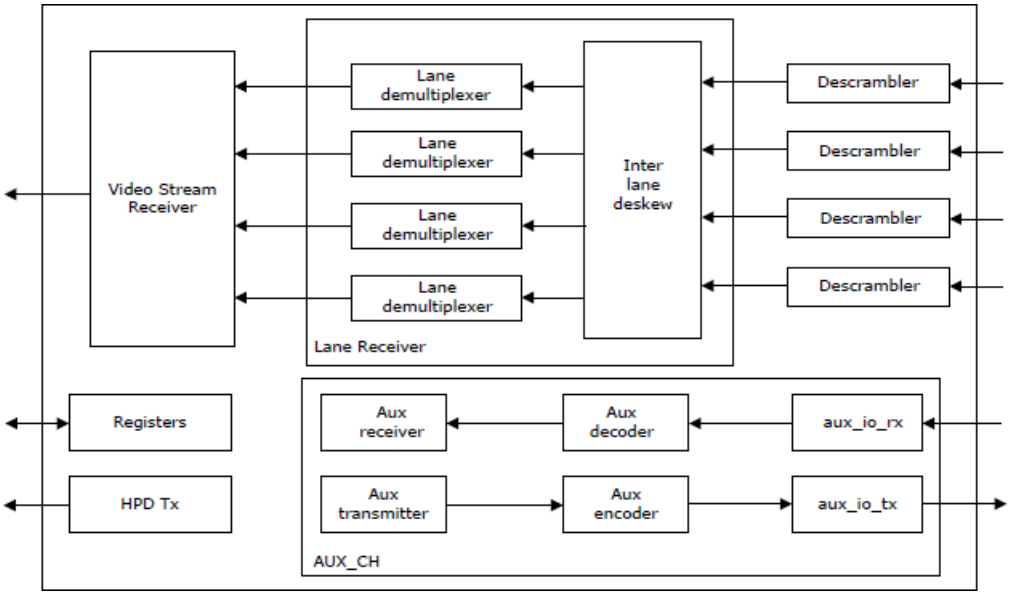
User Guide

DS50003546A – 1

1. Hardware Implementation (Ask a Question)

The following figure shows the DisplayPort Rx IP implementation.

Figure 1-1. DisplayPort Rx IP Implementation



DisplayPort Rx IP includes the following:

- Descrambler module
- Lane receiver module
- Video Stream Receiver module
- AUX_CH module

Descrambler de-scrambles the input lane data. Lane receiver demultiplexes all kinds of data on each lane. The Video Stream Receiver gets video pixels from the lane receiver, it recovers the video stream signal. AUX_CH module receives the AUX Request command from DisplayPort source device and transmits AUX Reply to DisplayPort source device.

1.1 Functional Description (Ask a Question)

This section describes the function description of the DisplayPort Rx IP.

HPD

The DisplayPort Rx IP outputs the HPD signal according to the DisplayPort sink application software settings. After the DisplayPort Rx IP is ready, the DisplayPort sink application software must set the HPD signal to 1. When it expects the DisplayPort source device to re-read the sink device status or re-training, the DisplayPort sink application software must set an HPD to generate the HPD interrupt signal.

AUX Channel

The DisplayPort source device communicates the DisplayPort sink through an AUX Channel. The source device sending request transaction to the sink device and the sink device sending Reply transaction to source Device. DisplayPort Rx implements the AUX transaction transmitter and receiver. For AUX transaction transmitter, the DisplayPort sink application software provides all the AUX transaction content bytes, the DisplayPort Rx IP generate the transaction bitstream. For the AUX transaction receiver, DisplayPort Rx IP receives the transaction and extracts all the bytes to the DisplayPort application software. The Link Policy Maker and the Stream Policy Maker must be implemented in the DisplayPort application software.

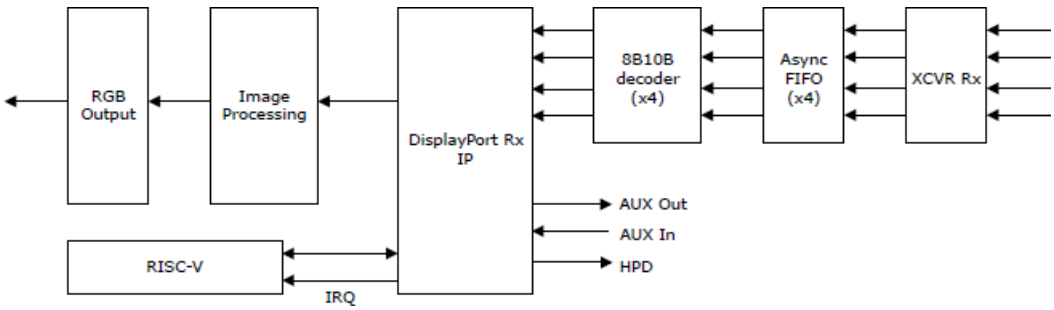
Video Stream Transmission

The DisplayPort Rx IP supports RGB 4:4:4, and only supports a single video stream. After training is done and the video stream is ready, the DisplayPort Rx IP starts to transmit video stream. After training, the DisplayPort Rx IP must be enabled for video receive. The DisplayPort Rx IP does not include a video clock recovery function. The user must recover the video clock outside the DisplayPort Rx IP or use a fixed high enough frequency clock to output the video stream data.

DisplayPort Rx IP Application

2. DisplayPort Rx IP Application (Ask a Question) The following figure shows the typical DisplayPort Rx IP application.

Figure 2-1. Typical application for DisplayPort Rx IP



As shown in the preceding figure, the transceiver block receives four lanes data. There are four asynchronous FIFO to synchronize all lanes data into one clock domain. These four lanes data are decoded to 8B code in the 8B10B decoder modules. The DisplayPort Rx IP gets lanes 8B data and output video stream data; it also works with the RISC-V software to finish the training and Link Policy Maker. The recovered video stream data is processed in the Image Processing module and generates output on the RGB output interface.

3. DisplayPort Rx Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the DisplayPort Tx GUI configurator and I/O signals.

3.1 Configuration Settings (Ask a Question)

The following table lists the description of the configuration parameters used in the hardware implementation of DisplayPort Rx. These are generic parameters and varied as per the requirement of the application.

Table 3-1. Configuration Parameters

Name	Default	Description
Line Buffer Depth	2048	Output line buffer depth It must be greater than line pixel number
Number of lanes	4	Supports 1, 2, and 4 lanes

3.2 Inputs and Outputs Signals (Ask a Question)

The following table lists the input and output ports of DisplayPort Rx IP.

Table 3-2. Input and Output Ports of DisplayPort Rx IP

Interface	Width		Direction Description
vclk_i	1	Input	Video clock
dpclk_i	1	Input	DisplayPort IP working clock It is DisplayPortLaneRate/40 For example, DisplayPort lane rate is 2.7 Gbps, dpclk_i is 2.7 Gbps/40 = 67.5 MHz

aux_clk_i	1	Input	AUX Channel clock, it is 100 MHz
pclk_i	1	Input	APB interface clock
prst_n_i	1	Input	Low-active reset signal synchronized with pclk_i
paddr_i	16	Input	APB address
pwrite_i	1	Input	APB write signal
psel_i	1	Input	APB select signal
penable_i	1	Input	APB enable signal
pwdata_i	32	Input	APB writing data
prdata_o	32	Output	APB reading data
pready_o	1	Output	APB reading data ready signal
int_o	1	Output	Interrupt signal to CPU
vsync_o	1	Output	VSYNC for output video stream It is synchronous with vclk_i.
hsync_o	1	Output	HSYNC for output video stream It is synchronous with vclk_i.
pixel_val_o	1/2/4	Output	Indicates the validation of pixels on pixel_data_o port, synchronous with vclk_i

DisplayPort Rx Parameters and Interface Signals

……..continued			
Interface	Width	Direction	Description
pixel_data_o	48/96/192	Output	Output video stream pixel data, it could be 1, 2, or 4 parallel pixels. it is synchronous with vclk_i. For 4 parallel pixels, • bit[191:144] for 1st pixel • bit[143:96] for 2nd pixel • bit[95:48] for 3rd pixel • bit[47:0] for 4th pixel Each pixel uses 48 bits, for RGB, bit[47:32] is R, bit[31:16] is G, bit[15:0] is B. Each color component uses the lowest BPC bits. For example, RGB with 24 bits per pixel, bit[7:0] is B, bit[23:16] is G, bit[39:32] is R, all other bits are reserved.
hpd_o	1	Output	HPD output signal
aux_tx_en_o	1	Output	AUX Tx data enable signal
aux_tx_io_o	1	Output	AUX Tx data
aux_rx_io_i	1	Input	AUX Rx data

dp_lane_k_i	Number of lanes * 4	Input	DisplayPort input lanes data K indication It is synchronous with dpclk_i. • Bit[15:12] for Lane0 • Bit[11:8] for Lane1 • Bit[7:4] for Lane2 • Bit[3:0] for Lane3
dp_lane_data_i	Number of lanes*32	Input	DisplayPort input lanes data It is synchronous with dpclk_i. • Bit[127:96] for Lane0 • Bit[95:64] for Lane1 • Bit[63:32] for Lane2 • Bit[31:0] for Lane3
mvid_val_o	1	Output	Indicates if mvid_o and nvid_o is available, it is synchronous with dpclk_i.
mvid_o	24	Output	Mvid It is synchronous with dpclk_i.
nvid_o	24	Output	Nvid It is synchronous with dpclk_i.
	xcvr_rx_ready_i Number of lanes	Input	Transceiver ready signals

pcs_err_i	Number of lanes	Input	Core Pcs decoder error signals
pcs_rstn_o	1	Output	Core Pcs decoder reset
lane0_rxclk_i	1	Input	Lane0 clock from Transceiver
lane1_rxclk_i	1	Input	Lane1 clock from Transceiver
lane2_rxclk_i	1	Input	Lane2 clock from Transceiver
lane3_rxclk_i	1	Input	Lane3 clock from Transceiver

4. Timing Diagrams (Ask a Question)

As shown in the figure, hsync_o is asserted for several cycles before each line. If there are n lines in a video frame, there are n hsync_o asserted. Before the first line and the first asserted hsync_o, vsync_o is asserted for several cycles. The position and width of VSYNC and HSYNC are configured by software.

Figure 4-1. Timing Diagram for Output Video Stream Interface Signal

5. DisplayPort Rx IP Configuration (Ask a Question)

This section describes the various DisplayPort Rx IP configuration parameters.

5.1 HPD (Ask a Question)

When the DisplayPort sink device is ready and connected to the DisplayPort source device, the DisplayPort sink application software must assert the HPD signal to 1 by writing 0x01 into register 0x0140. The DisplayPort sink application software must monitor the status of the sink device. If the sink device needs a source device to read the DPCD registers, the sink device software must send an HPD interrupt by writing 0x01 into register 0x0144, then write 0x00 into 0x0144.

5.2 Receive AUX Request Transaction (Ask a Question)

When the DisplayPort Rx IP received an AUX Request transaction and interrupt is enabled, the software must receive the NewAuxReply event interrupt. The software must perform the following steps to read the received AUX Request transaction from the DisplayPort IP:

1. Read register 0x012C to know the length (RequestBytesNum) of the received AUX transaction.

2. Read register 0x0124 RequestBytesNum times to get all the bytes of the received AUX transaction.

3. AUX Request transaction COMM[3:0] is the first reading byte bit [7:4].

4. DPCD address is ((FirstByte[3:0]<<16) | (SecondByte[7:0]<<8) | (ThirdByte[7:0])).

5. AUX Request Length field is FourthByte[7:0].

6. For DPCD writing Request transaction, all the bytes after the length field are writing data. 5.3 Transmit AUX Reply Transaction (Ask a Question)

After receiving an AUX Request transaction, the software must configure the DisplayPort Rx IP to transmit an AUX Reply transaction as soon as possible. The software is responsible to determine all the Reply transaction bytes, which includs the Reply type.

To transmit an AUX Reply, software must perform the following steps:

1. If AUX Reply transaction including DPCD reading data, write all the read data into register 0x010C byte by byte. If no DPCD reading data to be transmitted, skip this step.

2. Determine how many DPCD reading bytes (AuxReadBytesNum). If no DPCD reading bytes, AuxReadBytesNum is 0.

3. Determine the AUX Reply type (ReplyComm).

4. Write ((AuxReadBytesNum<<16) | ReplyComm) into register 0x0100.

5.4 DisplayPort Lanes Training (Ask a Question)

At the first training stage, the DisplayPort source device transmits TPS1 to make the attached DisplayPort sink device to get LANEx_CR_DONE.

At the second training stage, the DisplayPort source device transmits TPS2/TPS3/TPS4 to get the attached DisplayPort sink device to get LANEx_EQ_DONE, LANEx_SYMBOL_LOCKED, and INTERLANE_ALIGN_DONE.

LANEx_CR_DONE indicates that the FPGA Transceiver CDR is locked. LANEx_SYMBOL_LOCKED indicates that the 8B10B decoder decodes 8B bytes correctly.

Before the training procedure, the DisplayPort sink application software must let the source device. The DisplayPort Rx IP supports TPS3 and TPS4.

When the source device is sending TPS3/TPS4 (source device writes DPCD_0x0102 to indicate TPS3/ TPS4 transmission), the software must perform the following steps to check if training is done:

DisplayPort Rx IP Configuration

1. Write enabled lanes number into register 0x0000.

2. Write 0x00 into register 0x0014 to disable descrambler for TPS3. Write 0x01 to enable descrambler for TPS4.

3. Waiting until the source device reads DPCD_0x0202 and DPCD_0x0203 DPCD registers.

4. Read register 0x0038 to know if the DisplayPort Rx IP lanes have received TPS3. Set LANEx_EQ_DONE to 1 when TPS3 is received.

5. Read register 0x0018 to know if all lanes are aligned. Set INTERLANE _ALIGN_DONE to 1 if all lanes are aligned.

In the training procedure, the software might need to configure the Transceiver SI settings and Transceiver lane rate.

5.5 Video Stream Receiver (Ask a Question)

After training is completed, the DisplayPort Rx IP must enable the video stream receiver. To enable the video receiver, the software must perform the following configuration:

1. Write 0x01 into register 0x0014 to enable descrambler.

2. Write 0x01 into register 0x0010 to enable video stream receiver.

3. Read MSA from register 0x0048 to register 0x006C until meaningfully MSA values are found.

4. Write FrameLinesNumber into register 0x00C0. Write LinePixelsNumber into register 0x00D8. For example, if we know that it is 1920×1080 video stream from MSA, then write 1080 into register 0x00C0 and write 1920 into register 0x00D8.

5. Read register 0x01D4 to check if the recovered video stream frame has expected HWidth and expected VHeight.

6. Read register 0x01F0 to clear and discard the reading value because this register records the status from the last reading.

7. Waiting for about 1 second or several seconds, Read register 0x01F0 again. Checking bit [5] to check if the recovered video stream HWidth is locked. 1 means unlocked and 0 means locked. Checking bit [21] to check if recovered the video stream VHeight is locked. 1 means unlocked and 0 means locked.

5.6 Register Definition (Ask a Question)

The following table shows the internal registers defined in DisplayPort Tx IP.

Table 5-1. DisplayPort Rx IP Registers

Address	Bits	Name		Type	Default	Description
0x00000	[2:0]	Enabled_Lanes_Number		RW	0x4	Enabled lanes number 4 lanes, 2 lanes, or 1 lane
0x00004	[2:0]	Out_Parallel_Pixel_Number		RW	0x4	The number of parallel pixels at video stream output interface
0x00010	[0]	Video_Stream_Enable		RW	0x0	Enable video stream receiver
0x00014	[0]	Descramble_Enable		RW	0x0	Enable descrambler
0x00018	[0]	InterLane_Alignment_Status RO			0x0	Indicates if lanes are aligned
0x001C	[1]	Alignment_Error		RC	0x0	Indicates if there is error in alignment procedure
	[0]	New_Alignement		RC	0x0	Indicates if there was a new alignment event. When lanes are not aligned, a new alignment is expected. When lanes are aligned and there was a new alignment, it means lanes are out of alignment and aligned again.
0x00038		[14:12] Lane3_RX_TPS_Mode		RO	0x0	Lane3 received TPSx mode. 2 means TPS2, 3 means TPS3, and 4 means TPS4.

DisplayPort Rx IP Configuration

……..continued Address	Bits	Name	Type	Default	Description
	[10:8]	Lane2_RX_TPS_Mode	RO	0x0	Lane2 received TPSx mode
	[6:4]	Lane1_RX_TPS_Mode	RO	0x0	Lane1 received TPSx mode
	[2:0]	Lane0_RX_TPS_Mode	RO	0x0	Lane0 received TPSx mode
0x0044	[7:0]	Rx_VBID	RO	0x00	Received VBID
0x0048	[15:0]	MSA_HTotal	RO	0x0	Received MSA_HTotal
0x004C	[15:0]	MSA_VTotal	RO	0x0	Received MSA_VTotal
0x0050	[15:0]	MSA_HStart	RO	0x0	Received MSA_HStart
0x0054	[15:0]	MSA_VStart	RO	0x0	Received MSA_VStart
0x0058	[15]	MSA_VSync_Polarity	RO	0x0	Received MSA_VSYNC_Polarity
	[14:0]	MSA_VSync_Width	RO	0x0	Received MSA_VSYC_Width
0x005C	[15]	MSA_HSync_Polarity	RO	0x0	Received MSA_HSYNC_Polarity

	[14:0]	MSA_HSync_Width	RO	0x0	Received MSA_HSYNC_Width
0x0060	[15:0]	MSA_HWidth	RO	0x0	Received MSA_HWidth
0x0064	[15:0]	MSA_VHeight	RO	0x0	Received MSA_VHeight
0x0068	[7:0]	MSA_MISC0	RO	0x0	Received MSA_MISC0
0x006C	[7:0]	MSA_MISC1	RO	0x0	Received MSA_MISC1
0x00C0	[15:0]	Video_Frame_Line_Number	RW	0x438	The number of lines in a received video frame
0x00C4	[15:0]	Video_VSYNC_Width	RW	0x0004	Defines the output video VSYNC width in vclk_i cycles
0x00C8	[15:0]	Video_HSYNC_Width	RW	0x0004	Defines the output video HSYNC width in vclk_i cycles
0x00CC	[15:0]	VSYNC_To_HSYNC_Width	RW	0x0008	Defines the distance between VSYNC and HSYNC in vclk_i cycles
0x00D0	[15:0]	HSYNC_To_Pixel_Width	RW	0x0008	Defines the distance between HSYNC and first line pixel in cycles
0x00D8	[15:0]	Video_line_pixels	RW	0x0780	The number of pixels in a received video line
0x0100		[23:16] AUX_Tx_Data_Byte_Num	RW	0x00	The number of DPCD reading data bytes in the AUX Reply
	[3:0]	AUX_Tx_Command	RW	0x0	The Comm[3:0] in AUX Reply (Reply Type)

0x010C	[7:0]	AUX_Tx_Writing_Data	RW	0x00	Write all DPCD reading data bytes for the AUX Reply
0x011C	[15:0]	Tx_AUX_Reply_Num	RC	0x0	The number of AUX Reply transactions to be transmitted
0x0120	[15:0]	Rx_AUX_Request_Num	RC	0x0	The number of AUX Request transactions to be received
0x0124	[7:0]	AUX_Rx_Read_Data	RO	0x00	Read all bytes of received AUX Request transaction
0x012C	[7:0]	AUX_Rx_Request_Length	RO	0x00	The number of bytes in the received AUX Request transaction
0x0140	[0]	HPD_Status	RW	0x0	Set HPD output value
0x0144	[0]	Send_HPD_IRQ	RW	0x0	Write to 1 to send a HPD interrupt
0x0148	[19:0]	HPD_IRQ_Width	RW		0x249F0 Defines the HPD IRQ low-active pulse width in aux_clk_i cycles
0x0180	[0]	IntMask_Total_Interrupt	RW	0x1	Interrupt Mask: total interrupt
0x0184	[1]	IntMask_NewAuxRequest	RW	0x1	Interrupt Mask: Received new AUX Request
	[0]	IntMask_TxAuxDone	RW	0x1	Interrupt Mask: Transmit AUX Reply done
0x01A0	[15]	Int_TotalInt	RC	0x0	Interrupt: total interrupt
	[1]	Int_NewAuxRequest	RC	0x0	Interrupt: Received new AUX Request

	[0]	Int_TxAuxDone	RC	0x0	Interrupt: Transmit AUX Reply done
0x01D4		[31:16] Video_Output_LineNum	RO	0x0	The number of lines in an output video frame
	[15:0]	Video_Output_PixelNum	RO	0x0	The number of pixels in an output video line
0x01F0	[21]	Video_LineNum_Unlock	RC	0x0	1 means output video frame lines number is not locked
	[5]	Video_PixelNum_Unlock	RC	0x0	1 means output video pixels number is not locked

5.7 Driver Configuration (Ask a Question)

You can find the driver files in the following

path: ..\<Project_name>\component\Microchip\SolutionCore\dp_receiver\<DisplayPo rt Rx IP version>\Driver.

Testbench

6. Testbench (Ask a Question)

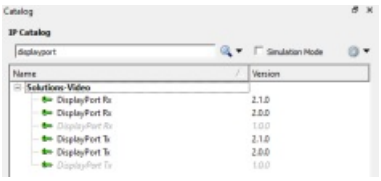
Testbench is provided to check the functionality of the DisplayPort Rx IP. DisplayPort Tx IP is used to verify the DisplayPort Rx IP functionality.

6.1 Simulation Rows (Ask a Question)

To simulate the core using the testbench, perform the following steps:

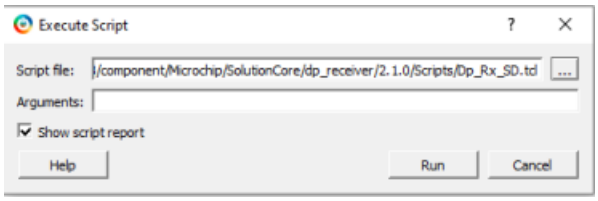
1. In the Libero SoC Catalog (View > Windows > Catalog), expand Solutions-Video , drag-and-drop the DisplayPort Rx, and then click OK. See the following figure.

Figure 6-1. Display Controller in Libero SoC Catalog



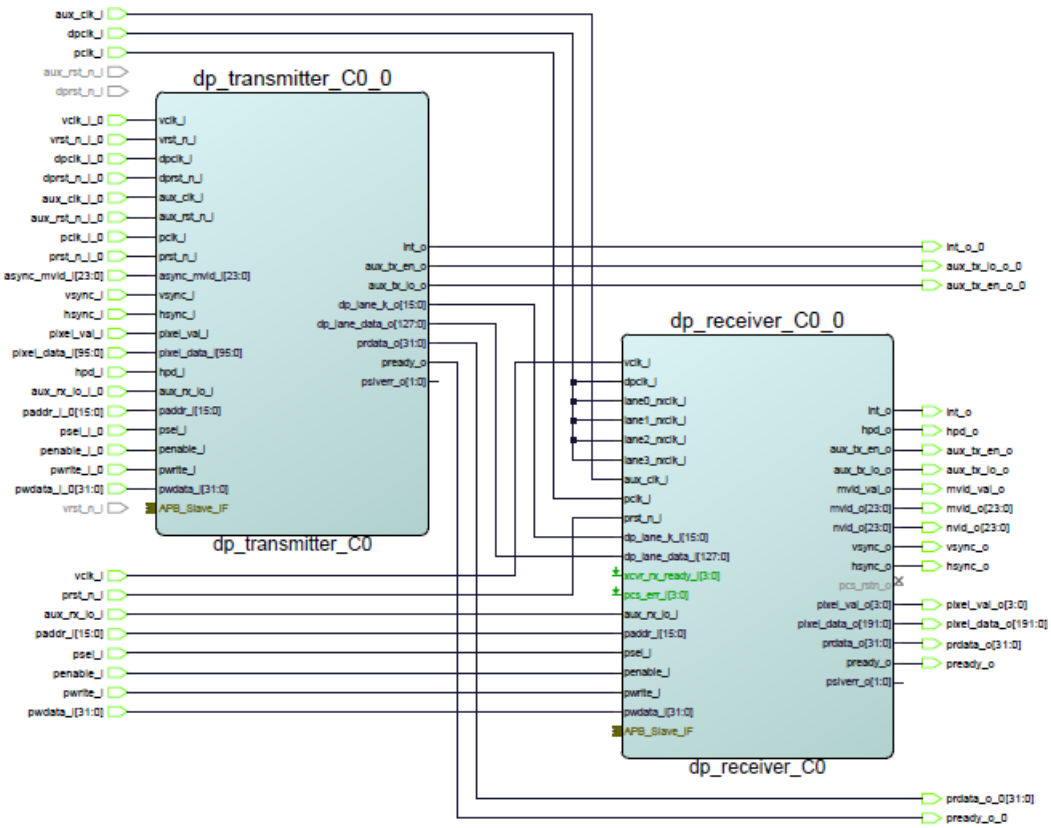
2. SmartDesign consists of DisplayPort Tx and DisplayPort Rx interconnections. To generate the SmartDesign for the DisplayPort Rx IP simulation, click Libero Project > Execute script. Browse to script ..\ <Project_name>\component\Microchip\SolutionCore\dp_receiver\ <DisplayPort Rx IP version>\scripts\Dp_Rx_SD.tcl, and then click Run .

Figure 6-2. Execute Script for DisplayPort Rx IP



The SmartDesign appears. See the following figure.

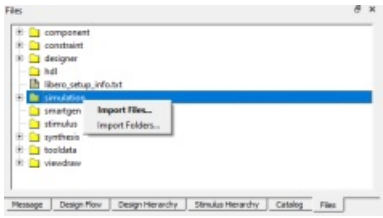
Figure 6-3. SmartDesign Diagram



3. On the Files tab, click simulation > Import Files. Figure 6-4. Import Files

dp_receiver_C0

prdata_o_0[31:0] pready_o_0



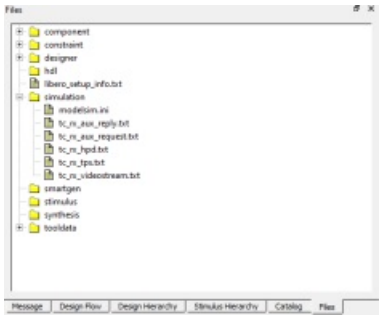
4. Import the tc_rx_videostream.txt, tc_rx_tps.txt, tc_rx_hpd.txt, tc_rx_aux_request.txt, and tc_rx_aux_reply.txt file from the

following path: ..\<Project_name>\component\Microchip\SolutionCore\ dp_receiver\<DisplayPort Rx IP version>\Stimulus.

5. To import a different file, browse the folder that contains the required file, and click Open. The imported file is listed under simulation, see the following figure.

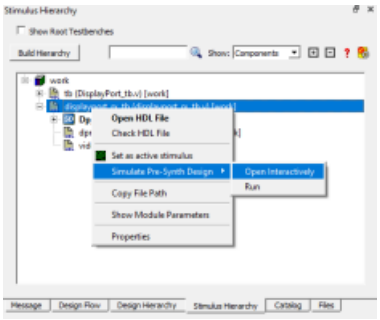
Testbench

Figure 6-5. Imported Files List in Simulation Folder



6. On the Stimulus Hierarchy tab, click displayport_rx_tb (displayport_rx_tb. v). Point to Simulate Pre-Synth Design, and then click Open Interactively

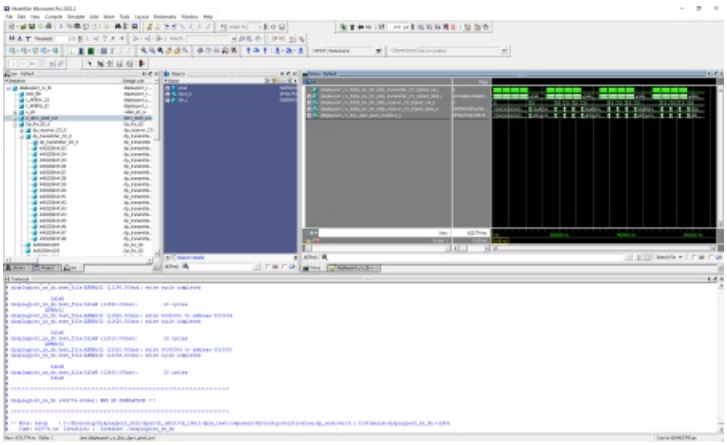
Figure 6-6. Simulating Testbench



ModelSim opens with the testbench file as shown in the following figure.

Testbench

Figure 6-7. DisplayPort Rx ModelSim Waveform



Important: If the simulation is interrupted due to the runtime limit specified in the DO file, use the run -all command to complete the simulation.

7. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 7-1. Revision History

Revision	Date	Description
A	06/2023	Initial release of document.

User Guide

DS50003546A – 17

Microchip FPGA Support

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

• From North America, call 800.262.1060

• From the rest of the world, call 650.318.4460

• Fax, from anywhere in the world, 650.318.8044

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

• Product Support – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software

• General Technical Support – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing

• Business of Microchip – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions. Customer Support

Users of Microchip products can receive assistance through several channels: • Distributor or Representative

• Local Sales Office

• Embedded Solutions Engineer (ESE)

• Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

• Microchip products meet the specifications contained in their particular Microchip Data Sheet.

• Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.

• Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.

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DS50003546A – 21

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