MICROCHIP Interface v1.1 T Format Interface

MICROCHIP Interface v1.1 T Format Interface User Guide

Contents

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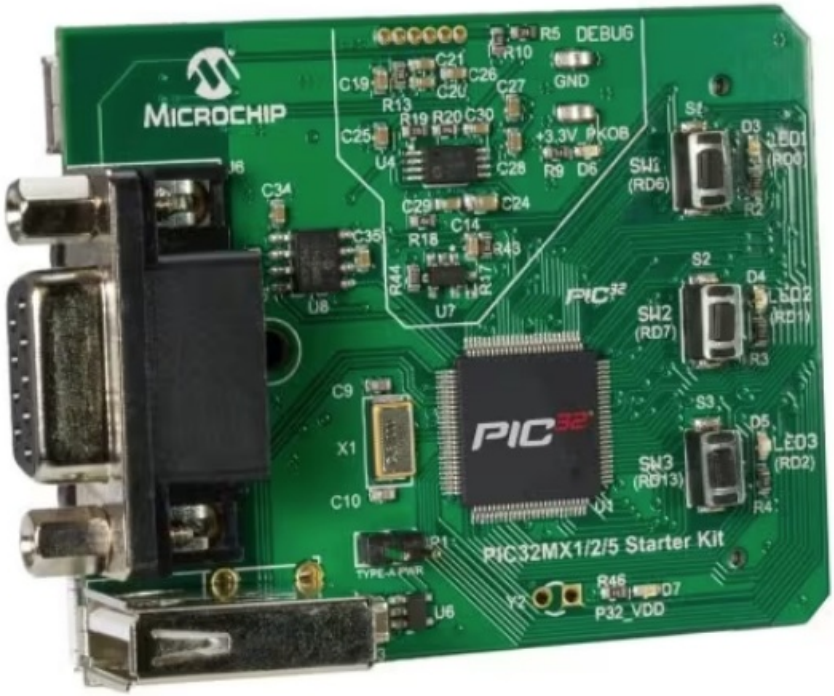


Product Information

- **Specifications**
  - **Core Version:** T-Format Interface v1.1
  - **Supported Device Families:** PolarFire MPF300T
  - **Supported Tool Flow:** Libero software
  - **Licensing:** Encrypted RTL code provided, must be purchased separately
  - **Performance:** 200 MHz

Product Usage Instructions

- **Installation of IP Core**
  - **To install the IP core in Libero SoC software:**
    - Update IP Catalog in Libero SoC software.
    - Download the IP core from the catalogue if not updated automatically.
    - Configure, generate and instantiate the core within the SmartDesign tool for project inclusion.
- **Device Utilization**
  - **The T-Format Interface utilizes resources as follows:**
    - **LUTs:** 236
    - **DFF:** 256
    - **Performance (MHz):** 200
- **User Guide and Documentation**
  - Refer to the provided user guide for detailed information on T-Format Interface parameters, interface signals, timing diagrams, and testbench simulation.

FAQs

- **Q: How to obtain the licensing for T-Format Interface?**

- **A:** The T-Format Interface is licensed with encrypted RTL that needs to be purchased separately. For more information, refer to the T-Format Interface documentation.

- **Q: What are the key features of the T-Format Interface?**
  - **A:** The key features of the T-Format Interface include the implementation of IP Core in Libero Design Suite and compatibility with various Tamagawa products such as rotary encoders.

Introduction

(Ask a Question).

The T-Format interface IP has been designed to provide an interface for the FPGAs to communicate with various compliant **Tamagawa** products such as rotary encoders.

Summary
The following table provides a summary of the T-Format interface characteristics.

Table 1. T-Format Interface Characteristics.

Core Version	This document applies to T-Format Interface v1.1.
Supported Device	• PolarFire® SoC
Families	• PolarFire
	• RTG4™
	• IGLOO® 2
	• SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v11.8 or later releases.
Licensing	Complete encrypted RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout are performed with Libero software. T-Format Interface is licensed with encrypted RTL that must be purchased separately. For more information, see **T-Format Interface**.

Features

- T-Format Interface has the following key features:
- Transmits and receives serial data from the physical layer (RS-485 interface)
- Aligns data as per T-Format and provides this data as registers that are read by subsequent blocks
- Checks for errors, such as parity, Cyclic Redundancy Check (CRC) mismatch, transmit errors, and so on, are reported by the external device
- Provides an alarm function that is triggered if the number of fault occurrences exceeds a configured threshold
- Provides ports for an external CRC generator block so that the user modifies the CRC polynomial if necessary

Implementation of IP Core in Libero Design Suite

- IP core must be installed in the IP Catalog of the Libero SoC software.
- This is done automatically through the IP Catalog update function in the Libero SoC software, or the IP core is manually downloaded from the catalogue.
- Once the IP core is installed in the Libero SoC software IP Catalog, the core is configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero project list.

Device Utilization and Performance

The following table lists the device utilization used for the T-Format Interface.
Table 2. T-Format Interface Utilization

Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T	248	256	200	0	0	0	0
PolarFire	MPF300T	236	256	200	0	0	0	0
SmartFusion® 2	M2S150	248	256	200	0	0	0	0

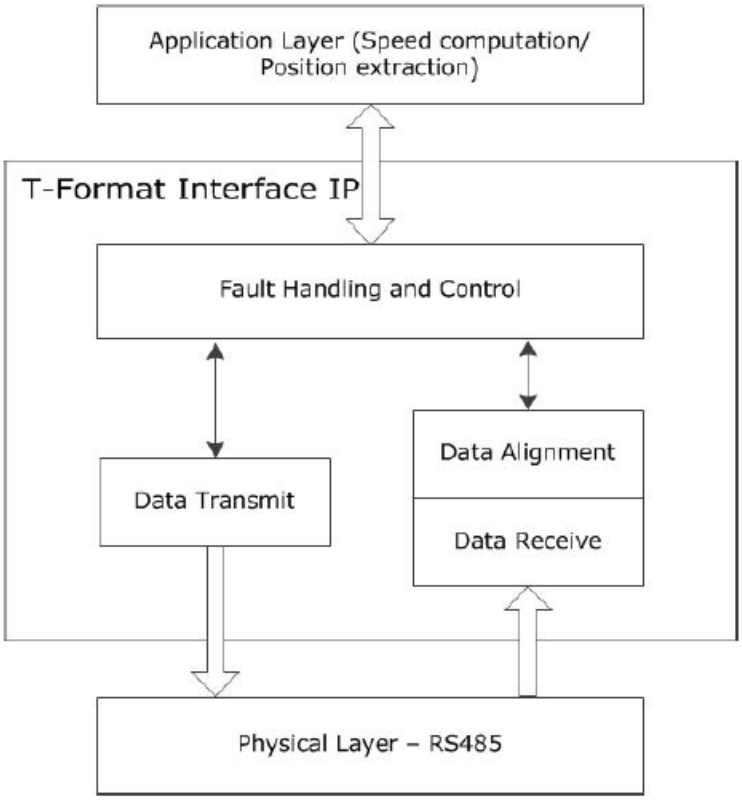
Important:

1. The data in this table is captured using typical synthesis and layout settings. CDR reference clock source was set to Dedicated with other configurator values unchanged.
2. The clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers.

Functional Description

- This section describes the implementation details of the T-Format Interface.
- The following figure shows the top-level block diagram of the T-Format Interface.

Figure 1-1. Top Level Block Diagram of T-Format Interface IP



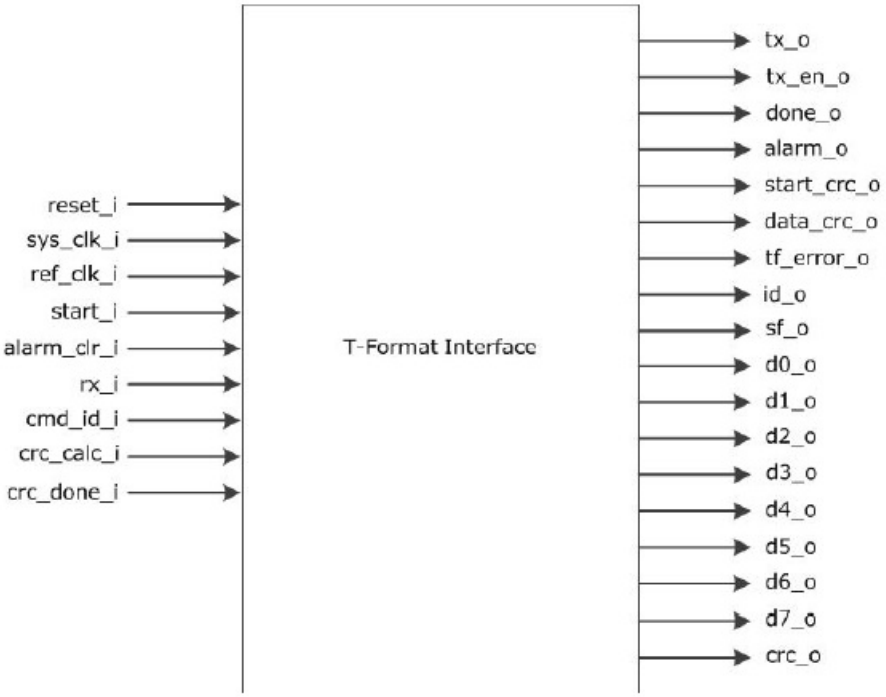
For complete details on T-Format, see **Tamagawa**. datasheets. The following table lists the various commands that are used to request data from the external device and their functions, and the number of data fields returned for each command.

Table 1-1. Commands for Control Field

Command ID	Function	Number of Data Fields in Received Frame
0	Rotor Angle (Data Read)	3
1	Multiturn data (Data Read)	3
2	Encoder ID (Data Read)	1
3	Rotor Angle and Multiturn data (Data Read)	8
7	Reset	3
8	Reset	3
C	Reset	3

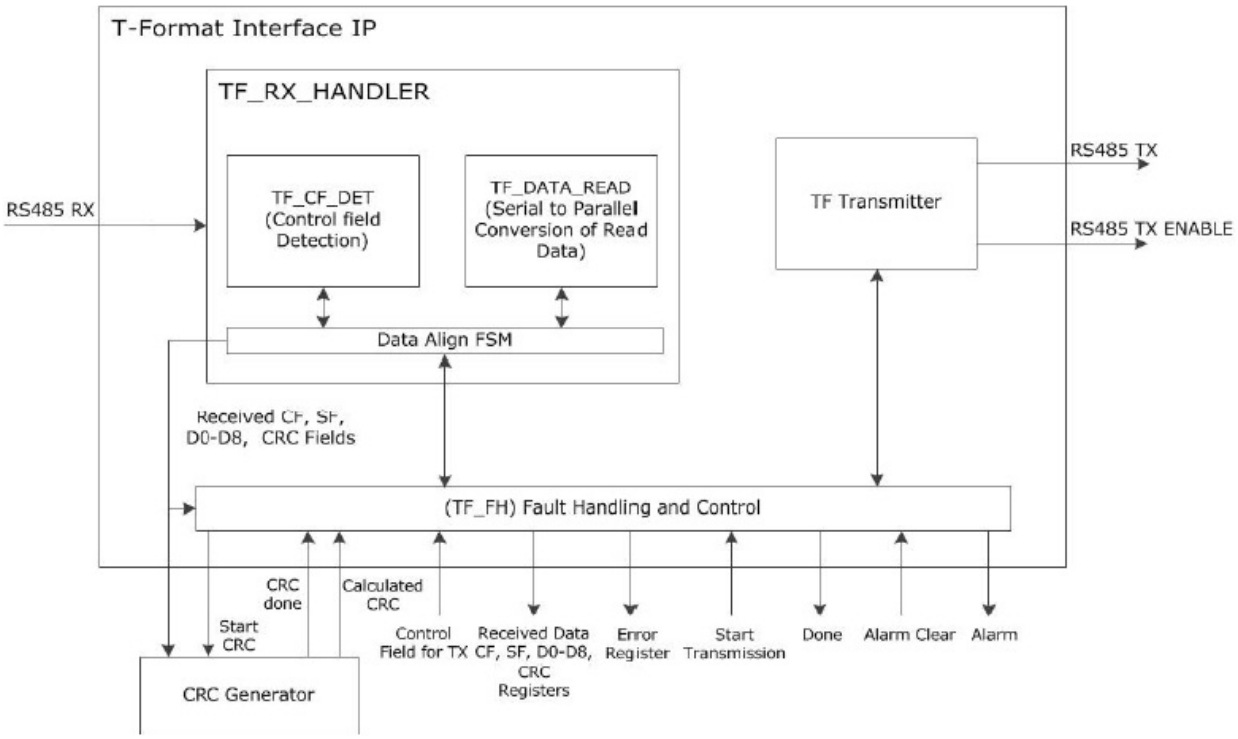
The following figure shows the system-level block diagram of the T-Format Interface.

Figure 1-2. System-Level Block Diagram of T-Format Interface



Thefollowing figure shows the functional block diagram of the T-Format interface.

Figure 1-3. FunctionalBlock Diagram of T-Format Interface IP



Each communication transaction in T-Format starts with a transmission of Control Frame (CF) from the requestor, followed by a frame received from the external device. The TF Transmitter block generates serial data to be sent to the external device. It also generates an optional tx_en_o signal required by some RS-485 converters. The encoder receives the data transmitted and transmits a frame of serial data to the IP, which is received in the rx_i input port of the IP block. The TF_CF_DET block first detects the control field and identifies the ID value. The data length is determined based on the received ID value, and subsequent fields are received and stored in respective registers using the TF_DATA_READ block. After the complete data is stored, the data in all fields except the CRC field is sent to an external CRC generator block, and the calculated CRC generated by this block is compared to the CRC received. Some of the other errors are also checked, and the done_o signal is asserted (‘1’ for one sys_clk_i cycle) after every error-free transaction.

Error Handling

- **The block identifies the following errors:**
  - Parity error in the received control field
  - Bad start sequence in received control field
  - Incomplete message where the RX line is stuck at 0 or stuck at 1
  - CRC mismatch between data in the received CRC field, and calculated CRC
  - Transmit Errors such as parity error or delimiter error in transmitted CF, as read from bit 6 and bit 7 of the status field (see Tamagawa datasheet).

These errors, when identified by the block, result in a fault counter getting incremented. When the fault counter value exceeds the configured threshold value (configured using g_FAULT_THRESHOLD), the alarm_o output is asserted. The alarm output is de-asserted when the alarm_clr_i input is high for one sys_clk_i period. The tf_error_o signal is used to display the type of error that has occurred. This data is reset to 0 when the next transaction begins (start_i is '1'). The following table describes various errors and their corresponding bit position in the tf_error_o register.

Table 1-2. tf_error_o Register Description

Bit	Function
5	TX delimiter error – as indicated in bit 7 of the status field
4	TX parity error – as indicated in bit 6 of the status field
3	CRC mismatch between CRC field received from slave and calculated CRC data
2	Incomplete message – delimiter error resulting in timeout
1	Bad start sequence in received control field – "0010" not received before the timeout
0	Parity Error in received control field

T-Format Interface Parameters and Interface Signals

This section discusses the parameters in the T-Format Interface GUI configurator and I/O signals.

Configuration Settings

- The following table lists the description of the configuration parameters used in the hardware implementation of
- T-Format Interface. These are generic parameters and are varied as per the requirement of the application.

Signal Name	Description
g_TIMEOUT_TIME	Defines the timeout time between successive fields in a frame in multiples of sys_clk_i period.
g_FAULT_THRESHOLD	Defines the fault threshold value – alarm_o is asserted when the fault counter exceeds this value.

Inputs and Outputs Signals
The following table lists the input and output ports of the T-Format Interface.

Table 2-2. Inputs and Outputs of T-Format Interface

Signal Name	Direction	Description
reset_i	Input	Active low asynchronous reset signal to design
sys_clk_i	Input	System Clock
ref_clk_i	Input	Reference clock, 2.5MHz*
start_i	Input	Startsignal to start T-Format transaction – must be ‘1’ for one sys_clk_i cycle
alarm_clr_i	Input	Clear alarm signal – must be ‘1’ for one sys_clk_i cycle
rx_i	Input	Serial data input from the encoder
crc_done_i	Input	Done signal from external CRC block –must be ‘1’ for one sys_clk_i cycle
cmd_i	Input	ControlField ID to be sent to the encoder
crc_calc_i	Input	Output of CRC Generator block with bits reversed, that is, crc_gen(7) -> crc_calc_i (0) , crc_gen(6)-> crc_calc_i(1), .. crc_gen(0)-> crc_calc_i(7)
tx_o	Output	Serial data output to encoder
tx_en_o	Output	Transmit enable signal – goes high when transmission is in progress
done_o	Output	Transaction done signal – asserted as a pulse with a width of one sys_clk_i cycle
alarm_o	Output	Alarm signal – asserted when the number of fault occurrences equals the threshold va lue configured in g_FAULT_THRESHOLD
start_crc_o	Output	Start signal for CRC generation block

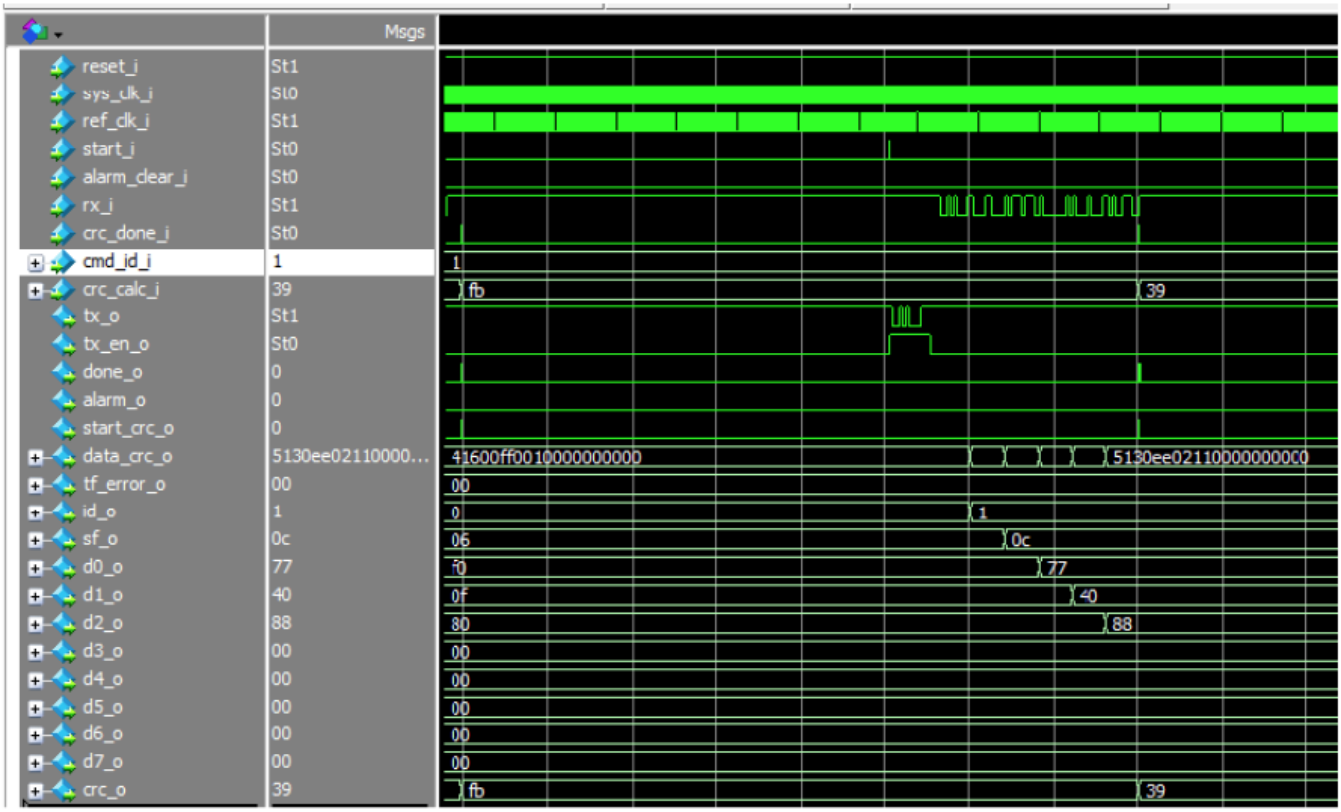
Signal Name	Direction	Description
data_crc_o	Output	Data for CRC generation block – data is provided as: {CF, SF, D0, D1, D2, .. D7} without delimiters. In case of shorter messages (where only D0-D2 have data), the other fields D3-D7 are taken as 0
tf_error_o	Output	TF Error register
id_o	Output	ID value from control field in received frame*
sf_o	Output	Status field from received frame*
d0_o	Output	D0field from received frame*
d1_o	Output	D1field from received frame*
d2_o	Output	D2field from received frame*
d3_o	Output	D3field from received frame*
d4_o	Output	D4field from received frame*
d5_o	Output	D5field from received frame*
d6_o	Output	D6field from received frame*
d7_o	Output	D7field from received frame*
crc_o	Output	CRC field from received frame*

Note: For more information, see the Tamagawa datasheet.

Timing Diagrams

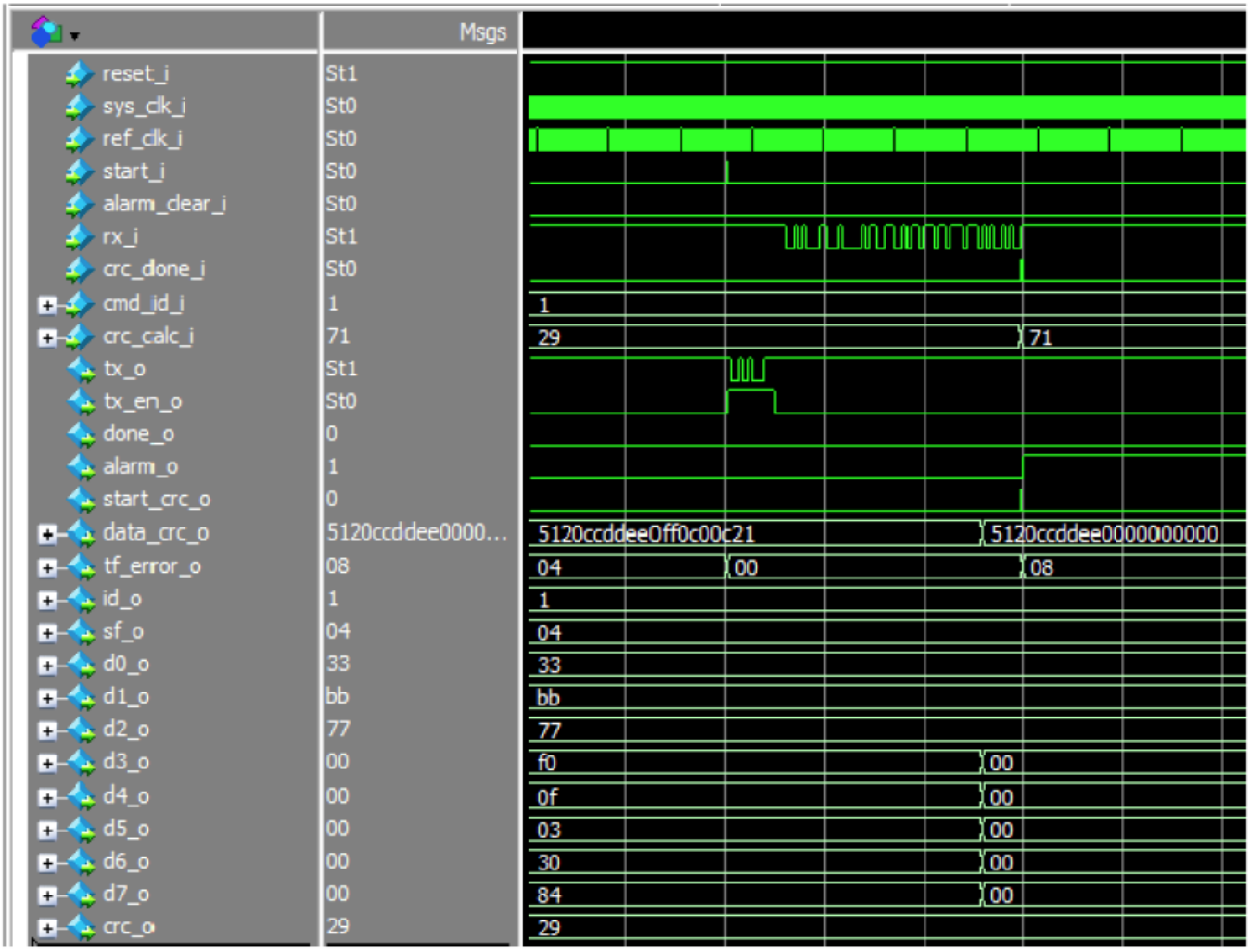
- This section discusses T-Format Interface timing diagrams.
- The following figure shows a normal T-format transaction. The done_o signal is generated at the end of every error-free transaction, and the tf_error_o signal remains at 0.

Figure 3-1. Timing Diagram – Normal Transaction



The following figure shows a T-Format transaction with a CRC error. The done_o signal is not generated, and the tf_error_o signal is 8, indicating that a CRC mismatch has occurred. The done_o signal is generated if the next transaction does not have any error.

Figure 3-2. Timing Diagram – CRC Error

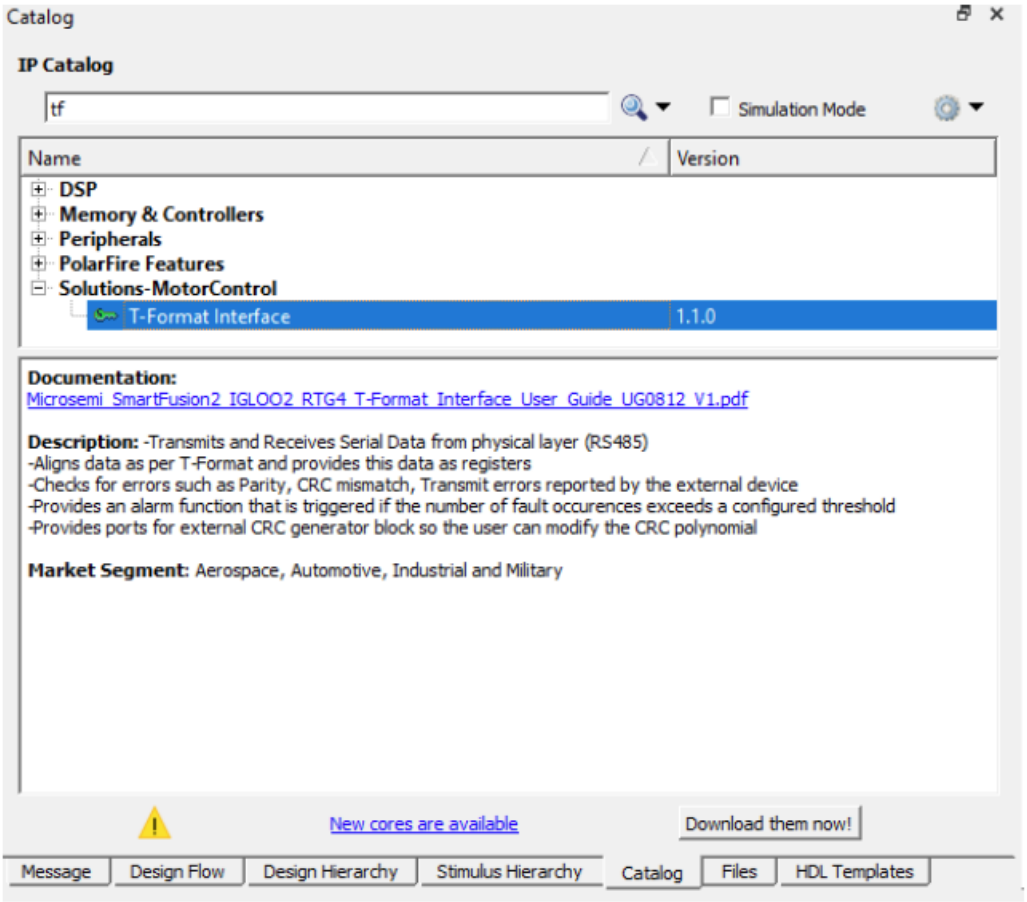


Testbench

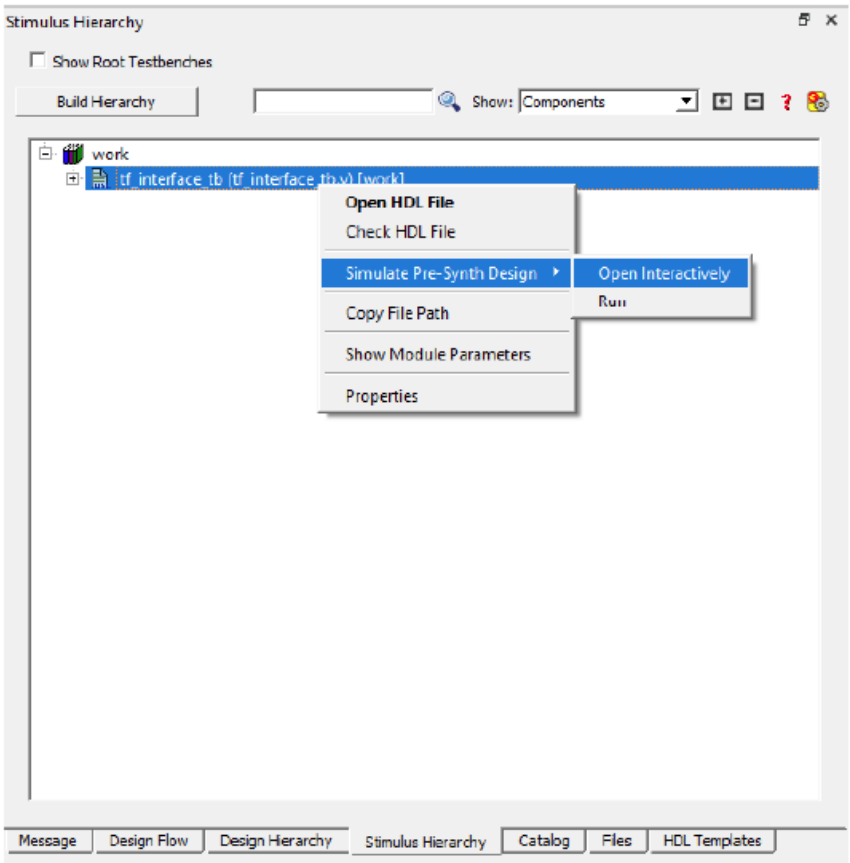
- A unified test-bench is used to verify and test the T-Format Interface called as user test-bench. Testbench is provided to check the functionality of the T-Format Interface IP.

Simulation
The following steps describe how to simulate the core using the testbench:

1. Open the Libero SoC application, click the Libero SoC Catalog tab, expand Solutions-MotorControl
2. Double-click T-Format Interface, and then click OK. The documentation associated with the IP is listed under Documentation.
    - **Important:** If you do not see the Catalog tab, navigate to the View Windows menu and click Catalog to make it visible.
    - **Figure 4-1.** T-Format Interface IP Core in Libero SoC Catalog

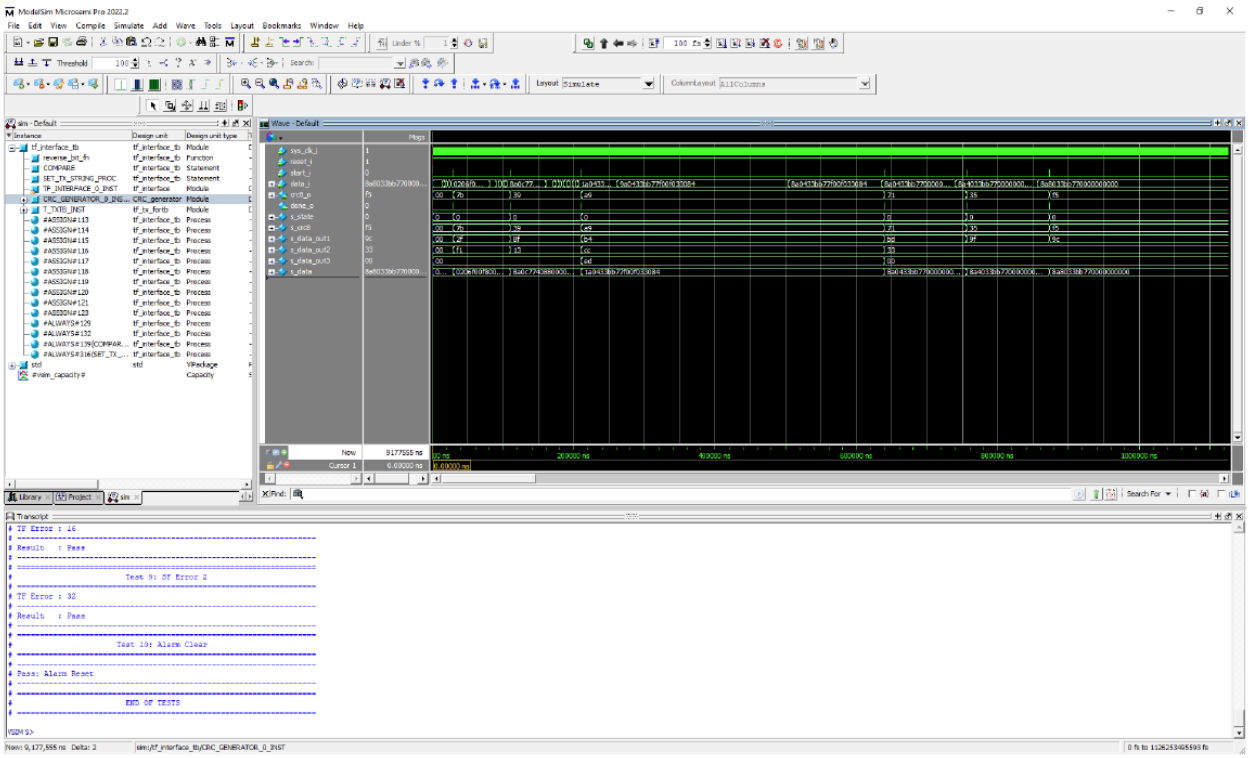


3. On the Stimulus Hierarchy tab, right-click testbench (t_format_interface_tb.v), point to Simulate Pre-Synth Design, and then click Open Interactively.
    - **Important:** If you do not see the Stimulus Hierarchy tab, navigate to View > Windows menu and click Stimulus Hierarchy to make it visible.
    - **Figure 4-2.** Simulating Pre-Synthesis Design



    - ModelSim opens with the testbench file as shown in the following figure.

- **Figure 4-3.** ModelSim Simulation Window



- **Important:** If the simulation is interrupted due to the runtime limit specified in the do file, use the run -all command to complete the simulation.

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	02/2023	The following is the list of changes in revision A of the document: • Migrated the document to the Microchip template. • Updated the document number to DS50003503A from 50200812. • Added 3. Timing Diagrams. • Added 4. Testbench.
1.0	02/2018	Revision 1.0 was the first publication of this document.

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Documents / Resources

	MICROCHIP Interface v1.1 T Format Interface [pdf] User Guide Interface v1.1 T Format Interface, Interface v1.1, T Format Interface, Format Interface, Interface

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