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IGLOO ® 2 Evaluation Kit Quickstart Card

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Introduction

Microchip's IGLOO2 FPGA Evaluation Kit makes it easier to develop embedded applications that involve motor control, system management, industrial automation, and high-speed serial I/O applications such as PCIe, SGMII, and user-customizable serial interfaces. The kit offers best-in-class feature integration coupled with the lowest power, proven security, and exceptional reliability. The board is also small form-factor PCIe-compliant, which allows quick prototyping and evaluation using any desktop PC or laptop with a PCIe slot.
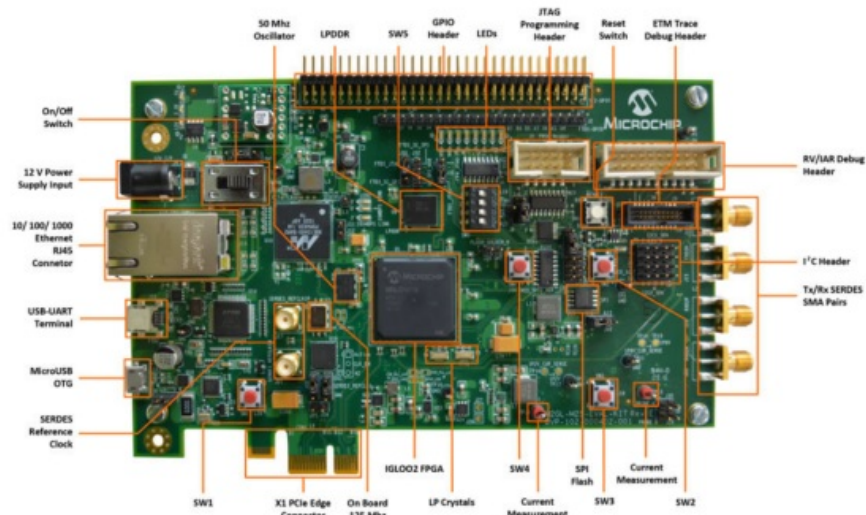
The kit has the following functionalities:

- Develop and test PCI Express Gen2 x1 lane designs
- Test signal quality of the FPGA transceiver using the full-duplex SerDes SMA pairs
- Measure the low power consumption of the IGLOO2 FPGA

- Create quickly a working PCIe link with the included PCIe Control Plane Demo

Table 1. Kit Contents—M2GL-EVAL-KIT

Quantity	Description
1	IGLOO ® 2 FPGA 12K LE M2GL010T-1FGG484 Evaluation Board
1	12V, 2A AC power adapter
1	FlashPro4 JTAG programmer
1	USB ® 2.0 A-Male to Mini-B cable
1	Quickstart card

Figure 1. Kit Diagram

Hardware Features

The IGLOO2 FPGA evaluation kit has the following hardware features:

- 12K LE IGLOO2 FPGA in the FGG484 Package (M2GL010T-1FGG484)
- 64 Mb SPI Flash Memory
- 512 Mb LPDDR
- PCI Express Gen2 x1 Interface
- Four SMA Connectors for Testing the Full-Duplex SerDes Channel
- RJ45 Interface for 10/100/1000 Ethernet

- JTAG/SPI Programming Interface

- Headers for I2C, SPI, and GPIOs

- Push-button Switches and LEDs for Demo Purposes

- Current Measurement Test Points

Jumper Settings

The IGLOO2 FPGA evaluation kit comes with the following default jumper settings.

Table 2. Jumper Settings

Jumper	Development Kit Function	Pins	Factroy Default
J23	Selects switch-side MUX inputs of A or B to the line side	1-2 (input A to the line side) that is on board 125 MHz differential clock oscillator output is routed to line side 2-3 (input B to the line side) that is external clock required to source through SMA connectors to the line side	Closed Open
J22	Selects the output enable control for the line side outputs	1-2 (line-side output enabled) 2-3 (line-side output disabled) Open	Closed Open
J24	Provides the VBUS supply to USB when using in Host mode	—	Open

J8	Selects between RVI header or FP4 header for application debug	1-2 FP4 for SoftConsole/ FlashPro 2-3 RVI for Keil ULINK/IAR J-Link 2-4 for toggling JTAG_SEL signal remotely using the GPIO capability of the FT4232 chip	Closed Open Open
J3	Selects either the SW2 input or the ENABLE_ FT4232 signal from the FT4232H chip	1-2 for manual power switching using the SW7 switch 2-3 for remote power switch using the GPIO capability of the FT4232 chip	Closed Open
J31	Selects between FTDI JTAG programming and FTDI slave programming	1-2 for FlashPro FTDI JTAG programming 2-3 for SPI slave programming	Closed Open
J32	Selects between FTDI SPI and SC_SCI header	1-2 for programming through FTDI SPI 2-3 for programming through SC_SPI header	Closed Open
J35	Selects between FP4 header and FTDI JTAG	1-2 for programming through FP4 header 2-3 for programming through FTDI JTAG	Closed Open

Running the Demo

The IGLOO2 FPGA evaluation kit is shipped with the PCI Express Control Plane demo preloaded. Instructions on running the demo design are available in the IGLOO2 FPGA Evaluation Kit PCIe Control Plane Demo user guide. For more information, see. Documentation Resources.

Programming

The IGLOO2 FPGA evaluation kit comes with a FlashPro4 programmer. Embedded

programming with the IGLOO2 FPGA evaluation kit is also available, and it is supported by the Libero SoC v11.4 SP1 or later.

Software and Licensing

The Libero SoC Design Suite is required for designing with the PolarFire video kit. Libero SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microchip's low power Flash FPGAs and SoC. The suite integrates industry standard Synopsys Synplify Pro synthesis and Siemens EDA ModelSim simulation with best-in-class constraints management and debug capabilities.

Download the latest Libero SoC release from Libero SoC v12.0 or later website.

Generate a Libero Silver license for your kit at www.microchipdirect.com/fpga-software-products.

Documentation Resources

For more information about the IGLOO2 FPGA evaluation kit, including user's guides, tutorials, and design examples, see the documentation at www.microchip.com/en-us/development-tool/M2GL-EVAL-KIT#Documentation.

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 [MICROCHIP IGLOO2 Evaluation Kit](#) [[pdf](#)] User Guide
IGLOO2 Evaluation Kit, IGLOO2, Evaluation Kit, Kit

References

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- User Manual

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