MICROCHIP DS50003319C-13 Ethernet HDMI TX IP User Guide

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DS50003319C-13 Ethernet HDMI TX IP

HDMI TX IP User Guide

Introduction (Ask a Question)

Microchip's High-Definition Multimedia Interface (HDMI) transmitter IP supports transmitting video and audio packet data described in the HDMI standard specification.

HDMI employs Transition Minimized Differential Signaling (TMDS) to efficiently transmit substantial volumes of digital data across the extended cable distances, ensuring high-speed, serial, and reliable digital signal transmission. A TMDS link consists of a single clock channel and three data channels. The video pixel clock is transmitted on the TMDS clock channel, which helps to keep the signals in synchronization. Video data is carried as 24-bit pixels on the three TMDS data channels, where each data channel is designated for red, green, and blue color component. Audio data is carried as 8-bit packets on the TMDS green and red channel.

TMDS encoder allows transmitting serial data at a high speed, while minimizing potential for Electro-magnetic Interference (EMI) over copper cables by minimizing the number of transitions (reducing interference between channels), and achieves Direct Current (DC) balance, on the wires, by keeping the number of ones and zeros on the line nearly equal.

HDMI TX IP is designed to be used along with PolarFire® SoC and PolarFire device transceivers. The IP is compatible with HDMI 1.4 and HDMI 2.0, which supports up to 60 frames per second, with a maximum bandwidth of 18 Gbps. The IP uses TMDS encoder that converts the 8-bit video data per channel and audio packet into the 10-bit DC-balanced, and transition minimized sequence. It is then transmitted serially at a rate of 10-bits per pixel, per channel. During the video blanking period, control tokens are transmitted. These tokens are generated based on the hsync and vsync signals. During data island period, audio packet is transmitted as 10-bit packets on red and green channel.

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Summary

The following table provides a summary of the HDMI TX IP characteristics.

Table 1. HDMI TX IP Characteristics

Core Version	This user guide supports HDMI TX IP v5.2.0
Supported Device Families	• PolarFire® SoC • PolarFire
Supported Tool Flow	Requires Libero® SoC v11.4 or later releases
Supported Interfaces	Interfaces supported by the HDMI TX IP are: • AXI4-Stream – This core supports AXI4-Stream to the input ports. When configured in this mode, IP takes AXI4 Stream standard complaint signals as inputs. • AXI4-Lite Configuration Interface – This Core supports AXI4-Lite configuration interface for 4Kp60 requirement. In this mode, IP inputs are supplied from SoftConsole. • Native – When configured in this mode, IP takes native video and audio signals as inputs.
Licensing	HDMI TX IP is provided with the following two license options: • Encrypted: Complete encrypted RTL code is provided for the core. It is available for free with any of the Libero license, enabling the core to be instantiated with SmartDesign. You can perform Simulation, Synthesis, Layout, and program the FPGA silicon using the Libero design suite. • RTL: Complete RTL source code is license locked, which needs to be purchased separately.

Features

HDMI TX IP has the following features:

• Compatible for HDMI 2.0 and 1.4b

• Supports one or four symbol/pixel per clock input

• Supports Resolutions up to 3840 x 2160 at 60 fps

• Supports 8, 10, 12, and 16-bit color depth

• Supports color formats such as RGB, YUV 4:2:2, and YUV 4:4:4

• Supports audio up to 32 channels

• Supports Encoding Scheme – TMDS

• Supports Native and AXI4 Stream Video and Audio Data interface

• Supports Native and AXI4-Lite Configuration interface for parameter modification

Installation Instructions

The IP core must be installed to the IP Catalog of Libero® SoC software automatically through the IP Catalog update function in Libero SoC software, or it is manually downloaded from the catalog. Once the IP core is installed in Libero SoC software IP Catalog, it is configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

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Resource Utilization (Ask a Question)

HDMI TX IP is implemented in PolarFire® FPGA (MPF300T – 1FCG1152I Package).

The following table lists the resources utilized when g_PIXELS_PER_CLK = 1PXL.

Table 2. Resource Utilization for 1PXL

	g_COLOR_FORMAT g_BITS_PER_COMPONENT (Bits)	g_AUX_CHANNEL_ENABLE g_4K60_SUPPORT Fabric		4 LUT	Fabric DFF	Interface 4LUT	Interface DFF	uSRAM (64×12)
RGB	8	Enable	Disable	787	514	108	108	9
		Disable	Disable	819	502	108	108	9
	10	Disable	Disable	1070	849	156	156	13

	12	Disable	Disable	1084	837	156	156	13
	16	Disable	Disable	1058	846	156	156	13
YCbCr422	8	Disable	Disable	696	473	96	96	8
YCbCr444	8	Disable	Disable	819	513	108	108	9
	10	Disable	Disable	1068	849	156	156	13
	12	Disable	Disable	1017	837	156	156	13
	16	Disable	Disable	1050	845	156	156	13

The following table lists the resources utilized when g_PIXELS_PER_CLK = 4PXL.

Table 3. Resource Utilization for 4PXL

	g_COLOR_FORMAT g_BITS_PER_COMPONENT (Bits)	g_AUX_CHANNEL_ENABLE g_4K60_SUPPORT Fabric		4LUT	Fabric DFF	Interface 4LUT	Interface DFF	uSRAM (64×12)

RGB	8	Disable	Enable	4078	2032	144	144	12
		Enable	Disable	1475	2269	144	144	12
		Disable	Disable	1393	1092	144	144	12
	10	Disable	Disable	2151	1635	264	264	22
	12	Disable	Disable	1909	1593	264	264	22
	16	Disable	Disable	1645	1284	264	264	22
YCbCr422	8	Disable	Disable	1265	922	144	144	12
YCbCr4	8	Disable	Disable	1119	811	144	144	12
	10	Disable	Disable	2000	1627	264	264	22

44	12	Disable	Disable	1909	1585	264	264	22
	16	Disable	Disable	1604	1268	264	264	22

HDMI TX IP Configurator

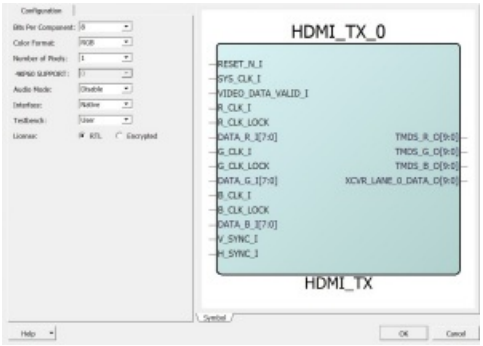
1. HDMI TX IP Configurator (Ask a Question)

This section provides an overview of the HDMI TX Configurator interface and its various components.

The HDMI TX Configurator provides a graphical interface to set up the HDMI TX core for specific video transmission requirements. This configurator allows the user to select parameters such as Bits Per Component, Color Format, Number of Pixels, Audio Mode, Interface, Testbench, and License. It is essential to adjust these settings correctly to ensure the effective transmission of video data over HDMI.

The interface of the HDMI TX Configurator consists of various dropdown menus and options that enable users to customize the HDMI transmission settings. The key configurations are described in Table 3-1.

The following figure provides a detailed view of the HDMI TX Configurator interface. Figure 1-1. HDMI TX IP Configurator



The interface also includes OK and Cancel buttons for confirming or discarding the configurations made.

Hardware Implementation

2. Hardware Implementation (Ask a Question)

HDMI Transmitter (TX) consists of two stages:

• An XOR/XNOR operation, which minimizes the number of transitions

• An INV/NONINV, which minimizes the disparity (DC balance). The extra two bits are added at this stage of operation. Control data (hsync and vsync) is encoded to 10 bits in four possible combinations to help the receiver synchronize its clock with the transmitter clock. A transceiver must be used along with the HDMI TX IP to serialize the 10 bits (1 pixel mode) or 40 bits (4 pixels mode).

The configurator also displays a representation of the HDMI Tx core, labeled HDMI_TX_0, indicating the various input and output connections that are interfaced with the core. There are three modes for the HDMI TX interface and are explained as follows:

RGB Color Format Mode

The ports of HDMI TX IP for one pixel per clock when the audio mode is enabled and Color format is RGB for PolarFire® devices is shown in the following figure. A visual representation of the HDMI Tx core's ports as follows:

• Control clock signals are R_CLK_LOCK, G_CLK_LOCK, and B_CLK_LOCK. Clock Signals are R_CLK_I, G_CLK_I, and B_CLK_I.

• Data channels including DATA_R_I, DATA_G_I, and DATA_B_I.

• Auxiliary Data signals are AUX_DATA_R_I and AUX_DATA_G_I.

Figure 2-1. HDMI TX IP Block Diagram (RGB Color Format)

For more information about I/O signals for RGB color format, see Table 3-2.

YCbCr444 Color Format Mode

The ports of HDMI TX IP for one pixel per clock when the audio mode is enabled and Color format is YCbCr444 is shown in the following figure. A visual representation of the HDMI Tx core's ports as follows:

• Control signals are Y_CLK_LOCK, Cb_CLK_LOCK, and Cr_CLK_LOCK.

• Clock signals are Y_CLK_I, Cb_CLK_I, and Cr_CLK_I.

• Data channels including DATA_Y_I, DATA_Cb_I, and DATA_Cr_I.

• Auxiliary Data input signals are AUX_DATA_Y_I and AUX_DATA_C_I.

Figure 2-2. HDMI TX IP Block Diagram (YCbCr444 Color Format)

For more information about I/O signals for YCbCr444 color format, see Table 3-6. YCbCr422 Color Format Mode

The ports of HDMI TX IP for one pixel per clock when the audio mode is enabled and Color format is YCbCr422 is shown in the following figure. A visual representation of the HDMI Tx core's ports as follows:

• Control signals are LANE1_CLK_LOCK, LANE2_CLK_LOCK, and LANE3_CLK_LOCK. • Clock signals are LANE1_CLK_I, LANE2_CLK_I, and LANE3_CLK_I.

• Data channels including DATA_Y_I and DATA_C_I.

Figure 2-3. HDMI TX IP Block Diagram (YCbCr422 Color Format)

For more information about I/O signals for YCbCr422 color format, see Table 3-7 User Guide

3. HDMI TX Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the HDMI TX GUI configurator and I/O signals. 3.1 Configuration Parameters (Ask a Question)

The following table lists the configuration parameters in the HDMI TX IP.

Table 3-1. Configuration Parameters

Parameter Name	Description
Color Format	Defines the color space. Supports the following color formats: • RGB • YCbCr422 • YCbCr444
Number of bits per component	Specifies the number of bits per color component. Supports 8, 10, 12, and 16 bits per component.
Number of Pixels	Indicates the number of pixels per clock input: • Pixel per clock = 1 • Pixel per clock = 4
4Kp60 Support	Support for 4K resolution at 60 frames per second: • When 1, 4Kp60 support is enabled • When 0, 4Kp60 support is disabled
Audio Mode	Configures the audio transmission mode. Audio data for R and G channel: • Enable • Disable
Interface	Native and AXI stream
Testbench	Allows the selection of a testbench environment. Supports the following testbench options: • User • None
License	Specifies the type of license. Provides the following two license options: • RTL • Encrypted

3.2 Ports (Ask a Question)

The following table lists the input and output ports of the HDMI TX IP for Native interface when Audio mode is enabled and Color format is RGB.

Table 3-2. Input and Output Signals

Signal Name	Direction	Width	Description
SYS_CLK_I	Input	1-bit	System clock, usually the same clock as the display controller
RESET_N_I	Input	1-bit	Asynchronous active-low reset signal
VIDEO_DATA_VALID_I	Input	1-bit	Video data valid input
AUDIO_DATA_VALID_I	Input	1-bit	Audio packet data valid input
R_CLK_I	Input	1-bit	TX clock for “R” channel from XCVR
R_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for R channel from XCVR
G_CLK_I	Input	1-bit	TX clock for “G” channel from XCVR
G_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for G channel from XCVR
B_CLK_I	Input	1-bit	TX clock for “B” channel from XCVR

HDMI TX Parameters and Interface Signals

……..continued Signal Name	Direction	Width	Description
B_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for B channel from XCVR
H_SYNC_I	Input	1-bit	Horizontal sync pulse
V_SYNC_I	Input	1-bit	Vertical sync pulse
PACKET_HEADER_I	Input	PIXELS_PER_CLK*1	Packet header for audio packet data
DATA_R_I	Input	PIXELS_PER_CLK*8	Input “R” data
DATA_G_I	Input	PIXELS_PER_CLK*8	Input “G” data
DATA_B_I	Input	PIXELS_PER_CLK*8	Input “B” data
AUX_DATA_R_I	Input	PIXELS_PER_CLK*4	Audio packet “R” channel data
AUX_DATA_G_I	Input	PIXELS_PER_CLK*4	Audio packet “G” channel data
TMDS_R_O	Output	PIXELS_PER_CLK*10	Encoded “R” data
TMDS_G_O	Output	PIXELS_PER_CLK*10	Encoded “G” data
TMDS_B_O	Output	PIXELS_PER_CLK*10	Encoded “B” data

The following table lists the ports for the AXI4 Stream interface with Audio Enable.

Table 3-3. Input and Output Ports for AXI4 Stream Interface

Port Name Type		Width	Description
TDATA_I	Input	3*g_BITS_PER_COMPONENT*g_PIXELS_PER_CLK Input video data	
TVALID_I	Input	1-bit	Input video valid
TREADY_O Output 1-bit			Output slave ready signal
TUSER_I	Input	PIXELS_PER_CLK*9 + 5	bit 0 = unused bit 1 = VSYNC bit 2 = HSYNC bit 3 = unused bit [3 + g_PIXELS_PER_CLK: 4] = Packet header bit [4 + g_PIXELS_PER_CLK] = Audio data valid bit [(5 * g_PIXELS_PER_CLK) + 4: (1*g_PIXELS_PER_CLK) + 5] = Audio G data bit [(9 * g_PIXELS_PER_CLK) + 4: (5*g_PIXELS_PER_CLK) + 5] = Audio R data

The following table lists the input and output ports of the HDMI TX IP for Native interface when Audio mode is disabled.

Table 3-4. Input and Output Signals

Signal Name	Direction	Width	Description
SYS_CLK_I	Input	1-bit	System clock, usually the same clock as the display controller
RESET_N_I	Input	1-bit	Asynchronous active -low reset signal
VIDEO_DATA_VALID_I	Input	1-bit	Video data valid input
R_CLK_I	Input	1-bit	TX clock for “R” channel from XCVR
R_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for R channel from XCVR
G_CLK_I	Input	1-bit	TX clock for “G” channel from XCVR
G_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for G channel from XCVR
B_CLK_I	Input	1-bit	TX clock for “B” channel from XCVR
B_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for B channel from XCVR
H_SYNC_I	Input	1-bit	Horizontal sync pulse
V_SYNC_I	Input	1-bit	Vertical sync pulse
DATA_R_I	Input	PIXELS_PER_CLK*8	Input “R” data

HDMI TX Parameters and Interface Signals

……..continued Signal Name Direction Width Description			
DATA_G_I	Input	PIXELS_PER_CLK*8	Input “G” data
DATA_B_I	Input	PIXELS_PER_CLK*8	Input “B” data
TMDS_R_O	Output	PIXELS_PER_CLK*10	Encoded “R” data
TMDS_G_O	Output	PIXELS_PER_CLK*10	Encoded “G” data
TMDS_B_O	Output	PIXELS_PER_CLK*10	Encoded “B” data

The following table lists the ports for the AXI4 Stream interface.

Table 3-5. Input and Output Ports for AXI4 Stream Interface

Port Name	Type	Width	Description
TDATA_I_VIDEO	Input	3*g_BITS_PER_COMPONENT*g_PIXELS_PER_CLK	Input video data
TVALID_I_VIDEO	Input	1-bit	Input video valid
TREADY_O_VIDEO	Output	1-bit	Output slave ready signal
TUSER_I_VIDEO	Input	4 bits	bit 0 = unused bit 1 = VSYNC bit 2 = HSYNC bit 3 = unused

The following table lists the ports for the YCbCr444 mode when audio mode is enabled.

Table 3-6. Input and Output for YCbCr444 Mode and Audio Mode Enabled

Signal Name	Direction Width		Description
SYS_CLK_I	Input	1-bit	System clock, usually the same clock as t he display controller
RESET_N_I	Input	1-bit	Asynchronous active-low reset signal
VIDEO_DATA_VAL ID_I Input		1-bit	Video data valid input
AUDIO_DATA_VAL ID_I Input		1-bit	Audio packet data valid input
Y_CLK_I	Input	1-bit	TX clock for “Y” channel from XCVR
Y_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for Y channel from XCV R
Cb_CLK_I	Input	1-bit	TX clock for “Cb” channel from XCVR
Cb_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for Cb channel from XC VR
Cr_CLK_I	Input	1-bit	TX clock for “Cr” channel from XCVR
Cr_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for Cr channel from XC VR
H_SYNC_I	Input	1-bit	Horizontal sync pulse
V_SYNC_I	Input	1-bit	Vertical sync pulse
PACKET_HEADE R_I	Input	PIXELS_PER_CLK*1	Packet header for audio packet data
DATA_Y_I	Input	PIXELS_PER_CLK*8	Input “Y” data

DATA_Cb_I	Input	PIXELS_PER_CLK*DATA_WIDTH Input “Cb” data	
DATA_Cr_I	Input	PIXELS_PER_CLK*DATA_WIDTH Input “Cr” data	
AUX_DATA_Y_I	Input	PIXELS_PER_CLK*4	Audio packet “Y” channel data
AUX_DATA_C_I	Input	PIXELS_PER_CLK*4	Audio packet “C” channel data
TMDS_R_O	Output	PIXELS_PER_CLK*10	Encoded “Cb” data
TMDS_G_O	Output	PIXELS_PER_CLK*10	Encoded “Y” data
TMDS_B_O	Output	PIXELS_PER_CLK*10	Encoded “Cr” data

The following table lists the ports for the YCbCr422 mode when audio mode is enabled.

HDMI TX Parameters and Interface Signals

Table 3-7. Input and Output for YCbCr422 Mode and Audio Mode Enabled

Signal Name	Direction Width		Description
SYS_CLK_I	Input	1-bit	System clock, usually the same clock as the display controller
RESET_N_I	Input	1-bit	Asynchronous Active -Low reset signal
VIDEO_DATA_VALID_I Input		1-bit	Video data valid input

LANE1_CLK_I	Input	1-bit	TX clock for “lane from XCVE lane 1” channel from XCVR
LANE1_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for lane from XCVE lane 1
LANE2_CLK_I	Input	1-bit	TX clock for “lane from XCVE lane 2” channel from XCVR
LANE2_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for lane from XCVE lane 2
LANE3_CLK_I	Input	1-bit	TX clock for “lane from XCVE lane 3” channel from XCVR
LANE3_CLK_LOCK	Input	1-bit	TX_CLK_STABLE for lane from XCVE lane 3
H_SYNC_I	Input	1-bit	Horizontal sync pulse
V_SYNC_I	Input	1-bit	Vertical sync pulse
PACKET_HEADER_I	Input	PIXELS_PER_CLK*1	Packet header for audio packet data
DATA_Y_I	Input	PIXELS_PER_CLK*DATA_WIDTH Input “Y” data	
DATA_C_I	Input	PIXELS_PER_CLK*DATA_WIDTH Input “C” data	
AUX_DATA_Y_I	Input	PIXELS_PER_CLK*4	Audio packet “Y” channel data
AUX_DATA_C_I	Input	PIXELS_PER_CLK*4	Audio packet “C” channel data
TMDS_R_O	Output	PIXELS_PER_CLK*10	Encoded “C” data
TMDS_G_O	Output	PIXELS_PER_CLK*10	Encoded “Y” data

TMDS_B_O	Output	PIXELS_PER_CLK*10	Encoded data related to sync information

Register Map and Descriptions

4. Register Map and Descriptions (Ask a Question)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	SCRAMBLER_IP_EN	7:0								START
		15:8								
		23:16								
		31:24								
0x04	XCVR_DATA_LANE_ 0_SEL	7:0							START[1:0]	
		15:8								
		23:16								
		31:24								

Register Map and Descriptions

4.1 SCRAMBLER_IP_EN (Ask a Question)

Name: SCRAMBLER_IP_EN

Offset: 0x000

Reset: 0x0

Property: Write-only

Scrambler Enable Control Register. This register must be written to obtain 4kp60 Support for the HDMI TX IP

Bit 31 30 29 28 27 26 25 24

Access

Reset

Bit 23 22 21 20 19 18 17 16

Access

Reset

Bit 15 14 13 12 11 10 9 8

Access

Reset

Bit 7 6 5 4 3 2 1 0

							START

Access W Reset 0

Bit 0 – START Writing “1” to this bit initiates Scrambler data transfer is enabled. HDMI 2.0 does employ a form of scrambling known as 8b/10b encoding. This encoding scheme is used to transmit data over the HDMI interface reliably and efficiently.

4.2 XCVR_DATA_LANE_0_SEL (Ask a Question)

Name: XCVR_DATA_LANE_0_SEL

Offset: 0x004

Reset: 0x1

Property: Write-only

XCVR_DATA_LANE_0_SEL register selects the data need to transfer to the XCVR from HDMI TX IP for obtaining the clock for Full HD, 4kp30, 4kp60.

Bit 31 30 29 28 27 26 25 24

Access

Reset

Bit 23 22 21 20 19 18 17 16

Access

Reset

Bit 15 14 13 12 11 10 9 8

Access

Reset

Bit 7 6 5 4 3 2 1 0

						START[1:0]

Access W W Reset 0 1

Bits 1:0 – START[1:0] Writing “10” to this bits initiates 4KP60 is enabled and the XCVR data-rate is given as FFFFF_00000.

5. Testbench Simulation (Ask a Question)

Testbench is provided to check the functionality of HDMI TX core. Testbench works only in native interface with 1 pixel per clock and audio mode enabled.

The following table lists the parameters that are configured according to the application.

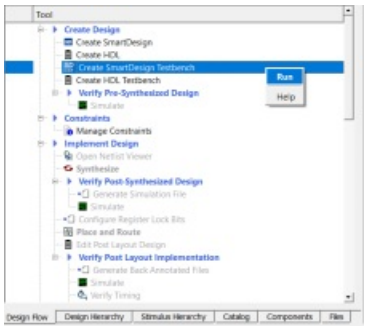
Table 5-1. Testbench Configuration Parameter

Name	Default Parameters
Color Format (g_COLOR_FORMAT)	RGB
Bits per component (g_BITS_PER_COMPONENT)	8
Number of Pixels (g_PIXELS_PER_CLK)	1
4Kp60 Support (g_4K60_SUPPORT)	0
Audio Mode (g_AUX_CHANNEL_ENABLE)	1 (Enable)
Interface (G_FORMAT)	0 (Disable)

To simulate the core using the testbench, perform the following steps:

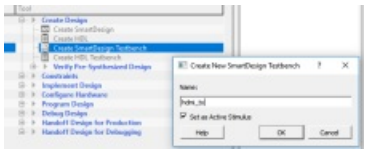
1. In the Design Flow window, expand Create Design.

2. Right-click Create SmartDesign Testbench, and then click Run, as shown in the following figure. Figure 5-1. Creating SmartDesign Testbench



3. Enter a name for the SmartDesign testbench, and then click OK.

Figure 5-2. Naming SmartDesign Testbench

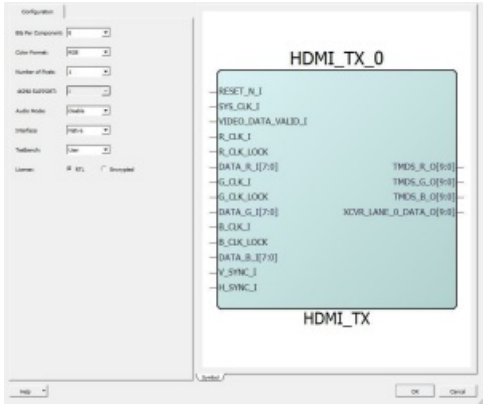


SmartDesign testbench is created, and a canvas appears to the right of the Design Flow pane.

4. Navigate to Libero® SoC Catalog, select View > Windows > IP Catalog, and then expand Solutions Video. Double-click HDMI TX IP (v5.2.0), and then click OK.

5. In the Parameter Configurator window, select the required Number of Pixels value, as shown in the following figure.

Figure 5-3. Parameter Configuration

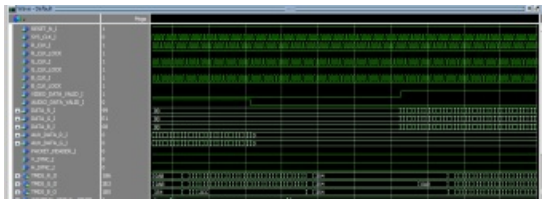


6. Select all the ports, right-click and select Promote to Top Level.

7. On the SmartDesign toolbar, click Generate Component.

8. On the Stimulus Hierarchy tab, right-click HDMI_TX_TB testbench file, and then click Simulate Pre-Synth Design > Open Interactively.

The ModelSim® tool opens with the testbench, as shown in the following figure. Figure 5-4. ModelSim Tool with HDMI TX Testbench File

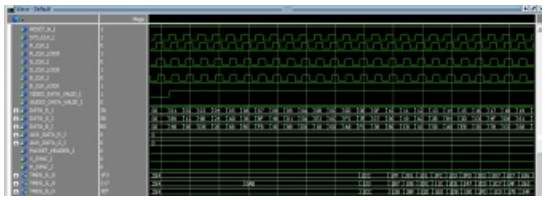


Important: If the simulation is interrupted due to the run time limit specified in the DO file, use the run -all command to complete the simulation.

5.1 Timing Diagrams (Ask a Question)

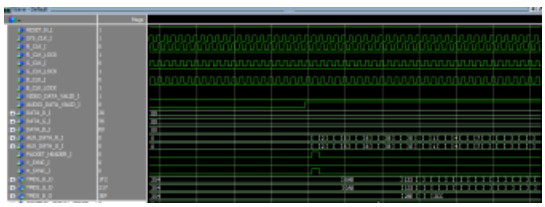
The following timing diagram for HDMI TX IP shows video data and control data periods for 1 pixel per clock.

Figure 5-5. HDMI TX IP Timing Diagram of Video Data for 1 Pixel Per Clock



The following diagram shows the four combinations of control data.

Figure 5-6. HDMI TX IP Timing Diagram of Control Data for 1 Pixel Per Clock



6. System Integration (Ask a Question)

This section shows a sample design description.

The following table lists the configurations of PF XCVR, PF TX PLL, and PF CCC.

Table 6-1. PF XCVR, PF TX PLL, and PF CCC Configurations

Resolution		Bit Width PF XCVR Configuration			PF TX PLL Configuration		PF CCC Configuration	
		TX Data Rate	TX Clock Division Factor	TX PCS Fabric Width	Desired Output Bit Clock	Reference Clock Frequency	Input Frequency	Output Frequency
1PXL (1080p60) 8		1485	4	10	5940	148.5	NA	NA
1PXL (1080p30) 10		925	4	10	3700	148.5	92.5	74
	12	1113.75	4	10	4455	148.5	111.375	74.25
	16	1485	4	10	5940	148.5	148.5	74.25
4PXL (1080p60) 10		1860	4	40	7440	148.5	46.5	37.2
	12	2229	4	40	8916	148.5	55.725	37.15
	16	2970	2	40	5940	148.5	74.25	37.125

4PXL (4kp30)	8	2970	2	40	5940	148.5	NA	NA
	10	3712.5	2	40	7425	148.5	92.812	74.25
	12	4455	1	40	4455	148.5	111.375	74.25
	16	5940	1	40	5940	148.5	148.5	74.25
4PXL (4Kp60)	8	5940	1	40	5940	148.5	NA	NA

HDMI TX Sample Design, when configured in g_BITS_PER_COMPONENT = 8-bit and

g_PIXELS_PER_CLK = 1 PXL mode, is shown in the following figure.

Figure 6-1. HDMI TX Sample Design

HDMI_TX_C0_0

PF_INIT_MONITOR_C0_0

FABRIC_POR_N

PCIE_INIT_DONE

USRAM_INIT_DONE

SRAM_INIT_DONE

DEVICE_INIT_DONE

XCVR_INIT_DONE

USRAM_INIT_FROM_SNVM_DONE

USRAM_INIT_FROM_UPROM_DONE

USRAM_INIT_FROM_SPI_DONE

SRAM_INIT_FROM_SNVM_DONE

SRAM_INIT_FROM_UPROM_DONE

SRAM_INIT_FROM_SPI_DONE

AUTOCALIB_DONE

PF_INIT_MONITOR_C0

CORERESET_PF_C0_0

CLK
EXT_RST_N
BANK_x_VDDI_STATUS
BANK_y_VDDI_STATUS
PLL_POWERDOWN_B
PLL_LOCK
FABRIC_RESET_N
SS_BUSY
INIT_DONE
FF_US_RESTORE
FPGA_POR_N

CORERESET_PF_C0

Display_Controller_C0_0

FRAME_END_O

H_SYNC_O

RESETN_I

V_SYNC_O

SYS_CLK_I

V_ACTIVE_O

ENABLE_I

DATA_TRIGGER_O

H_RES_O[15:0]

V_RES_O[15:0]

Display_Controller_C0

pattern_generator_verilog_pattern_0

DATA_VALID_O

SYS_CLK_I

FRAME_END_O

RESET_N_I

LINE_END_O

DATA_EN_I

RED_O[7:0]

FRAME_END_I

GREEN_O[7:0]

PATTERN_SEL_I[2:0]

BLUE_O[7:0]

BAYER_O[7:0]

Test_Pattern_Generator_C1

PF_XCVR_REF_CLK_C0_0

.

RESET_N_I

SYS_CLK_I

VIDEO_DATA_VALID_I

R_CLK_I

R_CLK_LOCK

G_CLK_I

G_CLK_LOCK

TMDS_R_O[9:0]

B_CLK_I

TMDS_G_O[9:0]

B_CLK_LOCK

TMDS_B_O[9:0]

V_SYNC_I

XCVR_LANE_0_DATA_O[9:0]

H_SYNC_I

.DATA_R_I[7:0]

DATA_R_I[7:0]

.DATA_G_I[7:0]

DATA_G_I[7:0]

.DATA_B_I[7:0]

DATA_B_I[7:0]

HDMI_TX_C0

PF_TX_PLL_C0_0

PF_XCVR_ERM_C0_0

PADs_OUT.

LANE3_TXD_N

CLKS_FROM_TXPLL_0

LANE3_TXD_P

LANE0_IN

LANE2_TXD_N

LANE0_PCS_ARST_N

LANE2_TXD_P

LANE0_PMA_ARST_N

LANE1_TXD_N

LANE0_TX_DATA[9:0]

LANE1_TXD_P

LANE1_IN

LANE0_TXD_N

LANE1_PCS_ARST_N

LANE0_TXD_P

LANE1_PMA_ARST_N

LANE0_OUT

LANE1_TX_DATA[9:0]

LANE0_TX_CLK_R

LANE2_IN

LANE0_TX_CLK_STABLE

LANE2_PCS_ARST_N

LANE1_OUT

LANE2_PMA_ARST_N

LANE1_TX_CLK_R

LANE2_TX_DATA[9:0]

LANE1_TX_CLK_STABLE

LANE3_IN

LANE2_OUT

LANE3_PCS_ARST_N

LANE2_TX_CLK_R

LANE3_PMA_ARST_N

LANE2_TX_CLK_STABLE

LANE3_TX_DATA[9:0] LANE3_OUTLANE3_TX_CLK_R

LANE3_TX_CLK_STABLE

PF_XCVR_ERM_C0

LANE3_TXD_N LANE3_TXD_P LANE2_TXD_N LANE2_TXD_P LANE1_TXD_N LANE1_TXD_P LANE0_TXD_N LANE0_TXD_P

PATTERN_SEL_I[2:0] REF_CLK_PAD_P REF_CLK_PAD_N

REF_CLK_PAD_P REF_CLK_PAD_NREF_CLK

REF_CLKPLL_LOCKCLKS_TO_XCVR

PF_XCVR_REF_CLK_C0

PF_TX_PLL_C0

For Example, in 8-bit configurations, the following components are the part of the design: • PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 1485 Mbps in PMA mode for TX only, with the data width configured as 10 bit for 1pxl mode and 148.5 MHz reference clock, based on the preceding table settings

• LANE0_TX_CLK_R output of PF_XCVR_ERM_C0_0 is generated as 148.5 MHz clock, based on the preceding table settings

• SYS_CLK_I (HDMI_TX_C0, Display_Controller_C0, pattern_generator_C0, CORERESET_PF_C0, and PF_INIT_MONITOR_C0) are driven by LANE0_TX_CLK_R, which is 148.5 MHz

• R_CLK_I, G_CLK_I, and B_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R, and LANE1_TX_CLK_R, respectively

System Integration

Sample integration for, g_BITS_PER_COMPONENT = 8 and g_PIXELS_PER_CLK = 4. For Example, in 8-bit configurations, the following components are the part of the design: • PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 2970 Mbps in PMA mode for

TX only, with the data width configured as 40-bit for 1pxl mode and 148.5 MHz reference clock based on the preceding table settings

• LANE0_TX_CLK_R output of PF_XCVR_ERM_C0_0 is generated as 74.25 MHz clock, based on the preceding table settings

• SYS_CLK_I (HDMI_TX_C0, Display_Controller_C0, pattern_generator_C0, CORERESET_PF_C0, and PF_INIT_MONITOR_C0) are driven by LANE0_TX_CLK_R, which is 148.5 MHz

• R_CLK_I, G_CLK_I, and B_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R, and LANE1_TX_CLK_R, respectively

HDMI TX Sample Design, when configured in g_BITS_PER_COMPONENT = 12 Bit and g_PIXELS_PER_CLK = 1 PXL mode, shown in the following figure.

Figure 6-2. HDMI TX Sample Design

PF_XCVR_ERM_C0_0

PATTERN_SEL_I[2:0]

REF_CLK_PAD_P REF_CLK_PAD_N

PF_CCC_C1_0

REF_CLK_0 OUT0_FABCLK_0PLL_LOCK_0

PF_CCC_C1

PF_INIT_MONITOR_C0_0

CORERESET_PF_C0_0

CLK

EXT_RST_N

BANK_x_VDDI_STATUS

BANK_y_VDDI_STATUS

PLL_POWERDOWN_B

PLL_LOCK

FABRIC_RESET_N

SS_BUSY

INIT_DONE

FF_US_RESTORE

FPGA_POR_N

CORERESET_PF_C0

Display_Controller_C0_0

FRAME_END_O
H_SYNC_O
RESETN_I
V_SYNC_O
SYS_CLK_I
V_ACTIVE_O
ENABLE_I
DATA_TRIGGER_O
H_RES_O[15:0]
V_RES_O[15:0]

Display_Controller_C0

pattern_generator_verilog_pattern_0

DATA_VALID_O

SYS_CLK_I

FRAME_END_O

RESET_N_I

LINE_END_O

DATA_EN_I

RED_O[7:0]

FRAME_END_I

GREEN_O[7:0]

PATTERN_SEL_I[2:0]

BLUE_O[7:0]

BAYER_O[7:0]

Test_Pattern_Generator_C0

PF_XCVR_REF_CLK_C0_0

REF_CLK_PAD_P

REF_CLK_PAD_NREF_CLK

PF_XCVR_REF_CLK_C0

HDMI_TX_0

RESET_N_I

SYS_CLK_I

VIDEO_DATA_VALID_I

R_CLK_I

R_CLK_LOCK

G_CLK_I

G_CLK_LOCK

TMDS_R_O[9:0]

B_CLK_I

TMDS_G_O[9:0]

B_CLK_LOCK

TMDS_B_O[9:0]

V_SYNC_I

XCVR_LANE_0_DATA_O[9:0]

H_SYNC_I

DATA_R_I[11:0]

DATA_R_I[11:4]

DATA_G_I[11:0]

DATA_G_I[11:4]

DATA_B_I[11:0]

DATA_B_I[11:4]

HDMI_TX_C0

PF_TX_PLL_C0_0

PADs_OUT

CLKS_FROM_TXPLL_0

LANE3_TXD_N

LANE0_IN

LANE3_TXD_P

LANE0_PCS_ARST_N

LANE2_TXD_N

LANE0_PMA_ARST_N

LANE2_TXD_P

LANE0_TX_DATA[9:0]

LANE1_TXD_N

LANE1_IN

LANE1_TXD_P

LANE1_PCS_ARST_N

LANE0_TXD_N

LANE1_PMA_ARST_N

LANE0_TXD_P

LANE1_TX_DATA[9:0]

LANE0_OUT

LANE2_IN

LANE1_OUT

LANE2_PCS_ARST_N

LANE1_TX_CLK_R

LANE2_PMA_ARST_N

LANE1_TX_CLK_STABLE

LANE2_TX_DATA[9:0] LANE2_OUTLANE3_IN

LANE2_TX_CLK_R

LANE3_PCS_ARST_N

LANE2_TX_CLK_STABLE

LANE3_PMA_ARST_N

LANE3_OUT

LANE3_TX_DATA[9:0]

LANE3_TX_CLK_R

LANE3_TX_CLK_STABLE

PF_XCVR_ERM_C0

LANE3_TXD_N LANE3_TXD_P LANE2_TXD_N LANE2_TXD_P LANE1_TXD_N LANE1_TXD_P LANE0_TXD_N LANE0_TXD_P

FABRIC_POR_N

PCIE_INIT_DONE

USRAM_INIT_DONE

SRAM_INIT_DONE

DEVICE_INIT_DONE

XCVR_INIT_DONE

USRAM_INIT_FROM_SNVM_DONE

USRAM_INIT_FROM_UPROM_DONE

USRAM_INIT_FROM_SPI_DONE

SRAM_INIT_FROM_SNVM_DONE

SRAM_INIT_FROM_UPROM_DONE

SRAM_INIT_FROM_SPI_DONE

AUTOCALIB_DONE

REF_CLKPLL_LOCKCLKS_TO_XCVR

PF_INIT_MONITOR_C0

PF_TX_PLL_C0

Sample integration for, g_BITS_PER_COMPONENT > 8 and g_PIXELS_PER_CLK = 1. For Example, in 12-bit configurations, the following components are the part of the design:

• PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 111.375 Mbps in PMA mode for TX only, with the data width configured as 10 bit for 1pxl mode and 1113.75 Mbps reference clock, based on the Table 6-1 settings

• LANE1_TX_CLK_R output of PF_XCVR_ERM_C0_0 is generated as 111.375 MHz clock, based on the Table 6-1 settings

• R_CLK_I, G_CLK_I, and B_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R, and LANE1_TX_CLK_R, respectively

• PF_CCC_C0 generates a clock named OUT0_FABCLK_0, with a frequency of 74.25 MHz, when input clock is 111.375 MHz, which is driven by LANE1_TX_CLK_R

• SYS_CLK_I (HDMI_TX_C0, Display_Controller_C0, pattern_generator_C0, CORERESET_PF_C0, and PF_INIT_MONITOR_C0) is driven by OUT0_FABCLK_0, which is 74.25 MHz

Sample integration for, g_BITS_PER_COMPONENT > 8 and g_PIXELS_PER_CLK = 4. For Example, in 12-bit configurations, the following components are the part of the design:

• PF_XCVR_ERM (PF_XCVR_ERM_C0_0) is configured for data rate of 4455 Mbps in PMA mode for TX only, with the data width configured as 40 bit for 4pxl mode and 111.375 MHz reference clock, based on the Table 6-1 settings

• LANE1_TX_CLK_R output of PF_XCVR_ERM_C0_0 is generated as 111.375 MHz clock, based on the Table 6-1 settings

• R_CLK_I, G_CLK_I, and B_CLK_I are driven by LANE3_TX_CLK_R, LANE2_TX_CLK_R, and LANE1_TX_CLK_R, respectively

• PF_CCC_C0 generates a clock named OUT0_FABCLK_0, with a frequency of 74.25 MHz, when input clock is 111.375 MHz, which is driven by LANE1_TX_CLK_R

• SYS_CLK_I (HDMI_TX_C0, Display_Controller_C0, pattern_generator_C0, CORERESET_PF_C0, and PF_INIT_MONITOR_C0) is driven by OUT0_FABCLK_0, which is 74.25 MHz

7. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 7-1. Revision History

Revision	Date	Description
C	05/2024	The following is the list of changes in revision C of the document: • Updated Introduction section • Removed resource utilization tables for one pixel and four pixels and added Table 2 and Table 3 in 1. Resource Utilization section • Updated Table 3-1 in the 3.1. Configuration Parameters section • Added Table 3-6 and Table 3-7 in the 3.2. Ports section • Added 6. System Integration section
B		09/2022 The following is the list of changes in revision B of the document: • Updated the content of Features and Introduction • Added Figure 2-2 for disabled Audio Mode • Added Table 3-4 and Table 3-5 • Updated the Table 3-2 and Table 3-3 • Updated Table 3-1 • Updated 1. Resource Utilization • Updated Figure 1-1 • Updated Figure 5-3
A		04/2022 The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template • The document number was updated to DS50003319 from 50200863
2.0	—	The following is a summary of the changes made in this revision. • Added Features and Supported Families sections
1.0		08/2021 Initial revision

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Documents / Resources

	MICROCHIP DS50003319C-13 Ethernet HDMI TX IP [pdf] User Guide DS50003319C - 13, DS50003319C - 2, DS50003319C - 3, DS50003319C-13 Ethernet HDMI TX IP, DS50003319C-13, Ethernet HDMI TX IP, HDMI TX IP, IP

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