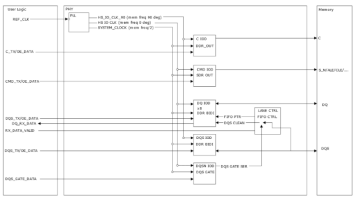

MICROCHIP DDR Read IP User Guide

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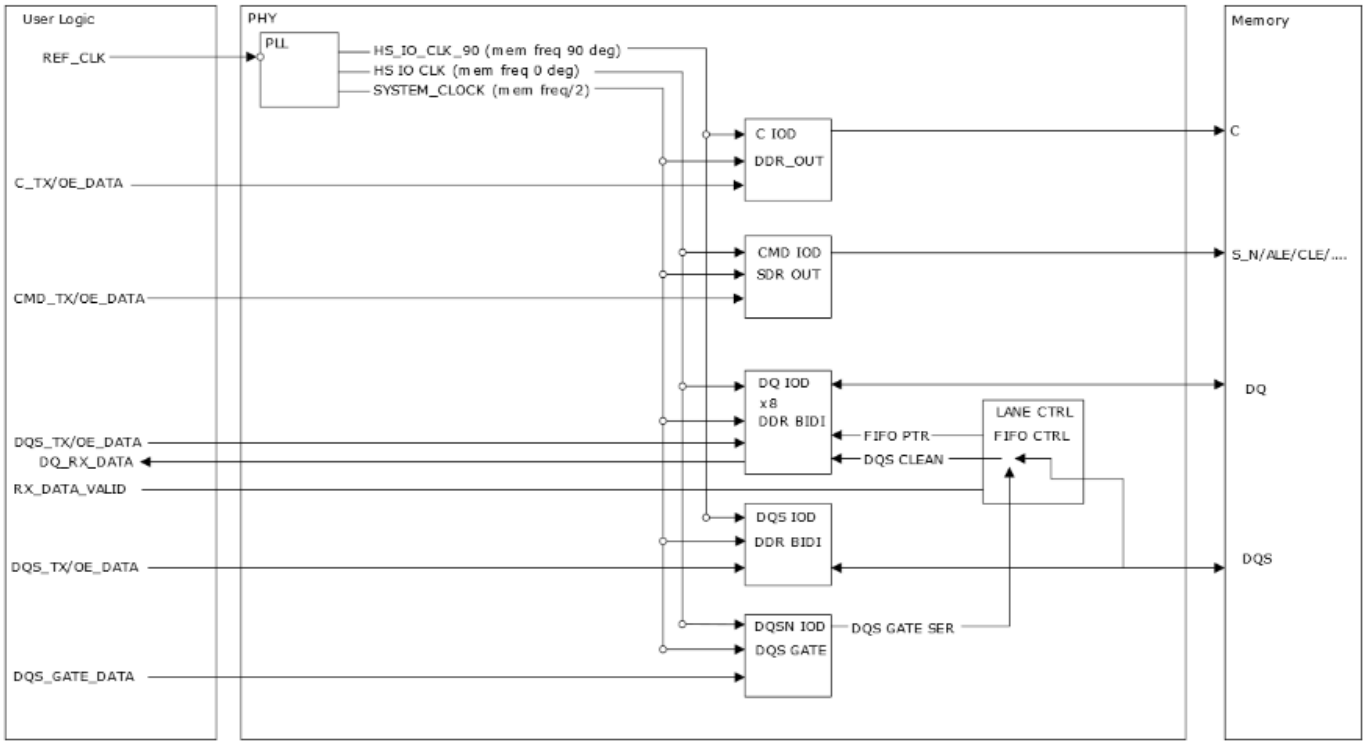
MICROCHIP DDR Read IP



Specifications

- Product Name: DDR Read IP v2.0
- Compatible with Video Arbiter IP
- Used for reading a burst of continuous data from DDR memory
- Typically used in video applications to read each horizontal line of the video frame stored in DDR memory

The DDR Read IP also has input and output ports in Arbiter

Interface bus and AXI4 Stream Interface, are listed in the user manual.

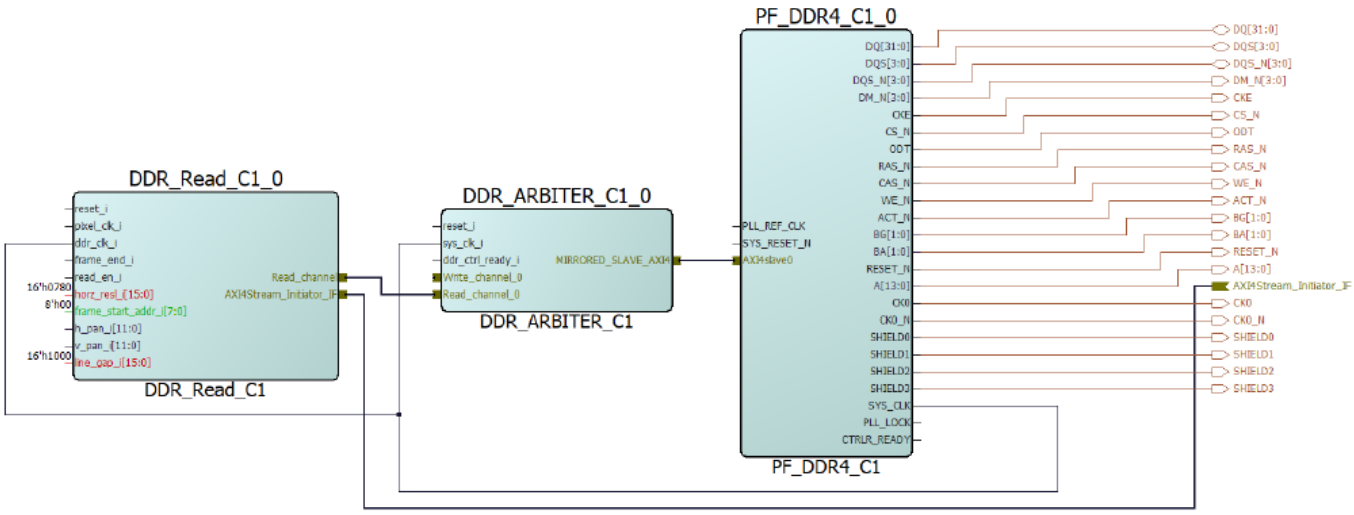
FAQ

1. What is the purpose of DDR Read IP?
2. What is the required compatibility for DDR Read IP?
3. In which applications are DDR Read IP typically used?

Introduction

DDR Read IP reads a burst of continuous data from the DDR memory. The DDR Read IP must be used with the Video Arbiter IP that converts the read requests to AXI4 transactions. The DDR Read IP is typically used in video applications to read each horizontal line of the video frame stored in DDR memory.

Figure 1. SmartDesign Arbiter Interface



Key Features

- Typically used to Read Video Frame Lines
- Supports Output Video Pixel Width of 8, 16, and 32 bits
- Supports Video Arbiter Interface of 128, 256, and 512 bits
- Supports AXI4 Stream Interface

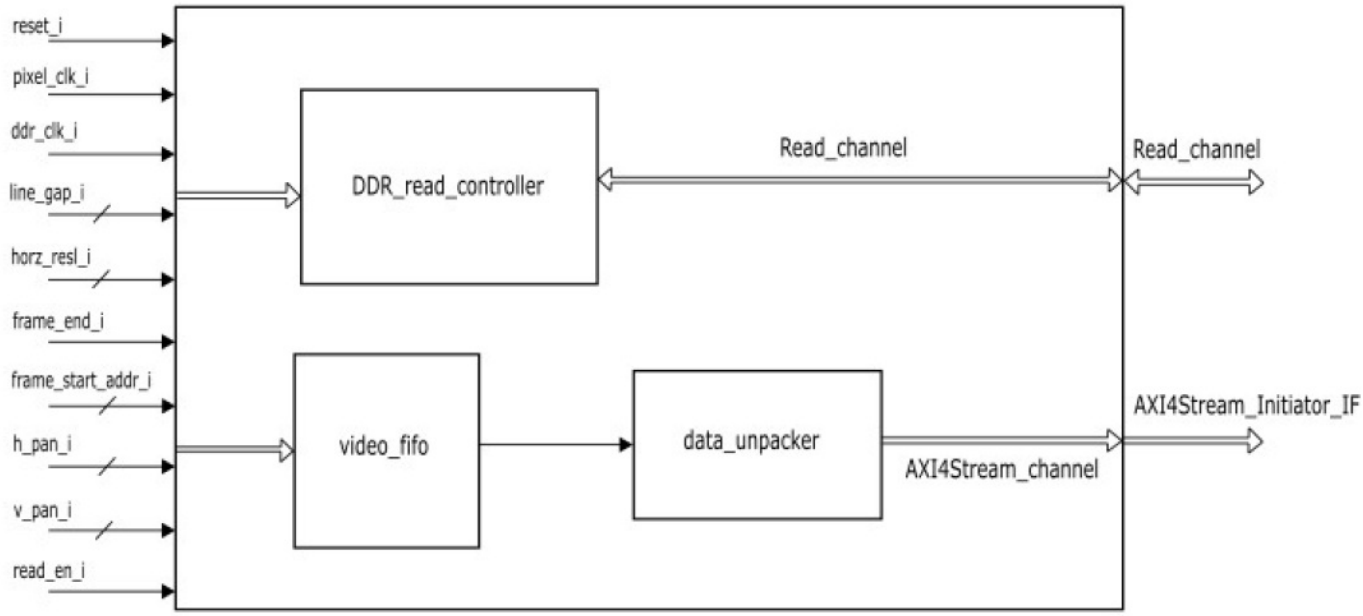
Hardware Implementation

The IP generates the control signals to the Video arbiter IP based on the user inputs of the horizontal resolution frame start address. The rising edge of read_en_i initiates a read transaction. The data from the video umpire is stored in a CDC FIFO that converts the data from the DDR clock domain to the pixel clock domain. The data is read from FIFO at the falling edge of read_en_i and unpacked to generate pixel data. The read_en_i should be high for sufficient duration to complete the DDR read transaction and the recommended duration is for several clocks equal to horizontal resolution. The first line is read from the address defined by frame_start_addr_i, and after each read transaction, the address is incremented by line_gap_i. The read address is reset to the frame_start_addr_i at every frame_end_i signal. The output data is high for a horizontal resolution number of clocks.

Design Description

- The following figure shows the top-level pin-out diagram of DDR Read.

Figure 1-1. DDR Read Top-level Pin Out Diagram



Input and Output Ports

The following table lists the input and output ports of the DDR Read IP in the Native Interface.

Table 1-1. Input and Output Ports of the DDR Read in Native Interface.

Port Name	Type	Width	Description
reset_i	Input	—	Active Low asynchronous reset signal to design
pixel_clk_i	Input	—	Pixel clock
ddr_clk_i	Input	—	DDR clock from the memory controller
frame_end_i	Input	—	End of frame signal
read_en_i	Input	—	Read enable signal for reading
line_gap_i	Input	16 bits	Line gap between two lines
horz_resl_i	Input	16 bits	Horizontal resolution

Port Name	**Type**	**Width**	**Description**
h_pan_i	Input	12 bits	Horizontal offset for each video line for horizontal panning
v_pan_i	Input	12 bits	Vertical offset from frame start address for vertical panning
read_ackn_i	Input	—	Acknowledgment for read request from video arbiter
read_done_i	Input	—	Read completion input from the video arbiter
ddr_data_valid_i	Input	—	Read data valid from Arbiter
frame_start_addr	Input	8 bits	Video frame start address
wdata_i	Input	Input Data Width	Read data from Arbiter
read_req_o	Output	—	Read the request to the arbiter
read_start_addr_o	Output	32 bits	DDR address from where read has to be started
burst_size_o	Output	8 bits	Read burst size
data_valid_o	Output	—	Data Valid
data_o	Output	Output Data Width	Data for Video Pipelining

The following table lists the input and output ports of the DDR Read IP in the Arbiter Interface bus.
Table 1-2. Input and Output Ports of the DDR Read in Arbiter Interface Bus.

Port Name	Type	Width	Description
RDATA_I	Input	Input Data Width	Read data from Arbiter
RVALID_I	Input	—	Read data valid from Arbiter
ARREADY_I	Input	—	Arbiter acknowledgment from read request
BUSER_I	Input	—	Read completion
ARADDR_O	Output	32 bits	DDR address from where read has to be started
ARVALID_O	Output	—	Read the request to the arbiter
ARSIZE_O	Output	8 bits	Read burst size

The following table lists the input and output ports of the DDR Read IP in the AXI4 Stream Interface.
Table 1-3. Input and Output Ports of the DDR Read in AXI4 Stream Interface.

Port Name	Type	Width	Description
CLOCK_I	Input	—	Pixel clock
RESET_n_I	Input	—	Active Low asynchronous reset signal to design
TDATA_O	Output	Output Data Width	Output Video Data
TSTRB_O	Output	[Output Data Width/8 – 1 : 0]	Output Video Data strobe
TKEEP_O	Output	[Output Data Width/8 – 1 : 0]	Output Video Data Keep
TVALID_O	Output	—	Output Video data valid
TUSER_O	Output	4 bits	Output user data 0bit= VSYNC 3bit =Frame end

Port Name	Type	Width	Description
TLAST_O	Output	—	Output Video End of Frame

Configuration Parameters

The following table lists the configuration parameters used in the DDR Read IP hardware implementation. These are generic parameters and can be varied based on the application requirements.
Table 1-4. Configuration Parameters

Parameter Name	Description
Horizontal Resolution	Defines horizontal resolution
Input Data Width	Defines the input data width (128, 256, and 512 bits)
Output Data Width	Defines the output data width (8, 16, 24, 32, and 64 bits)
Arbiter Interface	Options to select the Arbiter Interface from the drop-down menu as Native or Bus Interface
Data Interface	Options to select the Data Interface from the drop-down menu as Native and AXI4 Stream Interface

Resource Utilization

The following table lists the resource utilization for DDR Read IP in the Native Interface with the input data width = 256 and output data width = 8.
DDR Read block is implemented on the PolarFire FPGA device, MPF300TS_ES-1FCG1152E package.
Table 1-5. DDR Read IP in Native Interface

Resource	Usage
DFFs	502
4 input LUTs	513
MACC	0
LSRAM 18K	14
SRAM	0

The following table lists the resource utilization for DDR Read IP in the Bus Interface and AXI4 stream with input data width = 256 and output data width = 8.
Table 1-6. DDR Read IP in Bus Interface and AXI4 Stream

Resource	Usage
DFFs	512
4 input LUTs	514
MACC	0
LSRAM 18K	14
SRAM	0

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
1.0	03/2022	Initial Revision.

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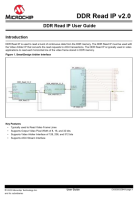	MICROCHIP DDR Read IP [pdf] User Guide DDR Read IP, DDR, Read IP, IP

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