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MICROCHIP DDR AXI4 Arbiter User Guide

Contents

MICROCHIP DDR AXI4 Arbiter

Introduction: The AXI4-Stream protocol standard uses the terminology Master and Slave. The equivalent Microchip terminology used in this document is Initiator and Target, respectively.
Summary: The following table provides a summary of the DDR AXI4 Arbiter characteristics.

Characteristic	Value
Core Version	DDR AXI4 Arbiter v2.2
Supported Device Families	–
Supported Tool Flow Licensing	–

Features: DDR AXI4 Arbiter has the following key features:

- IP core must be installed to the IP Catalog of the Libero SoC software.
- The core is configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero project list.

Device Utilization and Performance:

Device Details	Family	Device	Resources	Performance (MHz)
LUTs DFF RAMs LSRAM SRAM Math Blocks Chip Globals	PolarFire	MPF300T-1	5411 4202	266

Functional Description

Functional Description: This section describes the implementation details of the DDR_AXI4_Arbiter. The following figure shows the top-level pin-out diagram of the DDR AXI4 Arbiter.

DDR_AXI4_Arbiter Parameters and Interface Signals

Configuration Settings:
The configuration settings for DDR_AXI4_Arbiter are not specified in this document.

Inputs and Outputs Signals:
The input and output signals for DDR_AXI4_Arbiter are not specified in this document.

Timing Diagrams
The timing diagrams for DDR_AXI4_Arbiter are not specified in this document.

Testbench

Simulation:
The simulation details for DDR_AXI4_Arbiter are not specified in this document.
Revision History
The revision history for DDR_AXI4_Arbiter is not specified in this document.
Microchip FPGA Support
The Microchip FPGA Support information for DDR_AXI4_Arbiter is not specified in this document.

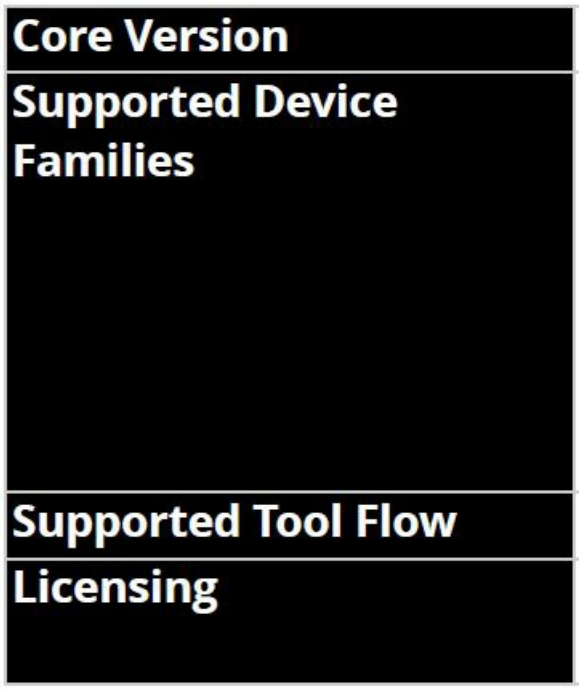
Product Usage Instructions

1. Install DDR AXI4 Arbiter v2.2 to the IP Catalog of the Libero SoC software.
2. Configure, generate and instantiate the core within the SmartDesign tool for inclusion in the Libero project list.

Introduction (Ask a Question)

Memories are an integral part of any typical video and graphics application. They are used for buffering entire video frames when the local memory of the FPGA is insufficient to hold the entire frame. When there are multiple reads and writes of video frames into DDR, an arbiter will be required to arbitrate between multiple requests. The DDR AXI4 Arbiter IP provides 8 write channels to write frame buffers into external DDR memory and 8 read channels to read frames from external memory. The arbitration is based on a first-come, first-served basis. If two requests occur simultaneously, the channel with the lower channel number will take priority. The arbiter connects to the DDR controller IP through the AXI4 interface. The DDR AXI4 Arbiter provides an AXI4 Initiator interface to the DDR on-chip controllers. The arbiter supports up to eight write channels and eight read channels. The block arbitrates between eight read channels to provide access to the AXI read channel in a first-come, first-served manner. The block arbitrates between eight write channels to provide access to the AXI write channel in a first-come, first-served manner. All eight read-and-write channels have equal priority. The AXI4 Initiator interface of the Arbiter IP can be configured for various data widths ranging from 64 bits to 512 bits.
Important: The AXI4-Stream protocol standard uses the terminology “Master” and “Slave”. The equivalent Microchip terminology used in this document is Initiator and Target, respectively.
Summary (Ask a Question)
The following table provides a summary of the DDR AXI4 Arbiter characteristics.

Table 1. DDR AXI4 Arbiter Characteristics



This document applies to DDR AXI4 Arbiter v2.2.

- PolarFire® SoC
- PolarFire
- RTG4™
- IGLOO® 2
- SmartFusion® 2

Requires Libero® SoC v12.3 or later releases. The IP can be used in RTL mode without any license. For more information, see DDR_AXI4_Arbiter.

Features (Ask a Question)

DDR AXI4 Arbiter has the following key features:

- Eight Write channels
- Eight Read channels
- AXI4 Interface to DDR controller
- Configurable AXI4 width: 64, 128, 256, and 512 bits
- Configurable Address width: 32 to 64 bits

Implementation of IP Core in Libero® Design Suite (Ask a Question)
IP core must be installed to the IP Catalog of the Libero SoC software. This is installed automatically through the IP Catalog update function in the Libero SoC software, or the IP core is manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, the core is configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero project list.
Device Utilization and Performance (Ask a Question)
The following table lists the device utilization used for DDR_AXI4_Arbiter.
Table 2. DDR_AXI4_Arbiter Utilization

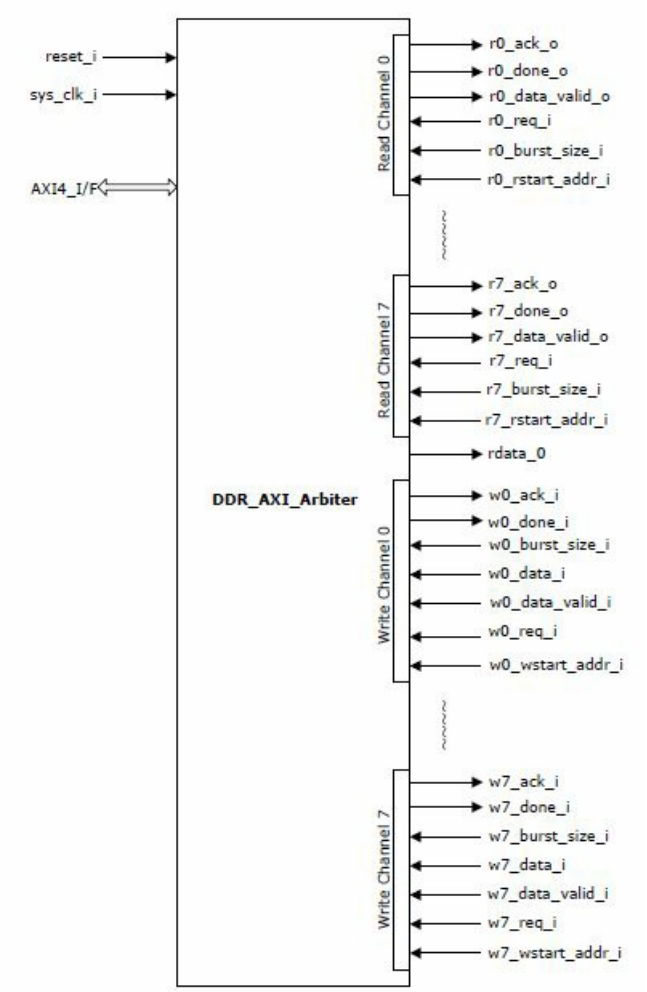
Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T-1	5411	4202	266	13	1	0	0
PolarFire	MPF300T-1	5411	4202	266	13	1	0	0
SmartFusion® 2	M2S150-1	5546	4309	192	15	1	0	0

Important:

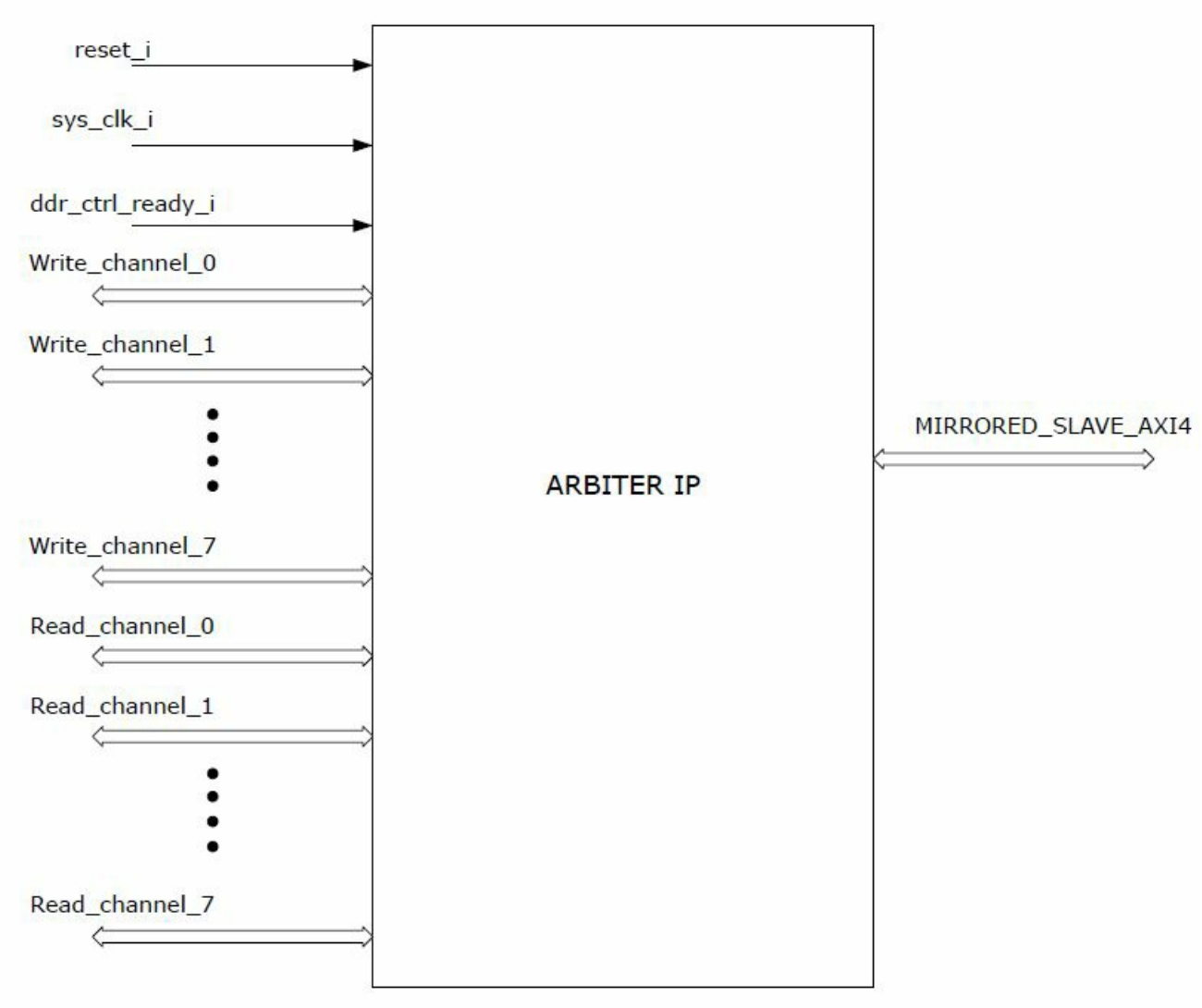
- The data in the preceding table is captured using typical synthesis and layout settings. The IP is configured for eight write channels, eight read channels, address width of 32 bit, and data width of 512 bits configuration.
- Clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers.

Functional Description (Ask a Question)

This section describes the implementation details of the DDR_AXI4_Arbiter. The following figure shows the top-level pin-out diagram of the DDR AXI4 Arbiter. Figure 1-1. Top-Level Pin-Out Block Diagram for Native Arbiter Interface



The following figure shows the system-level block diagram of the DDR_AXI4_Arbiter in Bus interface mode. Figure 1-2. System-Level Block Diagram of DDR_AXI4_Arbiter



A read transaction is triggered by setting the input signal r(x)_req_i high on a particular read channel. The arbiter responds by acknowledgment when it is ready to service the read request. Then it samples the starting AXI address and reads the burst size which is input from the external initiator. The channel processes the inputs and generates the required AXI transactions to read data from the DDR memory. The read data output from the arbiter is common to all the read channels. During data read out, the read data valid of the corresponding channel goes high. The end of the read transaction is denoted by a read-done signal when all the requested bytes are sent out. Similar to a read transaction, a write transaction is triggered by setting the input signal w(x)_req_i high. Along with the request signal, the write start address and the burst length must be provided during the request. When the arbiter is available to service the written request, it responds by sending an acknowledgment signal on the corresponding channel. Then the user has to provide the write data along with the data-valid signal on the channel. The number of clocks the data valid high period must match the burst length. The arbiter completes the write operation and sets the write done signal high denoting the completion of the write transaction.

DDR_AXI4_Arbiter Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the DDR_AXI4_Arbiter GUI configurator and I/O signals.

2.1 Configuration Settings (Ask a Question)

The following table lists the description of the configuration parameters used in the hardware implementation of DDR_AXI4_Arbiter. These are generic parameters and can be varied as per the requirement of the application.

Table 2-1. Configuration Parameter

Signal Name	Description
AXI ID Width	Defines the AXI ID width.
AXI Data Width	Defines the AXI data width.
AXI Address Width	Defines the AXI address width
Number of Read channels	Options to select the required no of write channels from the drop-down menu ranging from one channel to eight write channels.
Number of Write channels	Options to select the required no of read channels from the drop-down menu ranging from one channel to eight read channels.
AXI4_SELECTION	Options to select between AXI4_MASTER and AXI4_MIRRORED_SLAVE.
Arbiter Interface	Option to select the bus interface.

Inputs and Outputs Signals (Ask a Question)

The following table lists the inputs and output ports of the DDR AXI4 Arbiter for Bus interface.

Table 2-2. Input and Output Ports for Arbiter Bus Interface

Signal Name	Direction	Width	Description
reset_i	Input	—	Active Low asynchronous reset signal to design
sys_ckl_i	Input	—	System clock
ddr_ctrl_ready_i	Input	—	Receives the ready Input signal from the DDR controller
ARVALID_I_0	Input	—	Read request from read channel 0
ARSIZE_I_0	Input	8 bits	read burst size from read channel 0
ARADDR_I_0	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 0
ARREADY_O_0	Output	—	Arbiter acknowledgment to read request from read channel 0
RVALID_O_0	Output	—	Read data valid from read channel 0
RDATA_O_0	Output	[AXI_DATA_WIDTH-1 : 0]	Read data from read channel 0
RLAST_O_0	Output	—	Read end of frame signal from read channel 0
BUSER_O_r0	Output	—	Read completion to read channel 0
ARVALID_I_1	Input	—	Read request from read channel 1
ARSIZE_I_1	Input	8 bits	Read burst size from read channel 1
ARADDR_I_1	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 1
ARREADY_O_1	Output	—	Arbiter acknowledgment to read request from read channel 1
RVALID_O_1	Output	—	Read data valid from read channel 1
RDATA_O_1	Output	[AXI_DATA_WIDTH-1 : 0]	Read data from read channel 1
RLAST_O_1	Output	—	Read end of frame signal from read channel 1
BUSER_O_r1	Output	—	Read completion to read channel 1
ARVALID_I_2	Input	—	Read request from read channel 2

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Signal Name	Direction	Width	Description
ARSIZE_I_2	Input	8 bits	Read burst size from read channel 2
ARADDR_I_2	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 2
ARREADY_O_2	Output	—	Arbiter acknowledgment to read request from read channel 2

RVALID_O_2	Output	—	Read data valid from read channel 2
RDATA_O_2	Output	[AXI_DATA_WIDTH-1 : 0]	Read data from read channel 2
RLAST_O_2	Output	—	Read end of frame signal from read channel 2
BUSER_O_r2	Output	—	Read completion to read channel 2
ARVALID_I_3	Input	—	Read request from read channel 3
ARSIZE_I_3	Input	8 bits	Read burst size from read channel 3
ARADDR_I_3	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 3
ARREADY_O_3	Output	—	Arbiter acknowledgment to read request from read channel 3
RVALID_O_3	Output	—	Read data valid from read channel 3
RDATA_O_3	Output	[AXI_DATA_WIDTH-1 : 0]	Read data from read channel 3
RLAST_O_3	Output	—	Read end of frame signal from read channel 3
BUSER_O_r3	Output	—	Read completion to read channel 3
ARVALID_I_4	Input	—	Read request from read channel 4
ARSIZE_I_4	Input	8 bits	Read burst size from read channel 4
ARADDR_I_4	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 4
ARREADY_O_4	Output	—	Arbiter acknowledgment to read request from read channel 4
RVALID_O_4	Output	—	Read data valid from read channel 4
RDATA_O_4	Output	[AXI_DATA_WIDTH-1 : 0]	Read data from read channel 4
RLAST_O_4	Output	—	Read end of frame signal from read channel 4
BUSER_O_r4	Output	—	Read completion to read channel 4
ARVALID_I_5	Input	—	Read request from read channel 5
ARSIZE_I_5	Input	8 bits	Read burst size from read channel 5
ARADDR_I_5	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 5
ARREADY_O_5	Output	—	Arbiter acknowledgment to read request from read channel 5
RVALID_O_5	Output	—	Read data valid from read channel 5
RDATA_O_5	Output	[AXI_DATA_WIDTH-1 : 0]	Read data from read channel 5

RLAST_O_5	Output	—	Read end of frame signal from read channel 5
BUSER_O_r5	Output	—	Read completion to read channel 5
ARVALID_I_6	Input	—	Read request from read channel 6
ARSIZE_I_6	Input	8 bits	Read burst size from read channel 6
ARADDR_I_6	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 6
ARREADY_O_6	Output	—	Arbiter acknowledgment to read request from read channel 6
RVALID_O_6	Output	—	Read data valid from read channel 6
RDATA_O_6	Output	[AXI_DATA_WIDTH-1 : 0]	Read data from read channel 6
RLAST_O_6	Output	—	Read end of frame signal from read channel 6

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Signal Name	Direction	Width	Description
BUSER_O_r6	Output	—	Read completion to read channel 6
ARVALID_I_7	Input	—	Read request from read channel 7
ARSIZE_I_7	Input	8 bits	Read burst size from read channel 7
ARADDR_I_7	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 7
ARREADY_O_7	Output	—	Arbiter acknowledgment to read request from read channel 7
RVALID_O_7	Output	—	Read data valid from read channel 7
RDATA_O_7	Output	[AXI_DATA_WIDTH-1 : 0]	Read data from read channel 7
RLAST_O_7	Output	—	Read end of frame signal from read channel 7
BUSER_O_r7	Output	—	Read completion to read channel 7
AWSIZE_I_0	Input	8 bits	Write burst size for write channel 0
WDATA_I_0	Input	[AXI_DATA_WIDTH-1: 0]	Video data Input to write channel 0
WVALID_I_0	Input	—	Write data valid to write channel 0
AWVALID_I_0	Input	—	Write request from write channel 0
AWADDR_I_0	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 0

AWREADY_O_0	Output	—	Arbiter acknowledgment to write request from write channel 0
BUSER_O_0	Output	—	Write completion to write channel 0
AWSIZE_I_1	Input	8 bits	Write burst size for write channel 1
WDATA_I_1	Input	[AXI_DATA_WIDTH-1:0]	Video data Input to write channel 1
WVALID_I_1	Input	—	Write data valid to write channel 1
AWVALID_I_1	Input	—	Write request from write channel 1
AWADDR_I_1	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 1
AWREADY_O_1	Output	—	Arbiter acknowledgment to write request from write channel 1
BUSER_O_1	Output	—	Write completion to write channel 1
AWSIZE_I_2	Input	8 bits	Write burst size for write channel 2
WDATA_I_2	Input	[AXI_DATA_WIDTH-1:0]	Video data Input to write channel 2
WVALID_I_2	Input	—	Write data valid to write channel 2
AWVALID_I_2	Input	—	Write request from write channel 2
AWADDR_I_2	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 2
AWREADY_O_2	Output	—	Arbiter acknowledgment to write request from write channel 2
BUSER_O_2	Output	—	Write completion to write channel 2
AWSIZE_I_3	Input	8 bits	Write burst size for write channel 3
WDATA_I_3	Input	[AXI_DATA_WIDTH-1:0]	Video data Input to write channel 3
WVALID_I_3	Input	—	Write data valid to write channel 3
AWVALID_I_3	Input	—	Write request from write channel 3
AWADDR_I_3	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 3
AWREADY_O_3	Output	—	Arbiter acknowledgment to write request from write channel 3
BUSER_O_3	Output	—	Write completion to write channel 3
AWSIZE_I_4	Input	8 bits	Write burst size for write channel 4

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Signal Name	Direction	Width	Description

WDATA_I_4	Input	[AXI_DATA_WIDTH-1:0]	Video data Input to write channel 4
WVALID_I_4	Input	—	Write data valid to write channel 4
AWVALID_I_4	Input	—	Write request from write channel 4
AWADDR_I_4	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 4
AWREADY_O_4	Output	—	Arbiter acknowledgment to write request from write channel 4
BUSER_O_4	Output	—	Write completion to write channel 4
AWSIZE_I_5	Input	8 bits	Write burst size for write channel 5
WDATA_I_5	Input	[AXI_DATA_WIDTH-1:0]	Video data Input to write channel 5
WVALID_I_5	Input	—	Write data valid to write channel 5
AWVALID_I_5	Input	—	Write request from write channel 5
AWADDR_I_5	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 5
AWREADY_O_5	Output	—	Arbiter acknowledgment to write request from write channel 5
BUSER_O_5	Output	—	Write completion to write channel 5
AWSIZE_I_6	Input	8 bits	Write burst size for write channel 6
WDATA_I_6	Input	[AXI_DATA_WIDTH-1:0]	Video data Input to write channel 6
WVALID_I_6	Input	—	Write data valid to write channel 6
AWVALID_I_6	Input	—	Write request from write channel 6
AWADDR_I_6	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 6
AWREADY_O_6	Output	—	Arbiter acknowledgment to write request from write channel 6
BUSER_O_6	Output	—	Write completion to write channel 6
AWSIZE_I_7	Input	8 bits	Write burst size from write channel 7
WDATA_I_7	Input	[AXI_DATA_WIDTH-1:0]	Video data Input to write channel 7
WVALID_I_7	Input	—	Write data valid to write channel 7
AWVALID_I_7	Input	—	Write a request from write channel 7
AWADDR_I_7	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to happen from write channel 7
AWREADY_O_7	Output	—	Arbiter acknowledgment to write request from write channel 7

BUSER_O_7	Output	—	Write completion to write channel 7

The following table lists the inputs and output ports of the DDR AXI4 Arbiter for the native interface.
Table 2-3. Input and Output Ports for Native Arbiter Interface

Signal Name	Direction	Width	Description
reset_i	Input	—	Active low asynchronous reset signal to design
sys_clk_i	Input	—	System clock
ddr_ctrl_ready_i	Input	—	Receives the ready input signal from the DDR controller
r0_req_i	Input	—	Read request from initiator 0
r0_burst_size_i	Input	8 bits	Read burst size
r0_rstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 0
r0_ack_o	Output	—	Arbiter acknowledgment to read request from initiator 0

……..continued

Signal Name	Direction	Width	Description
r0_data_valid_o	Output	—	Read data valid from read channel 0
r0_done_o	Output	—	Read completion to initiator 0
r1_req_i	Input	—	Read request from initiator 1
r1_burst_size_i	Input	8 bits	Read burst size
r1_rstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 1
r1_ack_o	Output	—	Arbiter acknowledgment to read request from initiator 1
r1_data_valid_o	Output	—	Read data valid from read channel 1
r1_done_o	Output	—	Read completion to initiator 1
r2_req_i	Input	—	Read request from initiator 2
r2_burst_size_i	Input	8 bits	Read burst size
r2_rstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 2
r2_ack_o	Output	—	Arbiter acknowledgment to read request from initiator 2
r2_data_valid_o	Output	—	Read data valid from read channel 2
r2_done_o	Output	—	Read completion to initiator 2
r3_req_i	Input	—	Read request from initiator 3
r3_burst_size_i	Input	8 bits	Read burst size

r3_rstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 3
r3_ack_o	Output	—	Arbiter acknowledgment to read request from initiator 3
r3_data_valid_o	Output	—	Read data valid from read channel 3
r3_done_o	Output	—	Read completion to initiator 3
r4_req_i	Input	—	Read request from initiator 4
r4_burst_size_i	Input	8 bits	Read burst size
r4_rstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 4
r4_ack_o	Output	—	Arbiter acknowledgment to read request from initiator 4
r4_data_valid_o	Output	—	Read data valid from read channel 4
r4_done_o	Output	—	Read completion to initiator 4
r5_req_i	Input	—	Read request from initiator 5
r5_burst_size_i	Input	8 bits	Read burst size
r5_rstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 5
r5_ack_o	Output	—	Arbiter acknowledgment to read request from initiator 5
r5_data_valid_o	Output	—	Read data valid from read channel 5
r5_done_o	Output	—	Read completion to initiator 5
r6_req_i	Input	—	Read request from initiator 6
r6_burst_size_i	Input	8 bits	Read burst size
r6_rstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 6
r6_ack_o	Output	—	Arbiter acknowledgment to read request from initiator 6
r6_data_valid_o	Output	—	Read data valid from read channel 6
r6_done_o	Output	—	Read completion to initiator 6
r7_req_i	Input	—	Read request from initiator 7
r7_burst_size_i	Input	8 bits	Read burst size

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Signal Name	Direction	Width	Description
r7_rstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address from where read has to be started for read channel 7
r7_ack_o	Output	—	Arbiter acknowledgment to read request from initiator 7
r7_data_valid_o	Output	—	Read data valid from read channel 7

r7_done_o	Output	—	Read completion to initiator 7
rdata_o	Output	[AXI_DATA_WIDTH – 1 :0]	Video data output from read channel
w0_burst_size_i	Input	8 bits	Write burst size
w0_data_i	Input	[AXI_DATA_WIDTH – 1 :0]	Video data input to write channel 0
w0_data_valid_i	Input	—	Write data valid to write channel 0
w0_req_i	Input	—	Write request from initiator 0
w0_wstart_addr _i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 0
w0_ack_o	Output	—	Arbiter acknowledgment to write request from initiator 0
w0_done_o	Output	—	Write completion to initiator 0
w1_burst_size_i	Input	8 bits	Write burst size
w1_data_i	Input	[AXI_DATA_WIDTH – 1 :0]	Video data input to write channel 1
w1_data_valid_i	Input	—	Write data valid to write channel 1
w1_req_i	Input	—	Write request from initiator 1
w1_wstart_addr _i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 1
w1_ack_o	Output	—	Arbiter acknowledgment to write request from initiator 1
w1_done_o	Output	—	Write completion to initiator 1
w2_burst_size_i	Input	8 bits	Write burst size
w2_data_i	Input	[AXI_DATA_WIDTH – 1 :0]	Video data input to write channel 2
w2_data_valid_i	Input	—	Write data valid to write channel 2
w2_req_i	Input	—	Write request from initiator 2
w2_wstart_addr _i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 2
w2_ack_o	Output	—	Arbiter acknowledgment to write request from initiator 2
w2_done_o	Output	—	Write completion to initiator 2
w3_burst_size_i	Input	8 bits	Write burst size
w3_data_i	Input	[AXI_DATA_WIDTH – 1 :0]	Video data input to write channel 3
w3_data_valid_i	Input	—	Write data valid to write channel 3
w3_req_i	Input	—	Write request from initiator 3
w3_wstart_addr _i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 3

w3_ack_o	Output	—	Arbiter acknowledgment to write request from initiator 3
w3_done_o	Output	—	Write completion to initiator 3
w4_burst_size_i	Input	8 bits	Write burst size
w4_data_i	Input	[AXI_DATA_WIDTH – 1 :0]	Video data input to write channel 4
w4_data_valid_i	Input	—	Write data valid to write channel 4
w4_req_i	Input	—	Write request from initiator 4
w4_wstart_addr _i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to happen from write ch annel 4

……..continued			
Signal Name	**Directio n**	**Width**	**Description**
w4_ack_o	Output	—	Arbiter acknowledgment to write request from initiator 4
w4_done_o	Output	—	Write completion to initiator 4
w5_burst_size_i	Input	8 bits	Write burst size
w5_data_i	Input	[AXI_DATA_WIDTH – 1 :0]	Video data input to write channel 5
w5_data_valid_i	Input	—	Write data valid to write channel 5
w5_req_i	Input	—	Write request from initiator 5
w5_wstart_addr _i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 5
w5_ack_o	Output	—	Arbiter acknowledgment to write request from initiator 5
w5_done_o	Output	—	Write completion to initiator 5
w6_burst_size_i	Input	8 bits	Write burst size
w6_data_i	Input	[AXI_DATA_WIDTH – 1 :0]	Video data input to write channel 6
w6_data_valid_i	Input	—	Write data valid to write channel 6
w6_req_i	Input	—	Write request from initiator 6
w6_wstart_addr _i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 6
w6_ack_o	Output	—	Arbiter acknowledgment to write request from initiator 6
w6_done_o	Output	—	Write completion to initiator 6
w7_burst_size_i	Input	8 bits	Write burst size
w7_data_i	Input	[AXI_DATA_WIDTH – 1 :0]	Video data input to write channel 7

w7_data_valid_i	Input	—	Write data valid to write channel 7
w7_req_i	Input	—	Write request from initiator 7
w7_wstart_addr_i	Input	[AXI_ADDR_WIDTH – 1:0]	DDR address to which write has to be happen from write channel 7
w7_ack_o	Output	—	Arbiter acknowledgment to write request from initiator 7
w7_done_o	Output	—	Write completion to initiator 7
AXI I/F Signals			
Read Address Channel			
arid_o	Output	[AXI_ID_WIDTH – 1:0]	Read address ID. Identification tag for the read address group of signals.
araddr_o	Output	[AXI_ADDR_WIDTH – 1:0]	Read address. Provides the initial address of a read bur st transaction. Only the start address of the burst is provided.
arlen_o	Output	[7:0]	Burst length. Provides the exact number of transfers in a burst. This information determines the number of data tr ansfers associated with the address.
arsize_o	Output	[2:0]	Burst size. Size of each transfer in the burst.
arburst_o	Output	[1:0]	Burst type. Coupled with the size information, details ho w the address for each transfer within the burst is calculated. Fixed to 2’b01 à Incremental address burst.
arlock_o	Output	[1:0]	Lock type. Provides additional information about the ato mic characteristics of the transfer. Fixed to 2’b00 à Normal Access.

……..continued

Signal Name	Direction	Width	Description
arcache_o	Output	[3:0]	Cache type. Provides additional information about the ca cheable characteristics of the transfer. Fixed to 4’b0000 à Non-cacheable and non-bufferable.
arprot_o	Output	[2:0]	Protection type. Provides protection unit information for t he transaction. Fixed to 3’b000 à Normal, secure data access.

arvalid_o	Output	—	Read address valid. When HIGH, the read address and control information is valid and remain high until the address acknowledge signal, aready, is high. 1 = Address and control information valid 0 = Address and control information not valid
arready_o	Input	—	Read address ready. The target is ready to accept an ad dress and associated control signals. 1 = target ready 0 = target not ready
Read Data Channel			
rid	Input	[AXI_ID_WIDTH – 1:0]	Read ID tag. ID tag of the read data group of signals. Th e rid value is generated by the target and must match th e arid value of the read transaction to which it is respond ing.
rdata	Input	[AXI_DATA_WIDTH – 1 :0]	Read data
rresp	Input	[1:0]	Read response. The status of the read transfer. Allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
rlast	Input	—	Read last. Last transfer in a read burst.
rvalid	Input	—	Read valid. Required read data is available and the read transfer can complete. 1 = read data available 0 = read data not available
rready	Output	—	Read ready. Initiator can accept the read data and respo nse information. 1= initiator ready 0 = initiator not ready
Write Address Channel			
awid	Output	[AXI_ID_WIDTH – 1:0]	Write address ID. Identification tag for the write address group of signals.
awaddr	Output	[AXI_ADDR_WIDTH – 1:0]	Write address. Provides the address of the first transfer i n a write burst transaction. The associated control signal s are used to determine the addresses of the remaining t ransfers in the burst.

awlen	Output	[7:0]	Burst length. Provides the exact number of transfers in a burst. This information determines the number of data tr ansfers associated with the address.
awsize	Output	[2:0]	Burst size. Size of each transfer in the burst. Byte lane st robes indicate exactly which byte lanes to update.
awburst	Output	[1:0]	Burst type. Coupled with the size information, details ho w the address for each transfer within the burst is calculated. Fixed to 2'b01 à Incremental address burst.

……..continued			
Signal Name	**Direction**	**Width**	**Description**
awlock	Output	[1:0]	Lock type. Provides additional information about the ato mic characteristics of the transfer. Fixed to 2'b00 à Normal Access.
awcache	Output	[3:0]	Cache type. Indicates the bufferable, cacheable, write- t hrough, write-back, and allocate attributes of the transac tion. Fixed to 4'b0000 à Non-cacheable and non-bufferable.
awprot	Output	[2:0]	Protection type. Indicates the normal, privileged, or secu re protection level of the transaction and whether the tra nsaction is a data access or an instruction access. Fixed to 3'b000 à Normal, secure data access.
awvalid	Output	—	Write address valid. Indicates that valid write address an d control information are available. 1 = address and control information available 0 = address and control information not available. The a ddress and control information remain stable until the ad dress acknowledge signal, awready, goes HIGH.
awready	Input	—	Write address ready. Indicates that the target is ready to accept an address and associated control signals. 1 = target ready 0 = target not ready
Write Data Channel			
wdata	Output	[AXI_DATA_WIDTH – 1 :0]	Write data

wstrb	Output	[AXI_DATA_WIDTH – 8 :0]	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eig ht bits of the write data bus.
wlast	Output	—	Write last. Last transfer in a write burst.
wvalid	Output	—	Write valid. Valid write data and strobes are available. 1 = write data and strobes available 0 = write data and strobes not available
wready	Input	—	Write ready. Target can accept the write data. 1 = target ready 0 = target not ready
Write Response Channel			
bid	Input	[AXI_ID_WIDTH – 1:0]	Response ID. The identification tag of the write response. The bid value must match the awid value of th e write transaction to which the target is responding.
bresp	Input	[1:0]	Write response. Status of the write transaction. The allo wable responses are OKAY, EXOKAY, SLVERR, and DE CERR.
bvalid	Input	—	Write response valid. Valid write response is available. 1 = write response available 0 = write response not available
bready	Output	—	Response ready. Initiator can accept the response infor mation. 1 = initiator ready 0 = initiator not ready

Timing Diagrams (Ask a Question)

This section discusses DDR_AXI4_Arbiter timing diagrams. The following figures show the connection of the read and write request inputs, starting memory address, write inputs from the external initiator, read or write acknowledgment, and read or write completion inputs given by arbiter.

Figure 3-1. Timing Diagram for Signals used in Writing/Reading through AXI4 Interface

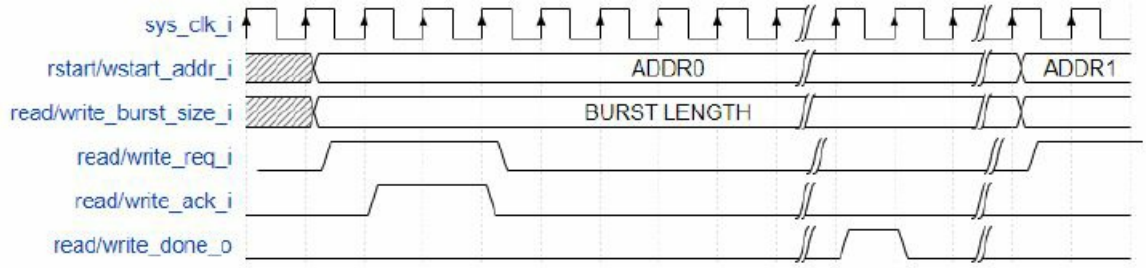


Figure 3-2. Timing Diagram for Writing into Internal Memory

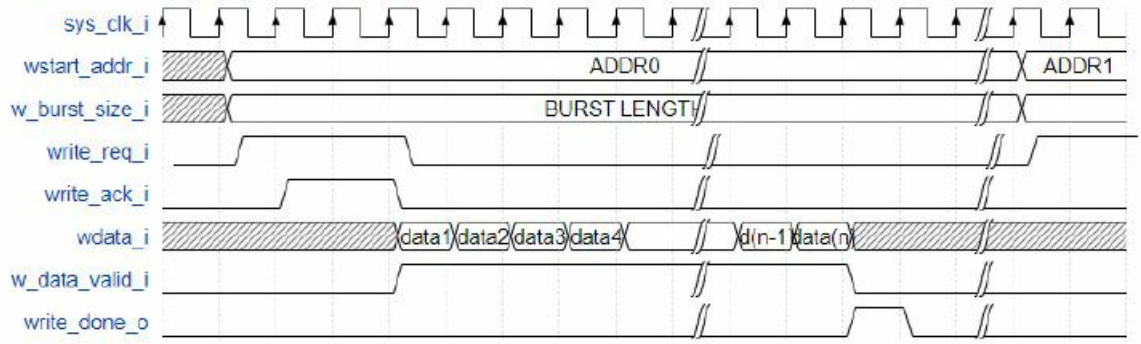
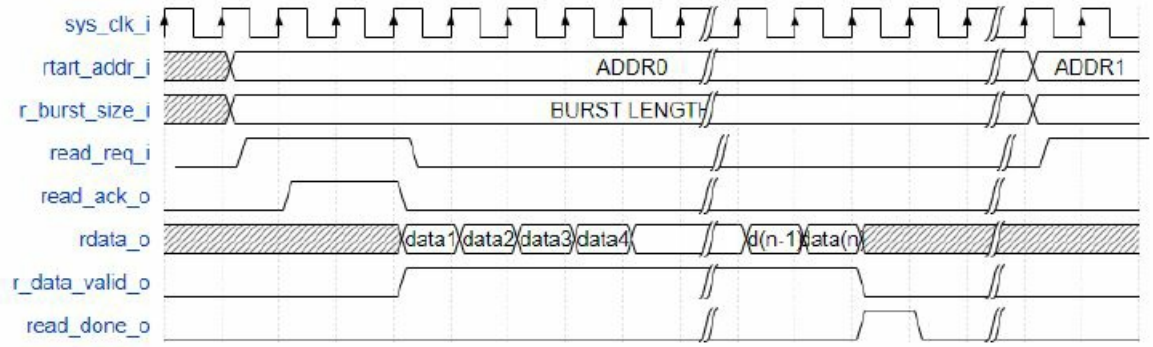


Figure 3-3. Timing Diagram for Data Received through DDR AXI4 Arbiter for Read Channels



Testbench (Ask a Question)

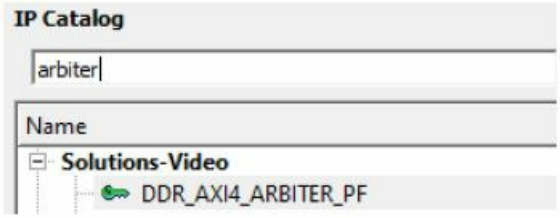
A unified testbench is used to verify and test DDR_AXI4_Arbiter called as user testbench. Testbench is provided to check the functionality of the DDR_AXI4_Arbiter IP. This testbench works only for two read channels and two write channels with Bus Interface configuration.

Simulation (Ask a Question)

The following steps describe how to simulate the core using the testbench:

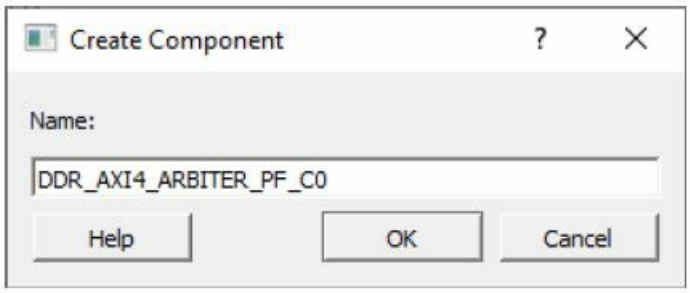
1. Open the Libero® SoC Catalog tab, expand Solutions-Video, double-click DDR_AXI4_Arbiter, and then click OK. The documentation associated with the IP are listed under Documentation. Important: If you do not see the Catalog tab, navigate to View > Windows menu and click Catalog to make it visible.

Figure 4-1. DDR_AXI4_Arbiter IP Core in Libero SoC Catalog



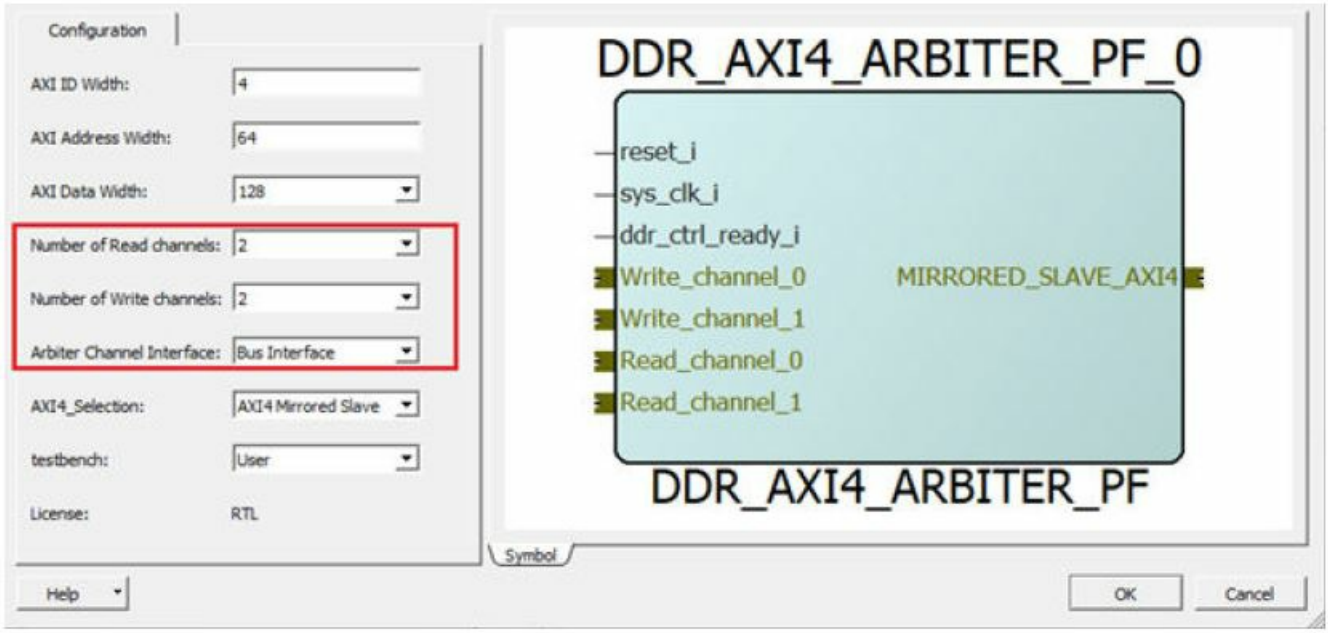
Create component window appears as shown in the following. Click OK. Ensure that the Name is DDR_AXI4_ARBITER_PF_C0.

Figure 4-2. Create Component



Configure the IP for 2 read channels, 2 write channels and select Bus Interface as shown in the following figure and click OK to generate the IP.

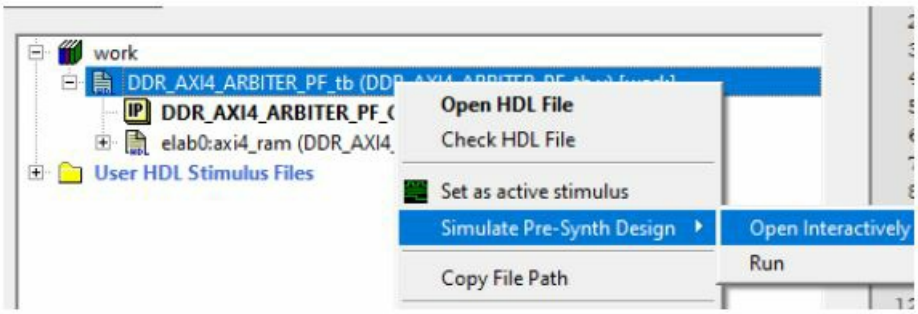
Figure 4-3. Configuration



On the Stimulus Hierarchy tab, select the testbench (DDR_AXI4_ARBITER_PF_tb.v), right click and then click Simulate Pre-Synth Design > Open Interactively.

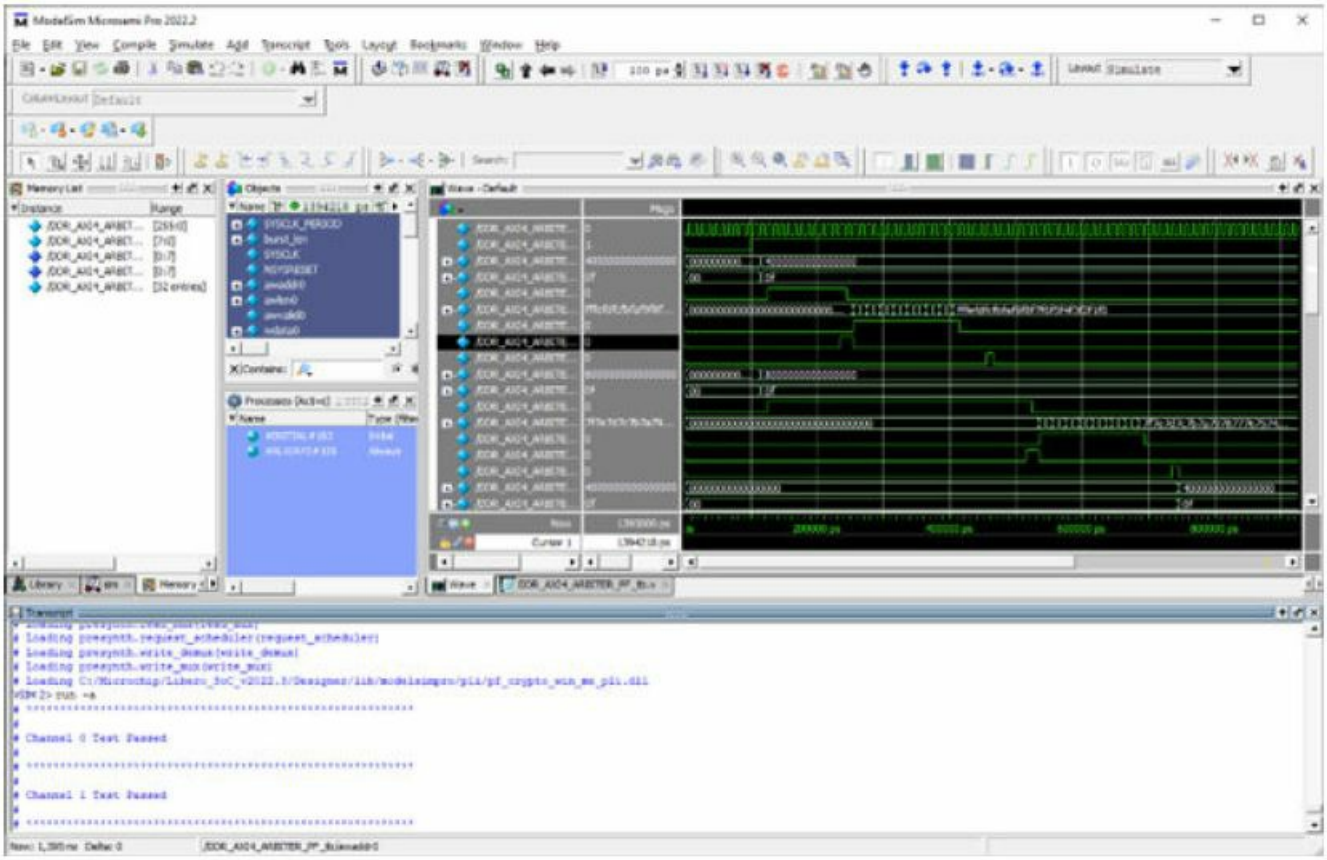
Important: If you do not see the Stimulus Hierarchy tab, navigate to View > Windows menu and click Stimulus Hierarchy to make it visible.

Figure 4-4. Simulating Pre-Synthesis Design



ModelSim opens with the testbench file, as shown in the following figure.

Figure 4-5. ModelSim Simulation Window



Important: If the simulation is interrupted due to the runtime limit specified in the .do file, use the run -all command to complete the simulation.

Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	04/2023	The following is the list of changes in revision A of the document: • Migrated the document to the Microchip template. • Updated the document number to DS00004976A from 50200950. • Added 4. Testbench.
2.0	—	The following is the list of changes in revision 2.0 of the document: • Added Figure 1-2. • Added Table 2-2. • Updated the names of some input and output signal names in Table 2-2.
1.0	—	Initial Release.

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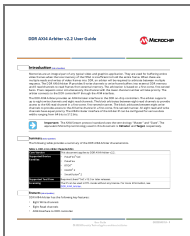	MICROCHIP DDR AXI4 Arbiter [pdf] User Guide DDR AXI4 Arbiter, DDR AXI4, Arbiter

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