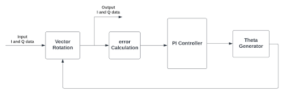

MICROCHIP Costas Loop Management User Guide

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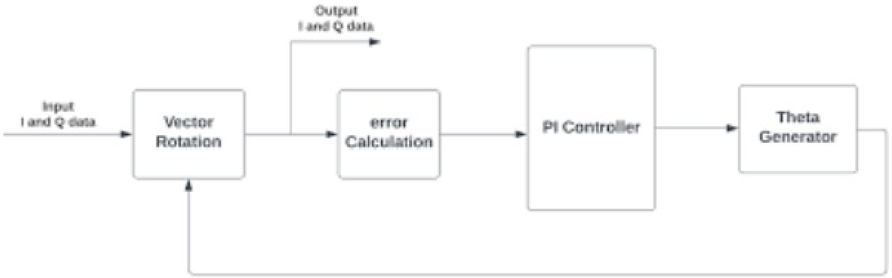


Contents

Introduction

In wireless transmission, the Transmitter (Tx) and Receiver (Rx) are separated by a distance and electrically isolated. Even though both Tx and Rx are tuned to the same frequency, there is a frequency offset between the carrier frequencies due to the ppm difference between the oscillators used in Tx and Rx. The frequency offset is compensated by using the data aided or non-data-aided (blind) synchronization methods.

A Costas Loop is a non-data-aided PLL-based method for carrier frequency offset compensation. The primary application of Costas loops is in wireless receivers. By using this, the frequency offset between the Tx and Rx is compensated without the help of pilot tones or symbols. The Costas Loop is implemented for the BPSK and QPSK modulations with a change in the error calculation block. Employing a Costas Loop for the phase or frequency sync might result in phase ambiguity, which must be corrected through techniques such as differential encoding.

Summary

The following table provides a summary of the Costas Loop characteristics.

Table 1. Costas Loop characteristics

Core Version	This document applies to Costas Loop v1.0.
Supported Device Families	• Polar Fire® SoC • Polar Fire
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Licensing	Costas Loop IP clear RTL is license locked and the encrypted RTL is freely available with any Libero license. **Encrypted RTL:** Complete encrypted RTL code is provided for the core, enabling the core to be instantiated with Smart Design. Simulation, Synthesis, and Layout can be performed with Libero software. **Clear RTL:** Complete RTL source code is provided for the core and test benches.

Features

Costas Loop has the following key features:

- Supports BPSK and QPSK modulations
- Tunable loop parameters for wide frequency range

Implementation of IP Core in Libero® Design Suite
IP core must be installed to the IP Catalog of the Libero SoC software. This is installed automatically through the IP
Catalog update function in the Libero SoC software, or the IP core is manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, the core is configured, generated, and instantiated within the Smart Design tool for inclusion in the Libero project list.

Device Utilization and Performance

The following tables list the device utilization used for Costas Loop.

Table 2. Costas Loop Utilization for QPSK

Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T	1256	197	200	0	0	6	0
PolarFire	MPF300T	1256	197	200	0	0	6	0

Table 3. Costas Loop Utilization for BPSK

Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T	1202	160	200	0	0	7	0
Polar Fire	MPF300T	1202	160	200	0	0	7	0

Important:

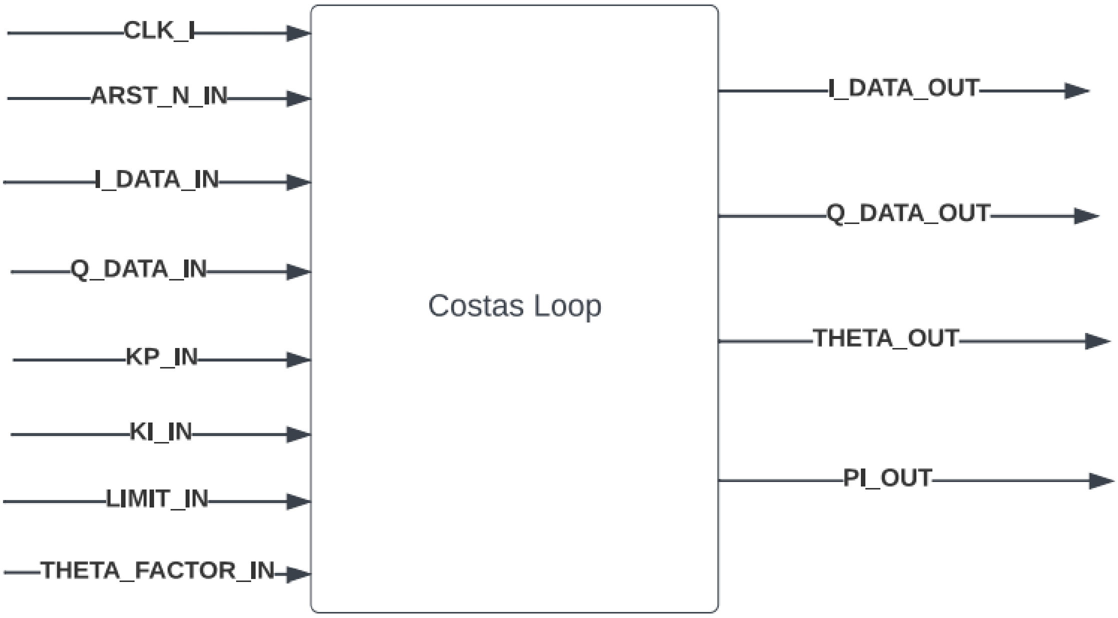
1. The data in this table is captured using typical synthesis and layout settings. CDR reference clock source was set to Dedicated with other configurator values unchanged.
2. Clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers.

Functional Description

This section describes the implementation details of the Costas Loop.

The following figure shows the system-level block diagram of the Costas Loop.

Figure 1-1. System-Level Block Diagram of Costas Loop



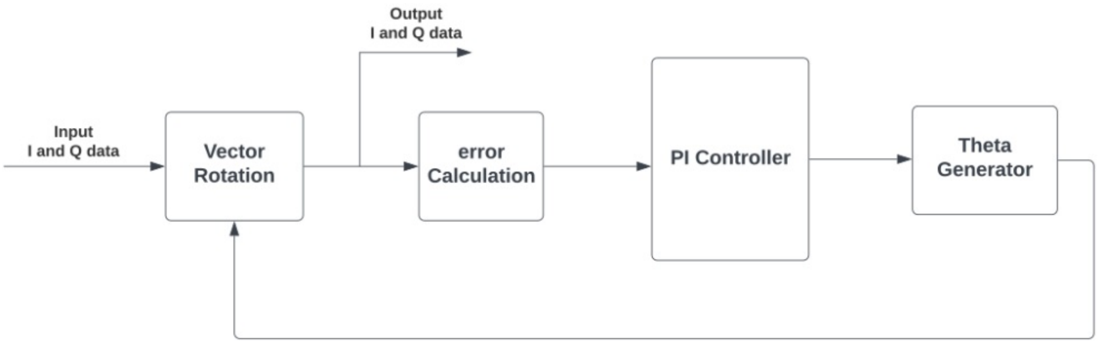
The latency between the input and output of the Costas top is 11 clock cycles. The THETA_OUT latency is 10 clock
cycles. Kp (proportionality constant), Ki (integral constant), Theta factor, and LIMIT factor must be fixed according to the noise environment and the frequency offset being introduced. The Costas Loop takes some time to lock, like in the PLL operation. Some packets might be lost during the initial locking time of the Costas Loop.

Architecture

Implementation of the Costas Loop requires the following four blocks:

- Loop Filter (PI Controller in this implementation)
- Theta Generator
- Error Calculation
- Vector Rotation

Figure 1-2. Costas Loop Block Diagram



The error for a specific modulation scheme is calculated based on the rotated I and Q values using the Vector Rotation Module. The PI controller computes frequency based on the error, proportional gain Kp, and integral gain Ki. The maximum frequency offset is set as a limit value for the PI controller's frequency output. The Theta Generator module generates the angle by integration. The theta factor input determines the slope of integration and depends.

on the sampling clock. The angle generated from the Theta Generator is used to rotate the I and Q input values. The error function is specific to a modulation type. As the PI controller is implemented in fixed-point format, scaling is performed on proportional and integral outputs of PI controller.

```
P_out = round((error*Kp)/(2^10))
I_out = I_out_previous + round((error*Ki)/(2^16))
PI_out = P_out + I_out;
```

Similarly, scaling is implemented for theta integration.

```
Theta = Theta_previous + round((freq*Theta_factor)/(2^18))
```

IP Core Parameters and Interface Signals

This section discusses the parameters in the Costas Loop GUI configurator and I/O signals.

Configuration Settings

The following table lists the description of the configuration parameters used in the hardware implementation of Costas Loop. These are generic parameters are varied as per the requirement of the application.

Table 2-1. Configuration Parameter

Signal Name	Description
Modulation Type	BPSK or QPSK

Inputs and Outputs Signals

The following table lists the input and output ports of Costas Loop.

Table 2-2. Input and Output Signals

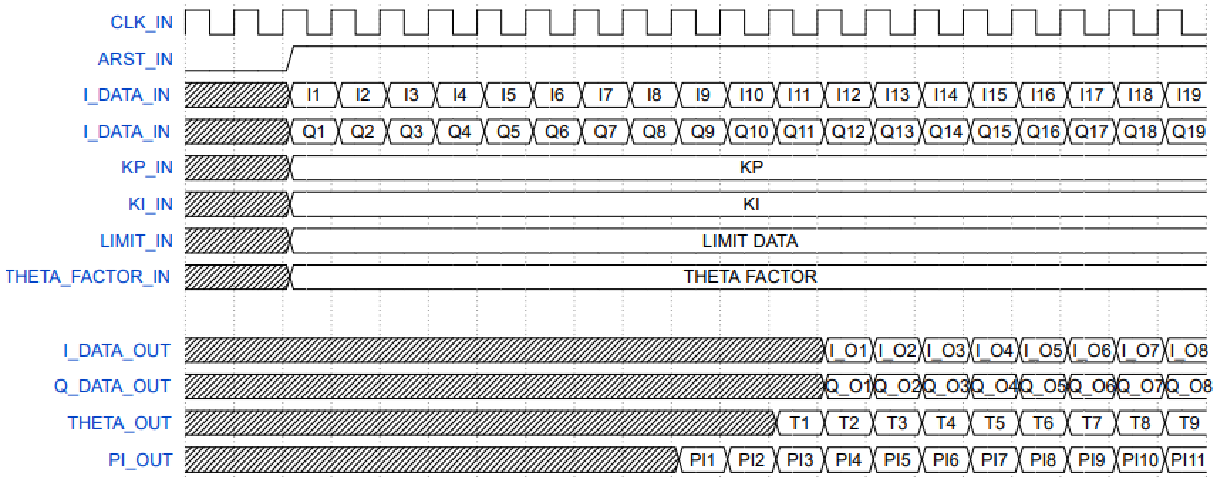
Signal Name	Direction	Signal Type	Width	Description
CLK_I	Input	—	1	Clock Signal
ARST_N_IN	Input	—	1	Active low asynchronous reset signal
I_DATA_IN	Input	Signed	16	In phase / Real data input
Q_DATA_IN	Input	Signed	16	Quadrature / Imaginary data Input
KP_IN	Input	Signed	18	Proportionality constant of PI controller
KI_IN	Input	Signed	18	Integral constant of PI controller
LIMIT_IN	Input	Signed	18	Limit for the PI controller
THETA_FACTOR_IN	Input	Signed	18	Theta factor for theta integration.
I_DATA_OUT	Output	Signed	16	In phase / Real data Output
Q_DATA_OUT	Output	Signed	16	Quadrature / Imaginary data Output
THETA_OUT	Output	Signed	10	Calculated Theta index (0-1023) for the verification
PI_OUT	Output	Signed	18	PI output

Timing Diagrams

This section discusses the Costas Loop timing diagram.

The following figure shows the timing diagram of Costas Loop.

Figure 3-1. Costas Loop Timing Diagram



Testbench

A unified testbench is used to verify and test Costas Loop called as user test bench. Test bench is provided to check the functionality of the Costas Loop IP.

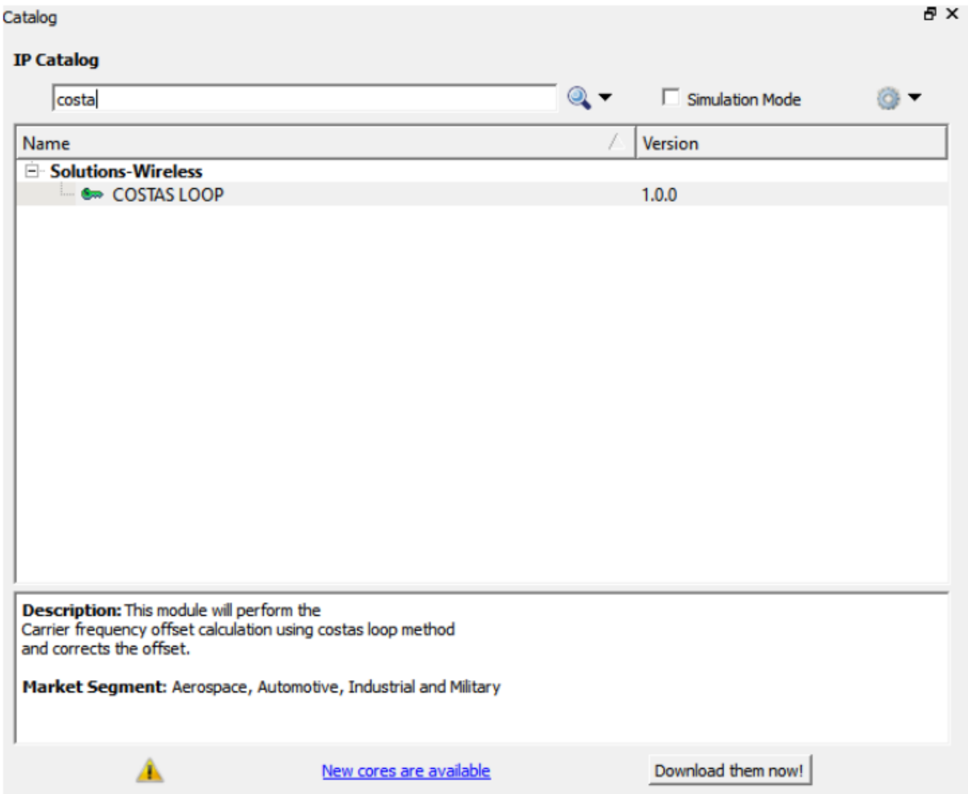
Simulation Rows

To simulate the core using the testbench, perform th following steps:

1. Open the Libero SoC application, click Catalog tab, expand Solutions-Wireless, double-click COSTAS LOOP, and then click OK. The documentation associated with the IP are listed under Documentations.

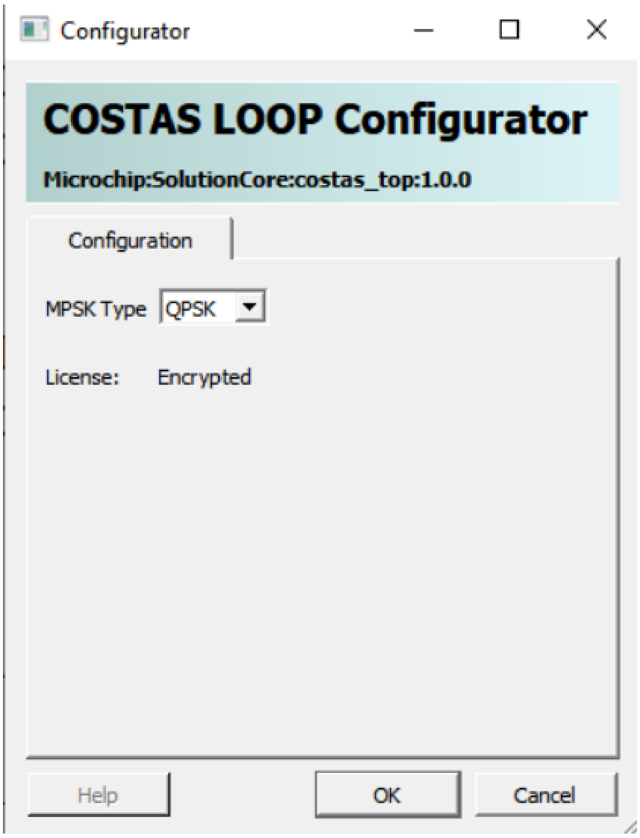
   Important: If you do not see the Catalog tab, navigate to View > Windows menu and click Catalog to make it visible.

   Figure 4-1. Costas Loop IP Core in Libero SoC Catalog



2. Configure the IP as per your requirement.

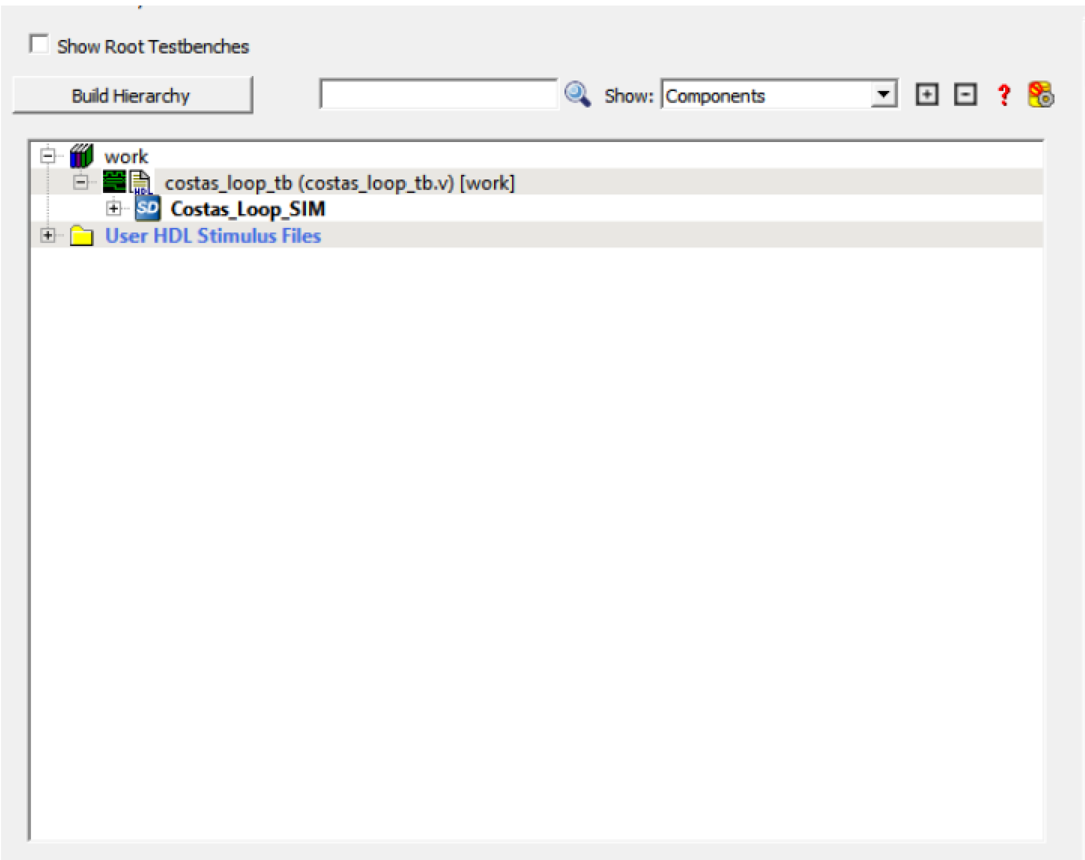
Figure 4-2. Configurator GUI



Promote all the signals to top level and generate the design

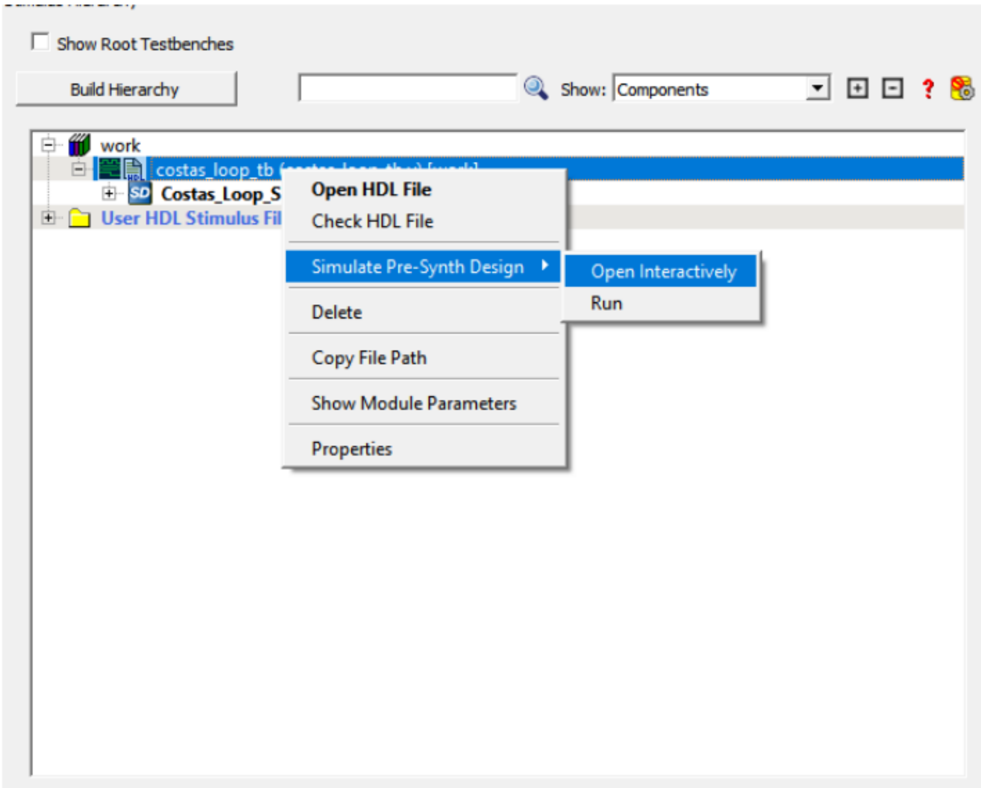
3. On the Stimulus Hierarchy tab, click Build Hierarchy.

Figure 4-3. Build Hierarchy



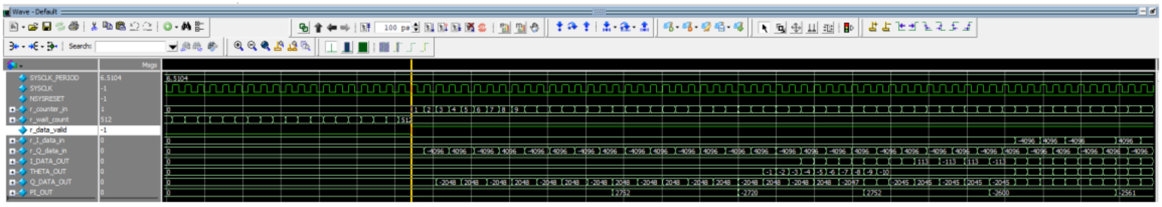
4. On the Stimulus Hierarchy tab, right-click the testbench (Costas loop bevy), point to Simulate Present Design, and then click Open Interactively

Figure 4-4. Simulating Pre-Synthesis Design



ModelSim opens with the testbench file, as shown in the following figure.

Figure 4-5. ModelSim Simulation Window



Important: If the simulation is interrupted due to the runtime limit specified in the .do file, use the run -all command to complete the simulation

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	03/2023	Initial release

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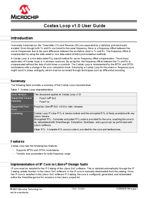	MICROCHIP Costas Loop Management [pdf] User Guide Costas Loop Management, Loop Management, Management

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