MICROCHIP CoreSmartBERT v2.9 Software User Guide

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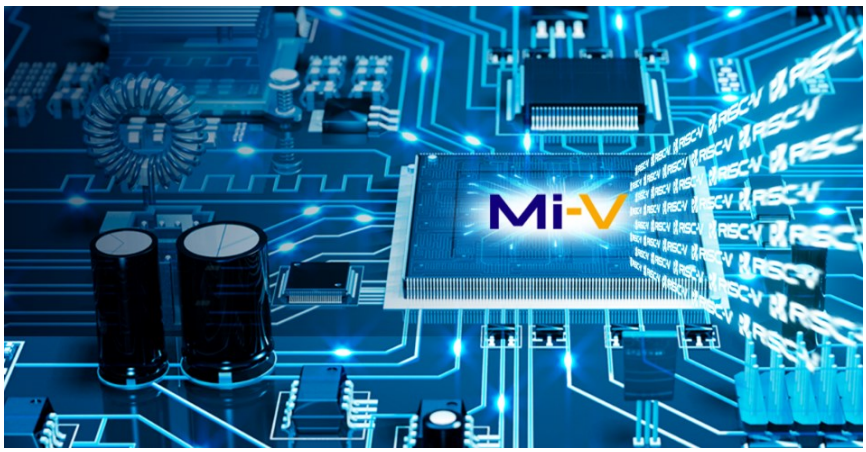


Contents

Introduction

The CoreSmartBERT core provides a broad-based evaluation and demonstration platform for PolarFire® and PolarFire SoC transceivers. CoreSmartBERT is configurable to use different transceivers, clocking topologies,

line rates, and reference clock rates. Data pattern generators and checkers are included for each transceiver, giving several different Pseudo Random Binary Sequences (PRBS) (27 , 29 , 223, and 231). The pattern generator sends data out through the transmitter. The pattern checker accepts data through the receiver and checks it against an internally generated pattern. These patterns are optimized for the logic width that has been selected at run time. SmartDebug provides the user interface to this core.

This user guide provides information on the CoreSmartBERT IP core and the features it supports. The purpose of this IP core is to add more test features for the transceiver, so that the end user can evaluate the Physical Media Attachment (PMA) functionality of transceiver on a board. The SmartDebug tool interfaces with this core, which allows the user to have an interactive Graphical User Interface (GUI) control.

Features

CoreSmartBERT has the following features:

- Supports PolarFire and PolarFire SoC Transceiver built-in PRBS Generator or Checker
- Generates a List of Patterns
- Inserts an Error into the Transmit Pattern
- Checking of Errors in the Receive Pattern
- Instantiating the Pattern Functionality Several Times to Support Multiple Lanes Simultaneously

Supported Families

CoreSmartBERT supports the following families:

- PolarFire® SoC
- PolarFire

Device Utilization and Performance

The following Field Programmable Gate Array (FPGA) device families implement CoreSmartBERT. The following table lists the summary of the implementation data for CoreSmartBERT.

Table 1. CoreSmartBERT Utilization

Device Details		Resources			Performance (MHz)
Family	**Device**	**LUTs**	**DFF**	**Logic Elements**	
PolarFire SoC	MPFS250T	2860	1082	3050	125
PolarFire	MPF300T	2860	1082	3050	125

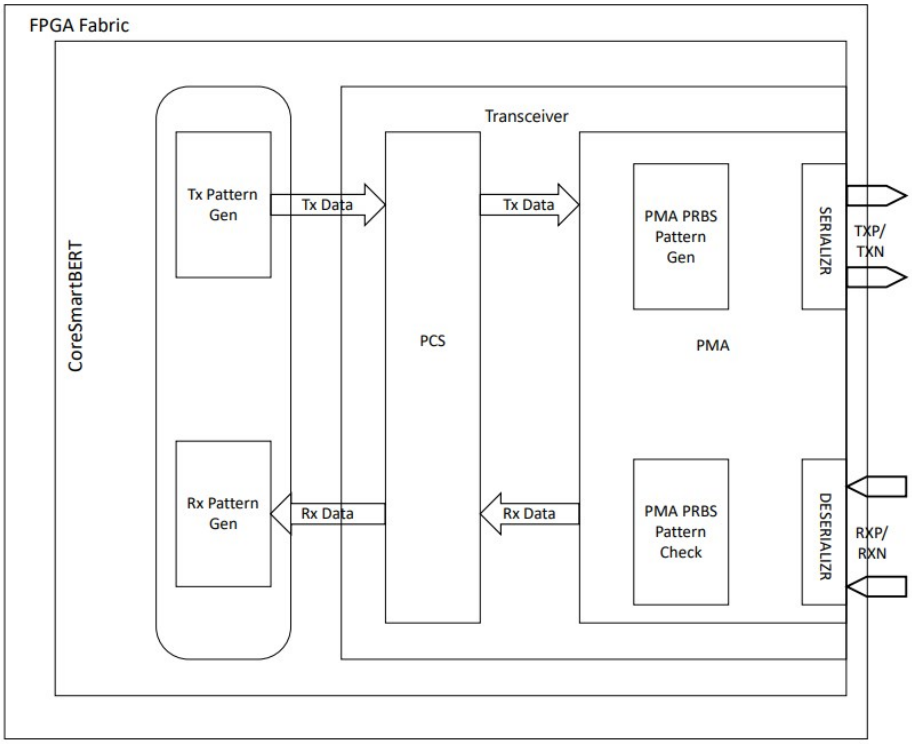
Note: We get the data in the preceding table using typical synthesis and layout settings: CDR reference clock source as Dedicated and unchanged other configurator values.

Functional Description

CoreSmartBERT includes the transceiver, which interfaces with the SmartDEBUG tool through a user control GUI, to run the hardened PRBS generator and checkers. It also has fabric pattern generators and checkers with more

features (for example, error injection) than the ones included in transceiver.

Figure 1-1. CoreSmartBERT Block Diagram



TX Pattern Gen
This transmitter block generates the following pattern:

- PRBS 7, 9, 23, 31 with error insertion logic

RX Pattern CHK
The receiver block checks the following patterns:

- PRBS 7, 9, 23, 31

Transceiver
The transceiver is PolarFire/PolarFire SoC's transceiver macro in Physical Media Attachment (PMA) mode.

Operation

This section describes the operation performed by CoreSmartBERT.

Test Pattern Overview
CoreSmartBERT supports the following test patterns.

PRBS
Pseudo Random Binary Sequence (PRBS) test patterns generate deterministic sequences with the properties of highly random signals, for example: white noise.

CoreSmartBERT supports the built in PBRS pattern generators and checkers in the transceiver and add the support for the fabric PRBS pattern generators and checkers with the ability to inject errors into the transmitter path.

These include support for the following

- PRBS 7
- PRBS 9
- PRBS 23
- PRBS 31

Smart Debug Tool
SmartDebug provides the user interface to control the CoreSmartBERT core to use its features.

SmartDebug has the following capabilities:

- Ability to control CoreSmartBERT and have the signal integrity controls on the screen at the same time
- Automatic detection of the presence of CoreSmartBERT in the design
- Ability to select the particular transceiver lane associated with CoreSmartBERT
- Availability of several patterns options
- An ability to enable to start the pattern transmitter
- An ability to enable to start the pattern receiver
- A button to insert a single error
- An error counter with a clear button

SLE_DEBUG Marco
SLE_DEBUG Marco is used to communicate with SmartDebug. The SLE_DEBUG mechanism gives ability to run synthesis while preserving a set of registers. It provides ability to identify, rename, and classify registers for SmartDebug.

CoreSmartBERT has SLE_DEBUG write and read registers that are used to inform the Smart Debug tool of parameters settings chosen, IP core versions number, and control various functions (for example, error injection, read errors, and so on.). The following table describes the SLE_DEBUG registers that are used in CoreSmartBERT.

Table 2-1. SLE_DEBUG Registers

Bits	Function	Type	Description
14	SLE_DATA_RATE	R	Reads data rate selected from the GUI. 1: 250 Mbps2: 1000 Mbps3: 1250 Mbps4: 2500 Mbps5: 3125 Mbps6: 5000 Mbps7: 6250 Mbps8: 8000 Mbps9: 10000 Mbps10: 10312.5Mbps
4	SLE_TX_CLK_DIV_FACTOR	R	Reads **Tx Clock Divide Factor** selected from the GUI.
1	SLE_CDR_REFERENCE_CLK_SOURCE	R	Reads the CDR Reference Clock Source selected from the GUI:0: Dedicated1: Fabric
4	SLE_CDR_REFERENCE_CLK_FREQ	R	Reads the CDR Reference Clock Frequency selected from the GUI:0: 25.001: 31.252: 50.003: 62.504: 75.005: 100.006: 125.007: 150.008: 156.259: 312.50
2	SLE_NUMBER_OF_LANES	R	Reads the number of lanes this IP core has enabled from the GUI.
1	SLE_PATTERN_PRBS7	R	Reads the PRBS7 pattern enable from the GUI.
1	SLE_PATTERN_PRBS9	R	Reads the PRBS9 pattern enable from the GUI.
1	SLE_PATTERN_PRBS23	R	Reads the PRBS23 pattern enable from the GUI.
1	SLE_PATTERN_PRBS31	R	Reads the PRBS31 pattern enable from the GUI.
16	SLE_CPZ_VERSION	R	Reads the CPZ Version number.This registers represents 8bit major and 8bit minor version number.For example, v2.1 = {8’d2, 8’d1}

……..continued

Bits	Function	Type	Description
4	SLE_TX_LANE[n]_PATTEN_GEN	RW	Transmitter Pattern Generator: 0: PRBS71: PRBS 91: PRBS232: PRBS31**Note:** Default value is set to 0.
1	SLE_TX_LANE[n]_GEN_EN	RW	Transmitter Pattern Generator Enable: 0: Disabled1: Enabled**Note:** Default value is set to 0.
4	SLE_RX_LANE[n]_PATTEN_CHK	RW	Receiver Pattern Checker: 0: PRBS71: PRBS92: PRBS233: PRBS31**Note:** Default value is set to 0.
1	SLE_RX_LANE[n]_CHR_EN	RW	Receiver Pattern Checker Enable: 0: Disabled1: Enabled**Note:** Default value is set to 0.
32	SLE_RX_LANE[n]_ERR_CNT	R	Receiver error counter.
1	SLE_ RX_LANE[n]_ERR_CNT_CLR	RW	Receiver error counter clear button.
1	SLE_ RX_LANE[n]_ALIGN	R	Receiver channel aligned to pattern.

Interface

This section discusses the parameters in the CoreSmartBERT GUI configurator and I/O signals.

Configuration GUI Parameters

The following table describes the UI parameters for configuring the CoreSmartBERT core.

Note: The Name column shows the actual parameter name used in RTL. The Description column starts with parameter name as it appear in the CoreSmartBERT configurator (GUI interface). These two names are used interchangeably throughout the document.

Table 3-1. CoreSmartBERT Parameters Descriptions

Name	Range	Default	Description
UI_PATTERN_PRBS7	0 or 1	1	**PRBS7**Pattern Enable
UI_PATTERN_PRBS9	0 or 1	1	**PRBS9**Pattern Enable
UI_PATTERN_PRBS23	0 or 1	1	**PRBS23**Pattern Enable
UI_PATTERN_PRBS31	0 or 1	1	**PRBS31**Pattern Enable
UI_NUMBER_OF_LANES	1-4	1	**Number of lanes**Number of lanes this IP core has enabled.
UI_DATA_RATE	250 – 10000	5000	**Transceiver data rate**Supported rates:• 250 Mbps• 1000 Mbps• 1250 Mbps• 2500 Mbps• 3125 Mbps• 5000 Mbps• 6250 Mbps• 8000 Mbps• 10000 Mbps• 10312.5 Mbps
UI_TX_CLK_DIV_FACTOR	1, 2, 4, 8 & 11	1	**TX clock division factor**
UI_CDR_REFERENCE_CLK_SOURCE	Dedicated or Fabric	Fabric	**CDR reference clock source**

……..continued			
Name	**Range**	**Default**	**Description**
UI_CDR_REFERENCE_CLK_FREQ	0-312.5	125	**CDR reference clock frequency**Supported frequencies:• 25.00 MHz• 31.25 MHz• 50.00 MHz• 62.50 MHz• 75.00 MHz• 100.00 MHz• 125.00 MHz• 150.00 MHz• 156.25 MHz• 312.50 MHz

I/O Signals

The following table describes the port signals for CoreSmartBERT.

Note: In the and following tables, n represents a range of 0 to 3 depending on the number of configured lanes.

Table 3-2. CoreSmartBERT I/O Signal Descriptions

Name	Width	Direction	Description
SYS_RESET_N	1	Input	Active low system reset
LANE[n]_CDR_REF_CLK_FAB	1	Input	CDR reference clock from fabric, only exposed when **Fabric** is selected as CDR reference clock source.
LANE[n]_CDR_REF_CLK_0	1	Input	CDR reference clock from dedicated pin, only exposed when**Dedicated** is selected as CDR reference clock source.
LANE[n]_TX_BIT_CLK_0	1	Input	Tx Bit Clock
LANE[n]_TX_PLL_REF_CLK_0	1	Input	PLL Reference Clock
LANE[n]_TX_PLL_LOCK_0	1	Input	PLL Lock

Table 3-3. CoreSmartBERT PAD Signal Descriptions

Name	Direction	Description
LANE[n]_TXD_P	Output	Transmitter Serial Data
LANE[n]_TXD_N	Output	
LANE[n]_RXD_P	Input	Receiver Serial Data
Lane[n]_RXD_N	Input	

Tool Flows

This section discusses various tool flow related information.

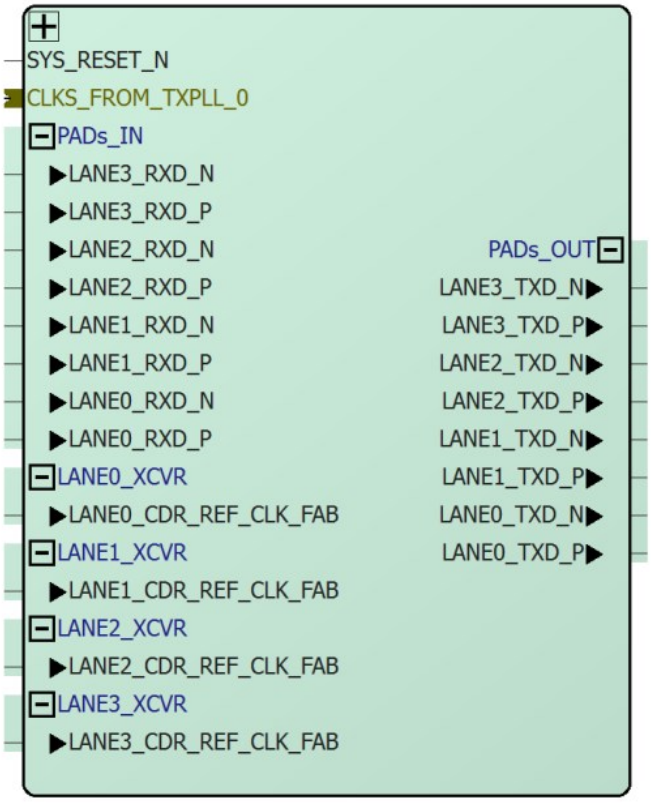
Licensing
CoreSmartBERT does not require any license.

RTL
Complete RTL source code is provided for free with any Libero license.

SmartDesign
CoreSmartBERT is available for download to the SmartDesign IP catalog through the Libero SOC web repository. To know how to create SmartDesign project, see SmartDesign User Guide.

The following figure shows an example of an instantiated view of CoreSmartBERT on the SmartDesign canvas.

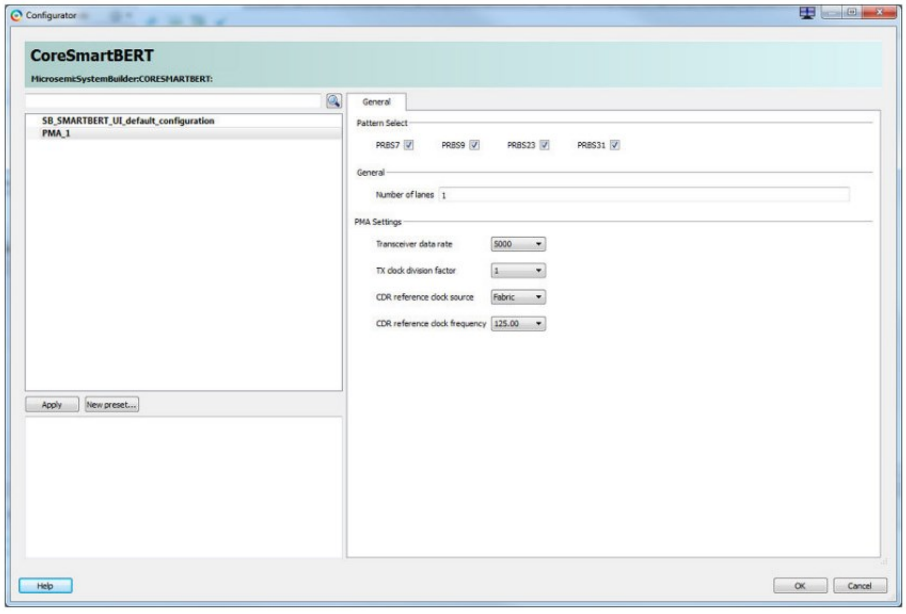
Figure 4-1. Instantiation of CoreSmartBERT on SmartDesign Canvas



Configuring the CoreSmartBERT

The following figures shows how the core instance can be configured using its configuration GUI.

Figure 4-2. CoreSmartBERT SmartDesign Configuration GUI



Synthesising in Libero SoC

To run synthesis with the configuration selected in the configuration GUI, perform the following steps:

1. Set the design root appropriately.
2. Under Implement Design, in the Design Flow tab, right-click Synthesize, and then click Run.

Running Place-and-Route in Libero SoC

To run the place and route, perform the following step:

- On the Design Flow tab, select Implement Design, right-click Place and Route, and then from the context menu, select Run.

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	07/2022	The following is the list of changes in revision A of the document:• The document was migrated to the Microchip template• Updated for CoreSmartBERT v2.9• The document number was updated to DS50003362A from 50200788
9.0	03/2021	Updated for CoreSmartBERT v2.8.
8.0	06/2020	Updated for CoreSmartBERT v2.7.
7.0	03/2020	Updated for CoreSmartBERT v2.6.
6.0	08/2019	Updated for CoreSmartBERT v2.5.
5.0	03/2019	Updated for CoreSmartBERT v2.4.
4.0	12/2018	Updated for CoreSmartBERT v2.3.
3.0	08/2018	Updated for CoreSmartBERT v2.2.
2.0	05/2018	Updated for CoreSmartBERT v2.1.
1.0	08/2017	Initial release.

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