MICROCHIP CAN-CN FPGA PolarFire FPGA Module User Manual

CAN-CN FPGA: PolarFire PCIe L2P2 Link State Support
Microchip Corporation
Subject: CAN-CN FPGA: PolarFire PCI Express L2P2 link state support

Contents

Description:

In Libero SoC release 2022.1 the option to enable the L2P2 power management link has been removed from the Generate SERDES Initialization GUI. All PolarFire transceiver PCIe Link Training and Status State Machine (LTSSM) hardware blocks do not support the L2P2 power management link state.

Reason For Change:

PolarFire transceiver blocks include embedded PCIe Gen1 and Gen2 Root-port and End-point controllers. The PCIe Sub-system (PCIESS) LTSSM supports Link Training states and Re-Training (Recovery) state. However, the

PCIESS does not support any software driven power management states such as L2P2, as incorrectly noted in the original documentation.

- Software-driven L2P2 entry commands issued by the PolarFire PCIESS Root-Port to the downstream end-points are not supported. As a root-port, this will cause the link to be completely disrupted and only recoverable by re-initializing the link with side-band PERSTn (fundamental reset) or a power cycle.
- PolarFire PCIESS End-point should not be commanded by the host to enter L2P2 link state. As an end-point, the link may be disruptive and only recoverable by re-initializing the link with side-band PERSTn (fundamental reset) or a power cycle.

Application Impact:

PolarFire devices do not support L2P2 power management link state.

- To avoid link disruptions, PCIe power management software must not command a PolarFire PCIESS Root-port or End-point to enter a lower-power link state (L2).
- It does not achieve further operational power-savings for the PolarFire device.
- Libero SoC release 2022.1 was updated to advertise disabled D3hot and D3cold in PCI Legacy Power Management state ofour Endpoint Config Space
- To achieve further operational power savings, on top of the already power-optimized PolarFire device architecture, the FPGA designer should employ power management techniques directly to the FPGA fabric design.

Action Required:

- Users should reference updated documentation provided by Microchip concerning PCIESS link Training State support..
- **https://www.microsemi.com/document-portal/doc_download/1245812-polarfire-fpga-and-polarfire-soc-fpga-pci-expressuser-guide**
- Refer to the PolarFire FPGA Low Power Application Note for device features that users can employ to build additional power-savings into their design.

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https://www.microsemi.com/document-portal/doc_download/1244032-ac485-polarfire-fpga-low-powerapplication-note

Contact Information:

If you have any questions about this subject, contact the FPGA-BU Technical Support at the web portal below
http://www.microchip.com/support

Regards,
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Documents / Resources

	MICROCHIP CAN-CN FPGA PolarFire FPGA Module [pdf] User Manual CAN-CN FPGA PolarFire FPGA Module, CAN-CN FPGA, PolarFire FPGA Module, Module

References

- Microsemi | Semiconductor & System Solutions | Power Matters
- polarfire_AN485_low_power.pdf
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- microsemi.com/document-portal/doc_download/1245812-polarfire-fpga-and-polarfire-soc-fpga-pci-express-user-guide