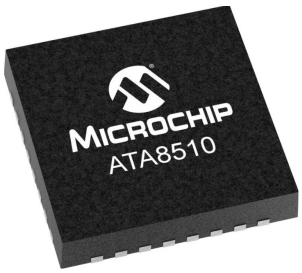

MICROCHIP ATA8510 Serial Peripheral Interface Command Sheet User Guide

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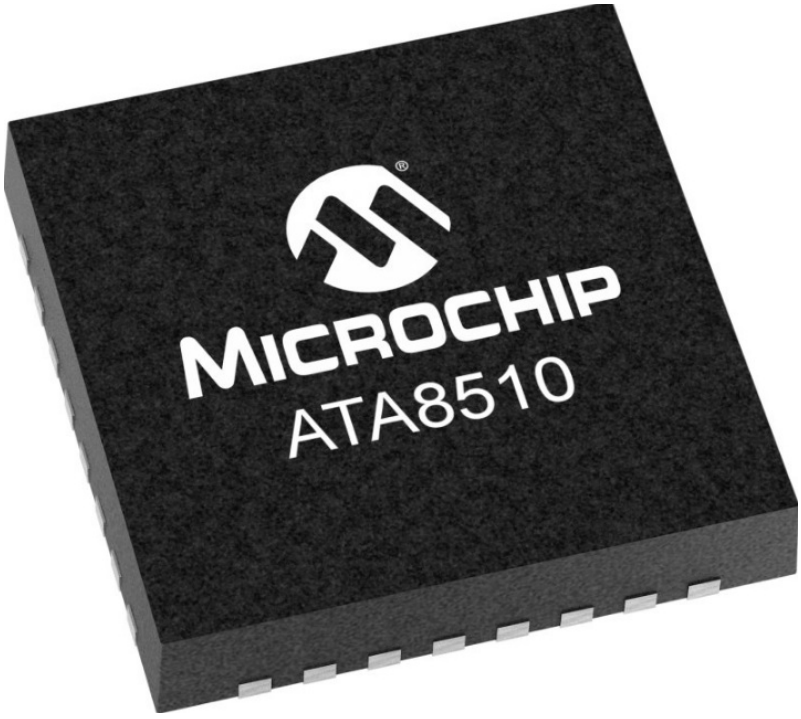


Contents

Introduction

This user guide provides a summary of all Serial Peripheral Interface (SPI) commands available with the ATA8510 Ultra High Frequency (UHF) product family, including a detailed command description, the setup procedure, command coding, and descriptions of the available parameters. This document also includes the SPI timing calculation, which helps to ensure proper timing in the application. This document is applicable for the following products:

- ATA8510
- ATA8515
- ATA8210
- ATA8215
- ATA8710

Quick References

Reference Documentation

For further details, refer to the ATA8510/15 Industrial User's Guide (DS50003142).

Acronyms and Abbreviations

Table 1-1. Acronyms and Abbreviations

Acronyms/Abbreviations	Description
EEPROM	Electrically Erasable Programmable Read-only Memory
FIFO	First-In First-Out
FW	Firmware
IRQ	Interrupt Request
ROM	Read-only Memory
RSSI	Received Signal Strength Indicator
RX	Receiver
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SCK	Serial Clock
SFIFO	Support First In First Out
TX	Transmitter
uC	Microcontroller
UHF	Ultra High Frequency

SPI Commands Overview

Figure 2-1. SPI Commands

Read Fill Level RX FIFO

Host uC
ATA8510

CMD [0x01]	0x00	0x00
events.system	events.events	data

Requested information
System status
Not used from FW

Read Fill Level TX FIFO

Host uC
ATA8510

CMD [0x02]	0x00	0x00
events.system	events.events	data

Get Event Bytes

Host uC
ATA8510

events.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
system	SYS_ERR	CMD_RDY	SYS_RDY	AVCCLOW	LOWBATT	SFIFO	DFIFO_RX	DFIFO_TX
events	IDCHKA	WCOKA	SOTA	EOTA	IDCHKB	WCOKB	SOTB	EOTB
power	PWRON	–	NPWRON6	NPWRON5	NPWRON4	NPWRON3	NPWRON2	NPWRON1
config	PathB	PathA	ch[1:0]		–	ser[2:0]		

Read RSSI FIFO

Host uC
ATA8510

CMD [0x05]	length	0x00	0x00	…	0x00		This co (length
events.system	events.events	dummy	data	…	data		

Read RX FIFO

Host uC
ATA8510

CMD [0x06]	length	0x00	0x00	…	0x00		This co (length
events.system	events.events	dummy	data	…	data		

Read RX FIFO

Host uC
ATA8510

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
serviceChannelConfig	enaPathB	enaPathA	channel[1:0]		–	service[2:0]		

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
serviceChannelConfig	–	–	–	–	startPollingIndex			

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
tuneCheckConfig	EN_ANT_TUNE	EN_TEMP_MEAS	EN_SRCCAL	EN_FRCCAL	EN_VCOCAL	–	EN_SELFCHECK	–

CMD [0x12]	0x00	0x00
events.system	events.events	rom version

The increment mechanism needs to be performed as followed to ensure that the right data will be provided:
Parameter at byte n-x [x>=2] = 0x01
Parameter at byte n-y [y<=1] = 0x00
[n = number of bytes transmitted via SPI]

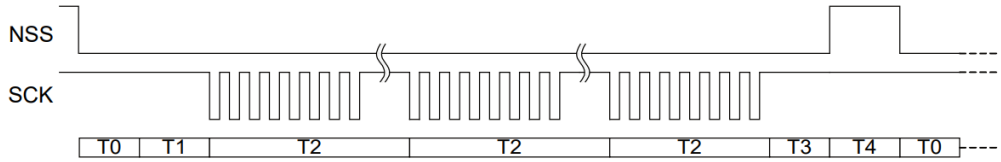
CMD [0x17]	value
events.system	events.events

0x00	disable
0x01	2.0V
0x02	2.1V
0x03	2.2V
0x04	2.3V
0x05	2.4V
0x06	2.5V
0x07	2.6V

0x08	2.7V
0x09	2.8V
0x0A	2.9V
0x0B	3.0V
0x0C	3.1V
0x0D	3.2V
0x0E	3.3V
0x0F	3.4V

SPI Timing Calculation

Figure 3-1. SPI Timing Calculation



Time	Timing at 40% interrrupt usage	Description	Depend on	Timing
T0	0 or 25 µs	Time from NSS LOW to AVRactive sleep mode is enabled	0 µs if no sleep mode is used or25 µs for any sleep mode	25 µs
T1	17.6 µs	Time from AVR active tobeginning of first telegram byte	INT1 IRQ (falling edge)	45 cycles (ISR) + 15 cyclesinterrupt response time
T2	16 µs	Time to shift in one SPI-bytewith f_SCK	f_SCK at 500 kHz (maximum)	8 bit / 500 kbit/s
T3	35.1 µs	Time to handle last byte	SPI RX/TX buffer IRQ Note:Depends on SPI command	max. 120 cycles (*2)
T4	16.1 µs	SPI idle time telegram	INT1 IRQ (rising edge)	40 cycles (ISR) + 15 cyclesinterrupt response time

Timing calculation done with AVR core clock of 5.7 MHz
*2) needed for SPI command “Read RX Buffer” and “Read RSSI Buffer”

Read Fill Level RX FIFO	0
Read Fill Level TX FIFO	0
Read Fill Level RSSI FIFO	0
Get Event Bytes	0
Read RSSI FIFO	120
Read RX FIFO	120
Write SRAM Register	110
Read SRAM Register	120
Write EEPROM	55
Read EEPROM	0
Write TX FIFO	110
Write TX Preamble FIFO	110
Set System Mode	55
Calibrate and Check	50
Patch SPI	XX

Get Version ROM	0
Get Version Flash	0
Customer Configurable Commmand	XX
System Reset	0
Trigger EEPROM Secure Write	65
Set Voltage Monitor	85
OFF Command	0
Read Temperature Value	0
Init SRAM Service	50
Start RSSI Measurement	55
Get RSSI Value	0
Read RX FIFO Byte Interrupt	70
Read RSSI FIFO Byte Interrupt	70

Document Revision HistorY

Revision	Date	Section	Description
A	12/2021	Document	Initial release

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