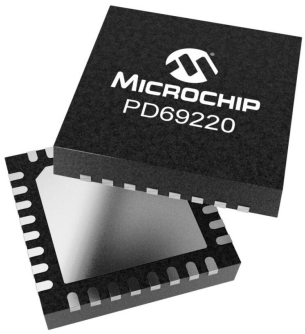

MICROCHIP AN4323 PD69200 to PD69220 Conversion Owner's Manual

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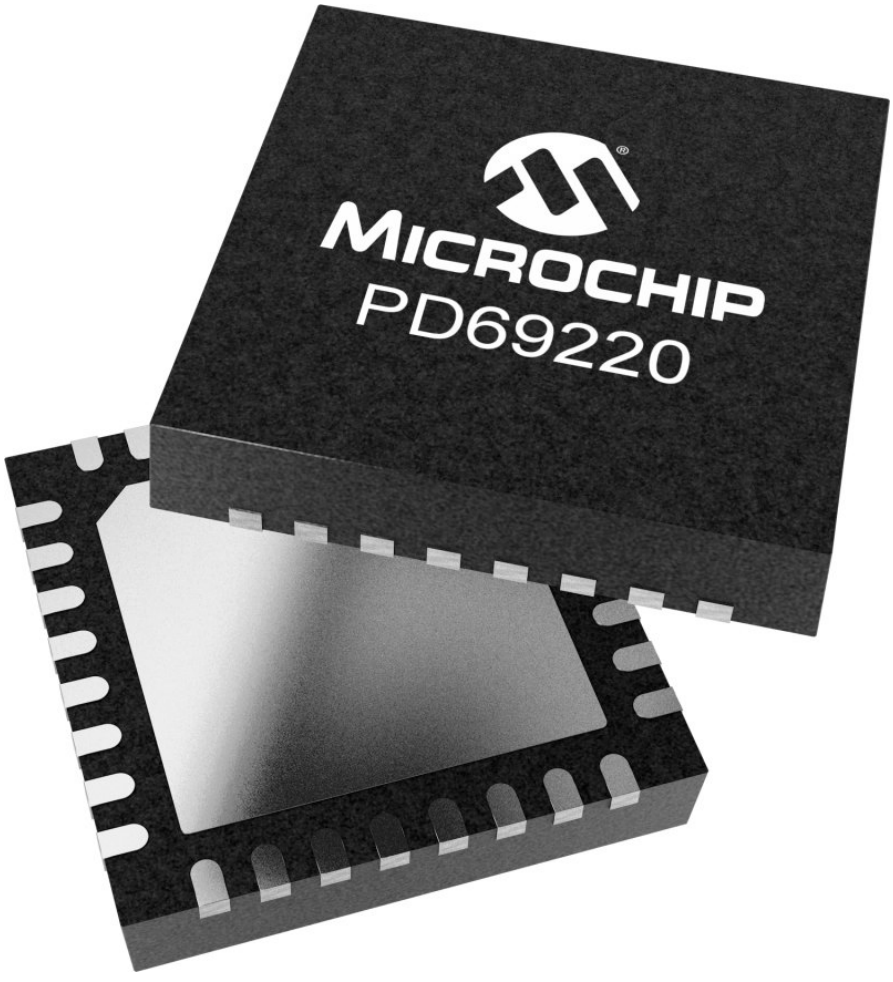


Contents

Introduction

This application note provides guidelines for using the PD69220 device on a Printed Circuit Board (PCB) that was designed for the PD69200 device. The following aspects must be considered:

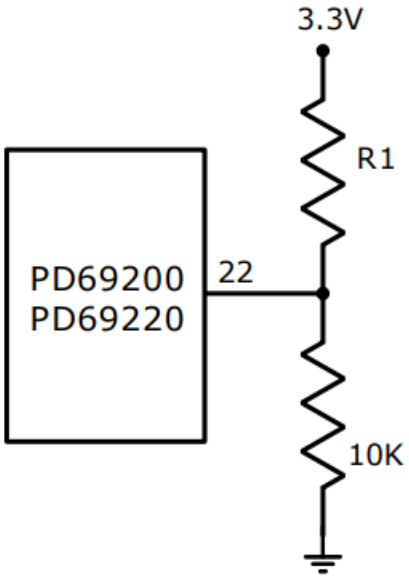
- Host–PoE controller communication management
  - UART or I2C address selection
- PCB footprint
  - Solder paste mask

    Using the 16-byte communication protocol, this application note also defines a method to determine which PoE controller (PD69200 or PD69220) is installed on a switch.

Host–PoE Controller Communication Management

The following figure and table show that UART (set to 19200 bps) or I2C (up to 400 KHz) communication between the host CPU and PoE controllers are managed by setting the PD69220/PD69220 address pin number 22 (I2C_ADDR)

Figure 1-1. PD69200/PD69220 Communication Management



The following table lists the specific value of R to choose UART or I2C and to set the address.

Table 1-1. Serial Communication Configuration

I2C Address Hexadecimal	**R1–KΩ (1%)**	
	PD69200	**PD69220**
UART	N.C.	N.C.
0x4	97.6	147
0x8	53.6	86.6
0xC	35.7	57.6
0x10	25.5	43.2
0x14	19.1	34
0x18	14.7	26.7
0x1C	11.3	22.1
0x20	8.87	18.2
0x24	6.81	15.4
0x28	5.23	13
0x2C	3.92	11
0x30	2.80	9.31
0x34	1.87	7.87
0x38	1.02	6.49
0x3C	0.324	5.49

Note: All other parameters of resistor R1 (size, power, footprint, and so on) are the same in all the controllers, except in the value.

PD69200 QFN vs. PD69220 LGA Package

The PD69200 device is packaged in a 32 pin 5 mm × 5 mm QFN package and the PD69220 device is packaged in a 32 pin 5 mm × 5 mm LGA. The pinout of the two devices are identical. However, there are physical differences in

the thermal pad and pins. Additionally, there are differences in the physical package construction of the QFN vs. LGA. Due to these differences, while using the PD69220 device on a PCB that was designed for the PD69200, the paste mask or stencil must be optimized for use with the PD69220 device.

Section **3. PCB Footprint** gives recommendations for a revised stencil for PD69220, if the original PCB used the footprint for PD69200 that was recommended in the PD69200 data sheet. If the footprint in the PD69200 data sheet is not used, follow the general principles outlined in section **3. PCB Footprint** to optimize the stencil based on the footprint that was used.

See the *PD69220 Data Sheet* for a footprint recommendation if the design is a new PCB that was designed for the PD69220 unit.

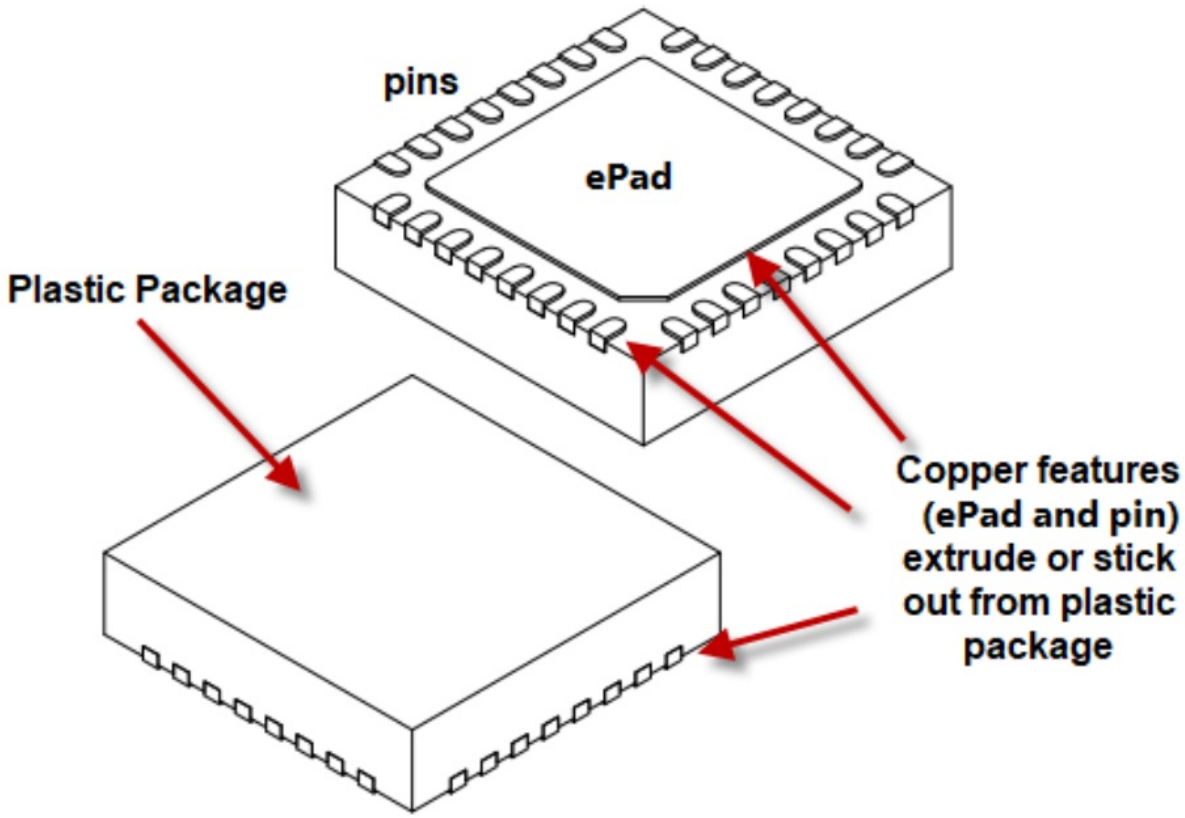
Package Construction

This section provides a general overview of the physical differences between the PD69200 QFN and the PD69220 LGA

PD69200 QFN

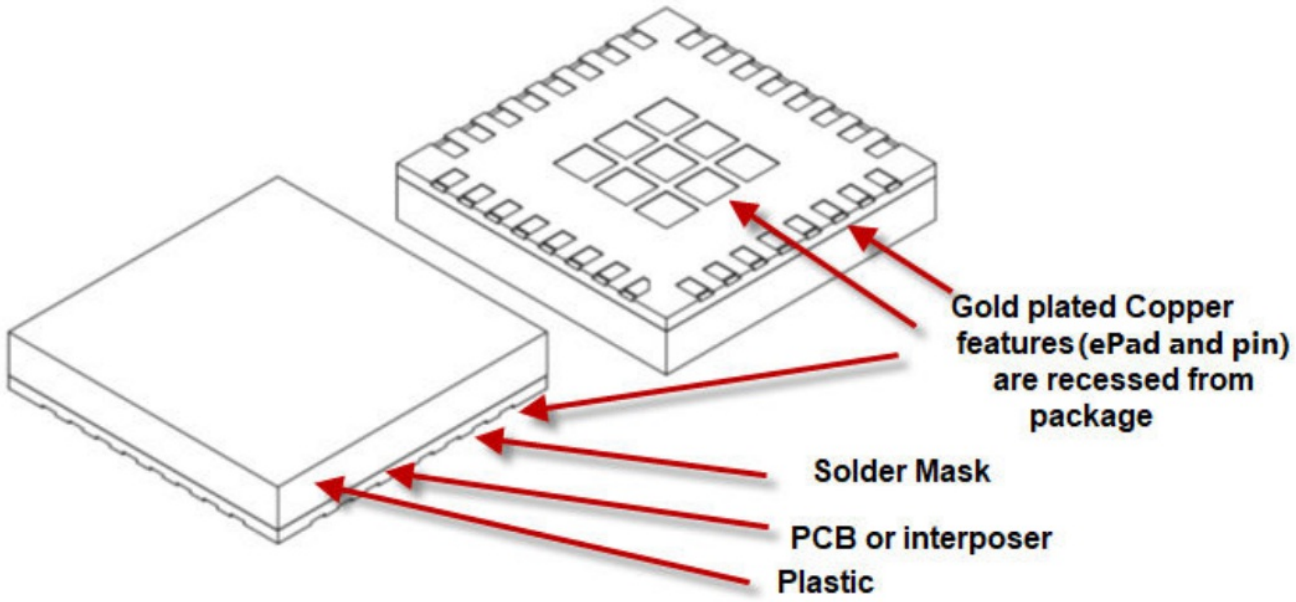
The PD69200 physical silicon die is mounted directed on a copper lead frame. The IC and lead frame are encapsulated in plastic. In this case, the bottom surface is plastic and the ePad and copper pin features extrude (stick out) from the plastic surface by the dimension A1 (a maximum of 0.05 mm). See the following figure.

Figure 2-1. PD69200 QFN Construction



PD69220 LGA

To make the PD69220 pinout identical to PD69200, an interposer or “small PCB” is used in the package construction. The PD69220 physical silicon die is mounted onto the interposer. The interposer routes to the package pins in such
a manner that the pinout between PD69200 and PD69220 is identical. The interposer and die are encapsulated in plastic. The bottom surface of the package is the solder mask associated with the interposer.
Due to this construction, the ePad and pins, rather than extruding from the package surface, are actually recessed into the package surface (like a cave) by the thickness of the solder mask.
The ePad and pins are copper electroplated with nickel-gold.
See the following figure



ePad

Figure 2-1 and Figure 2-2 show the difference in the ePad construction. The PD69220 ePad is a single 3.5 mm × 3.5 mm square, whereas ePads in the PD69200 device are nine 0.6 mm × 0.6 mm squares.
The nine squares are electrically connected to each other.

Pins

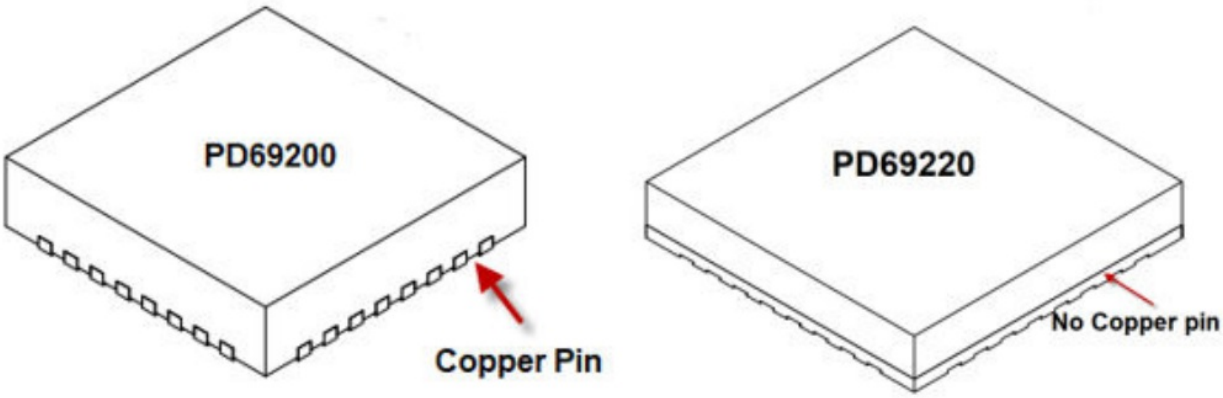
The following table lists the dimensions for PD69200 and PD69220 pins.

Table 2-1. Pin Dimensions

Device	Dimension	Minimum (mm)	Nom (mm)	Maximum (mm)
PD69200	Length (L)	0.30	0.40	0.50
	Width (b)	0.18	0.25	0.30
PD69220	Length (L)	0.30	0.35	0.40
	Width (b)	0.20	0.25	0.30

Wettable Flanks

There is no copper on PD69220 package side and it does not have a wettable flank. While the PD69200 unit does have a copper feature on the package side, no effort is taken to prevent oxidation. Therefore, this package is also considered to not have a wettable flank.
See the following figure



PCB Footprint

Microchip has provided a recommended footprint for PD69220 in the device datasheet and in this document. These recommendations apply when the Microchip recommended footprint for PD69200 is used on the PCB and the customer is mounting a PD69220 using the footprint designed for the PD69200 device.

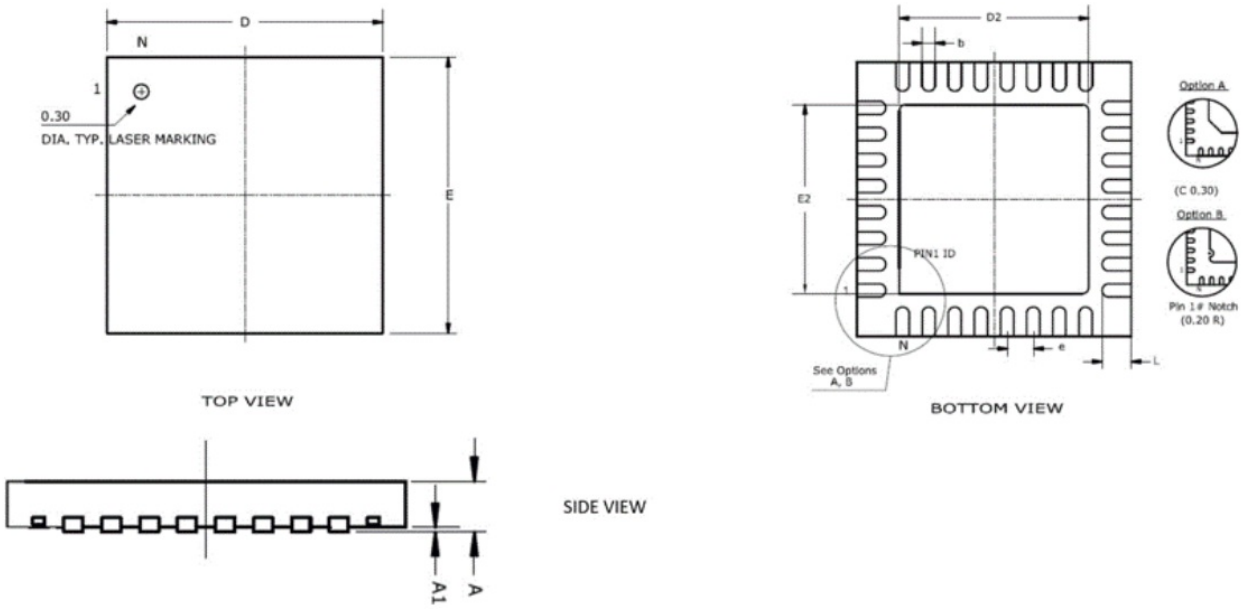
If the customer has used an alternate footprint for the PD69200 device, then the general principles discussed must be applied to develop an optimized stencil based on the actual PD69200 footprint used

PD69200 Package Outline Drawing

The following figure shows the package outline drawing of the PD69200 device.

Note: For the most current package drawings, see the Microchip Packaging Specification located at www.microchip.com/packaging

Figure 3-1. PD69200 Package Outline Drawing (32 Pin QFN 5 mm × 5 mm)



The following table lists the dimensions and measurements of the PD69200 package.

Table 3-1. PD69200 Package Outline Dimensions and Measurements

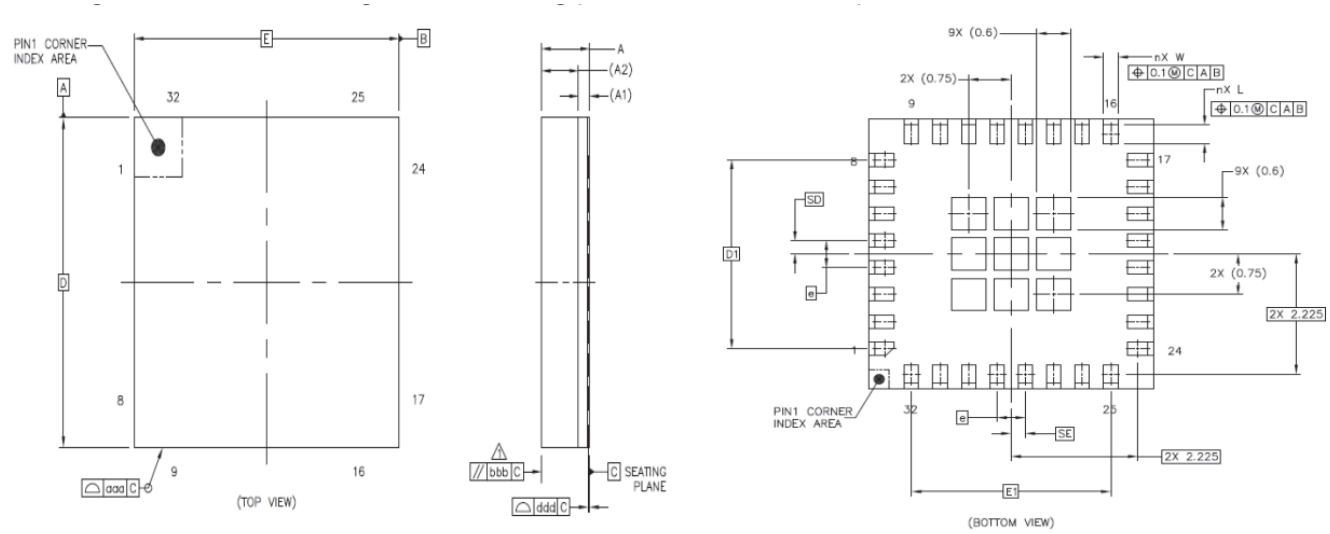
Dimension	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
e	0.50 BSC	—	0.02 BSC	—
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	3.50	3.70	0.138	0.147
E2	3.50	3.70	0.138	0.147
D	5.00 BSC	—	0.197 BSC	—
E	5.00 BSC	—	0.197 BSC	—

PD69220 Package Outline Drawing

The following figure shows the package outline drawing of the PD69220 device.

Note: For the most current package drawings, see the Microchip Packaging Specification located at www.microchip.com/packaging

Figure 3-2. PD69220 Package Outline Drawing (32-Pin LGA 5 mm × 5 mm)



The following table lists the dimensions and measurements of the PD69220 package.

Dimension	Millimeters		
	Min.	Typ.	Max.
A	—	—	1
A1	—	0.21	—
A2	—	0.7	—
D	—	5	—
E	—	5	—
W	0.2	0.25	0.3
L	0.30	0.35	0.4
e	—	0.5	—
n	—	32	—
D1	—	3.5	—
E1	—	3.5	—
SD	—	0.25	—
SE	—	0.25	—

Recommended PCB Layout

The following figures show the recommended PCB layout patterns for the 32-pin QFN 5 mm × 5 mm PD69200 and the change to the stencil required for the 32-pin LGA 5 mm × 5 mm PD69220, to use this footprint. Units are in millimeters.

Figure 3-3. PD69200 Solder Mask

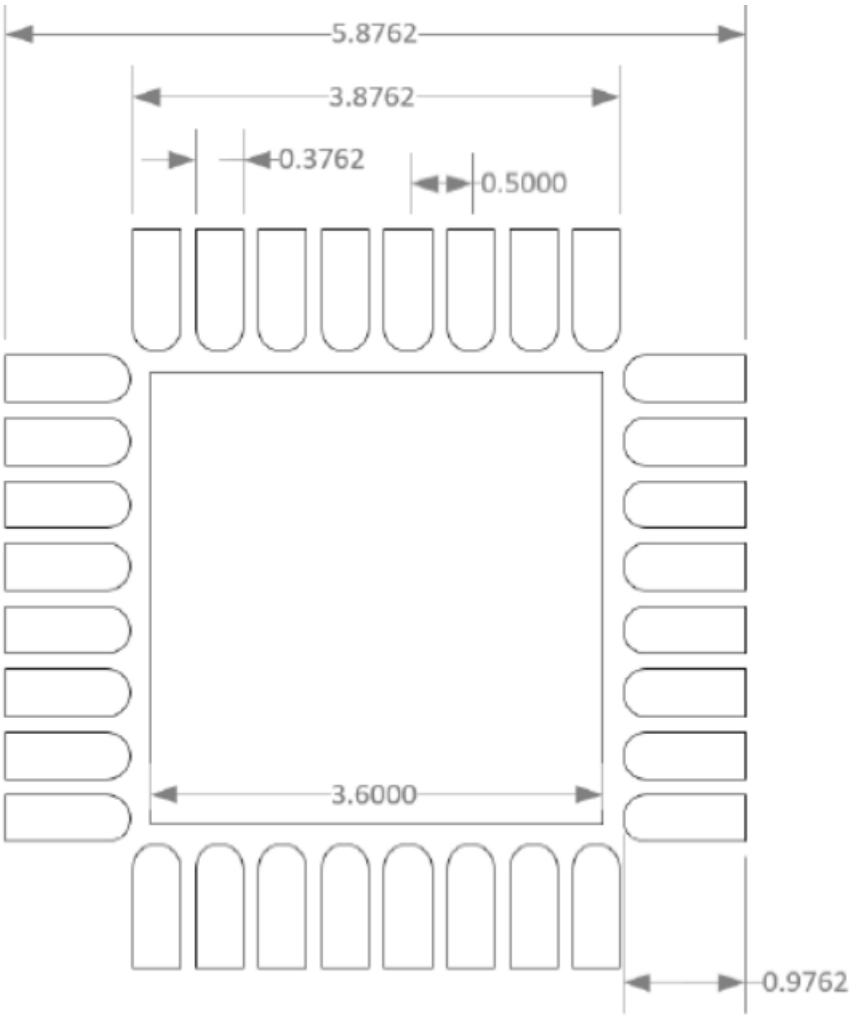
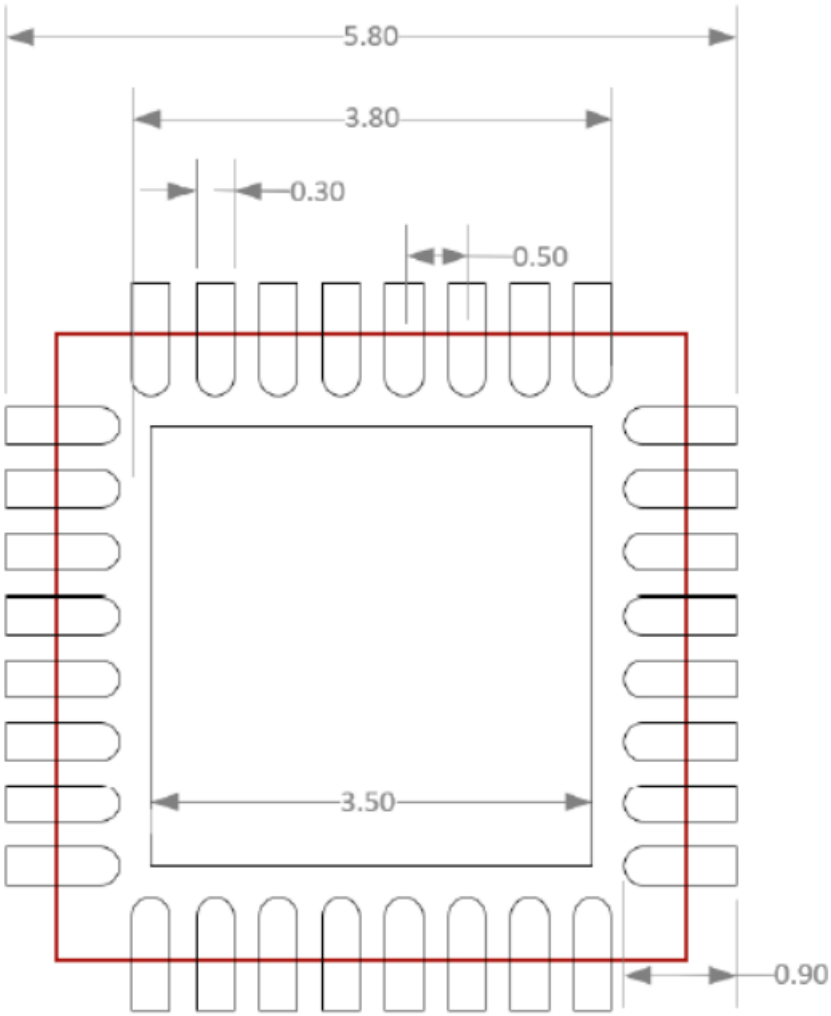


Figure 3-4. PD69200 Top-Layer Copper


5.80
3.80
0.30
0.50
3.50
0.90

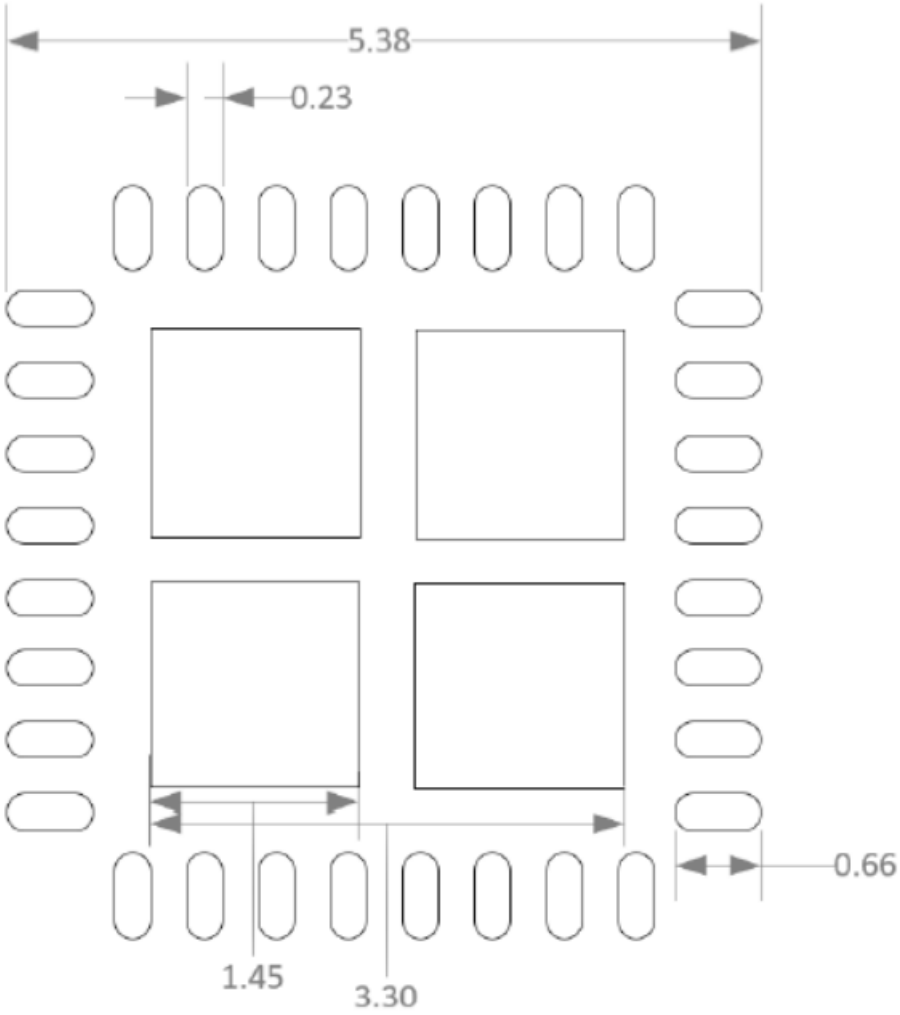
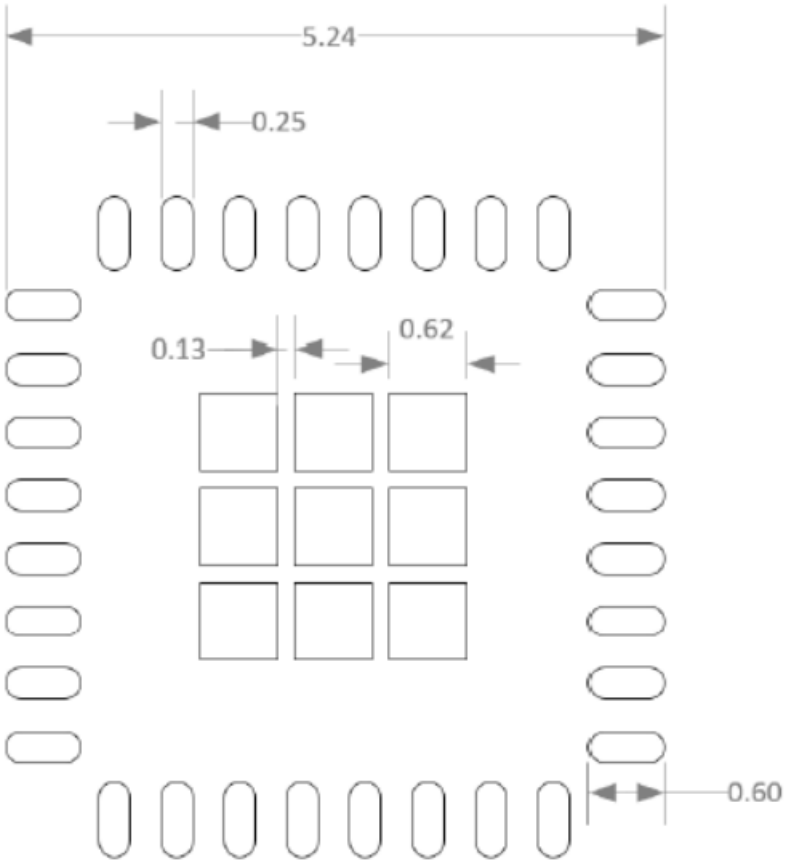


Figure 3-6. PD69220 Paste Mask



Identification of PoE Controller

This section describes how to determine if PD69200 or PD69220 is installed on a switch. There are two cases to consider:

- Under normal operation where valid firmware is installed
- Under a fault condition where the firmware installed in the controller has become corrupted

Under Normal Operation

In order to identify which PoE controller is assembled, execute the command “Get Software Version”, as described in section 4.1.19 of the *PD692x0 Communication Protocol User Guide* or section 3.1.17 of the *PD692x0 BT Serial Communication Protocol User Guide*. These documents can be found in the **Microchip Software Library**.

The response from the PoE controller includes the Prod#, which indicates the PoE controller type.

Table 4-1. Get Software Version

In order to identify which PoE controller is assembled, execute the command “Get Software Version”, as described in section 4.1.19 of the *PD692x0 Communication Protocol User Guide* or section 3.1.17 of the *PD692x0 BT Serial Communication Protocol User Guide*. These documents can be found in the **Microchip Software Library**.

The response from the PoE controller includes the Prod#, which indicates the PoE controller type.

Table 4-1. Get Software Version

[0] KEY	**[1] ECHO**	**[2] SUB**	**[3] SUB1**	**[4] SUB2**	**[5] DATA**	**[6] DATA**	**[7] DATA**	**[8] DATA**	**[9] DATA**	**[10] DATA**	**[11] DATA**	**[12] DATA**
0x02	##	0x07	0x1E	0x21	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Request	—	Global	Version	SW Version	N	N	N	N	N	N	N	N
0x03	##	Val	0x4E	Val	Val		Val	Val	Val		Val	
Telemetry	—	HW Version	N	**Prod#**	SW_Version		Param #	Build #	Internal SW #		0x0000	

Table 4-2. Product Number

Product Number (Decimal)	**PoE Controller Type**
22	PD69200 programmed with IEEE® 802.3at firmware
24	PD69200 programmed with IEEE 802.3bt firmware
27	PD69210 programmed with IEEE 802.3at firmware
26	PD69210 programmed with IEEE 802.3bt firmware
28	PD69220 programmed with IEEE 802.3at firmware
29	PD69220 programmed with IEEE 802.3bt firmware

Under a Fault Condition

Use the following procedure to identify which PoE controller is installed on a PCB in the case of a fault condition when the firmware is corrupted.

When CPU_Status1_Err field reports on firmware error (bit 1 = ‘1’), the telemetry structure changes to the following.

Table 4-3. Telemetry at Bootup Error

[0] KEY	[1] ECHO	[2] SUB	[3] SUB 1	[4] SUB 2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x03	0xFF	Val	0x4E	0x4E	Val	Val	Val	Val	0x4E	0x4E	0x4E	0x4E
Telemetry	—	CPU Status1 Err	N	N	**Err Code**	**Err Info1**	**Err Info2**	**Download Type**	N	N	N	N

The following table lists the fields description in case of an error.

Table 4-4. Error Type

Err Name	Err Code	Err Info1	Err Info2	Download Type
Need Download **PD69200**	0x4E	0x4E	0x4E	0x4E
Need Download **PD69210/220**	0x4E	0x4E	0x4E	0x33
HW error **Try to program PD69210 or PD69220 with PD69200 firmware**	0x02	CPU Type Boot 0x33	CPU Type App 0x2C	0x33
HW error **Try to program PD69200 with PD69210 or PD69220 firmware**	0x02	CPU Type Boot 0x2C	CPU Type App 0x33	0x4E
Sys Type error from APP **Try to program PD69210 with PD69220 firmware**	0x03	Boot Sys Type 0x40	App Sys Type 0x41	0x4E
Sys Type error from APP **Try to program PD69220 with PD69210 firmware**	0x03	Boot Sys Type 0x41	App Sys Type 0x40	0x4E

Revision History

Revision	Date	Description
C	07/2022	The following is the summary of changes made in this revision : • Added the following sections: ◦ 2. PD69200 QFN vs. PD69220 LGA Package ◦ 2.1. Package Construction ◦ 2.1.1. PD69200 QFN ◦ 2.1.2. PD69220 LGA ◦ 2.2. ePad ◦ 2.3. Pins ◦ 2.4. Wettable Flanks • Edited ◦ 3. PCB Footprint ◦ 3.2. PD69220 Package Outline Drawing ◦ 3.3. Recommended PCB Layout ◦ Removed tables System Type and MCU type from • 4.2. Under a Fault Condition
B	06/2022	• Added section Identification of PoE Controller, which des cribes how to determine which PoE controller (PD69200 or PD69220) is installed on a switch.
A	12/2021	Initial Revision

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