MICROCHIP AN4229 Risc V Processor Subsystem User Guide

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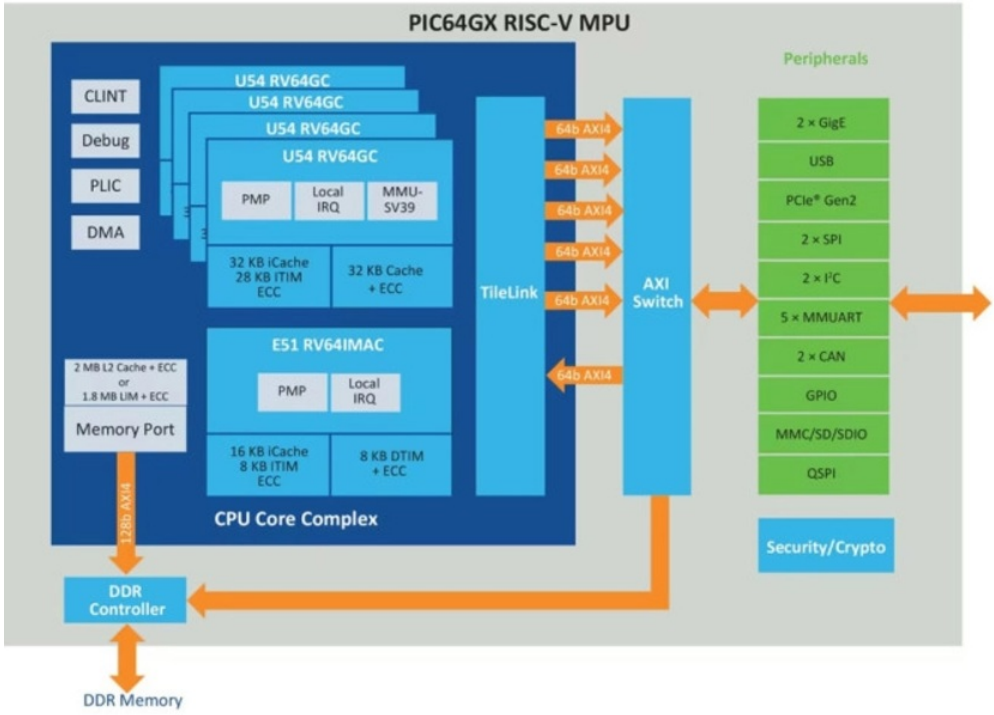


Product Information

Specifications

- Product Name: RT PolarFire
- Model: AN4229
- Processor Subsystem: RISC-V
- Power Requirements: 12V/5A AC power adapter
- Interface: USB 2.0 A to mini-B, Micro B USB 2.0

Product Usage Instructions

Design Requirements

The hardware and software requirements for building a Mi-V processor subsystem are as follows:

- 12V/5A AC power adapter and cord
- USB 2.0 A to mini-B cable
- Micro B USB 2.0 cable
- Refer to the readme.txt file in the design files for all software versions needed

Design Prerequisites

Before starting the design process, ensure the following steps are performed:

- [List of prerequisites]

Design Description

MIV_RV32 is a processor core designed to implement the RISC-V instruction set. The core can be implemented on an FPGA.

FAQ

- **Q: What are the hardware requirements for RT PolarFire?**
  A: The hardware requirements include a 12V/5A AC power adapter and cord, USB 2.0 A to mini-B cable, and Micro B USB 2.0 cable.
- **Q: What is the processor subsystem of RT PolarFire?**
  A: The processor subsystem is based on the RISC-V architecture.

Introduction (Ask a Question)

Microchip offers the Mi-V processor IP and software toolchain at no cost to develop RISC-V processor based designs. RISC-V is a standard open Instruction Set Architecture (ISA) under the governance of the RISC-V foundation. It offers numerous benefits, which include enabling the open-source community to test and improve cores at a faster pace than closed ISAs. RT PolarFire® Field Programmable Gate Array (FPGAs) support Mi-V soft processors to run user applications. This application note describes how to build a Mi-V processor subsystem to execute a user application from the designated TCM memory initialized from the SPI Flash.

Design Requirements (Ask a Question)
The following table lists the hardware and software requirements for building a Mi-V processor subsystem.

Table 1-1. Design Requirements

Requirement	Description
Hardware Requirements	
RT PolarFire® Development Kit (RTPF500TS-1 CG1509M) 12V/5A AC power adapter and cord USB 2.0 A to mini-B cable Micro B USB 2.0 cabl e	REV 1.0
Software Requirements	
Libero® SoC FlashPro Express SoftConsole	See the readme.txt file in the design files for all software versions needed to create the Mi-V reference design

Design Prerequisites (Ask a Question)

Before you start, perform the following steps:

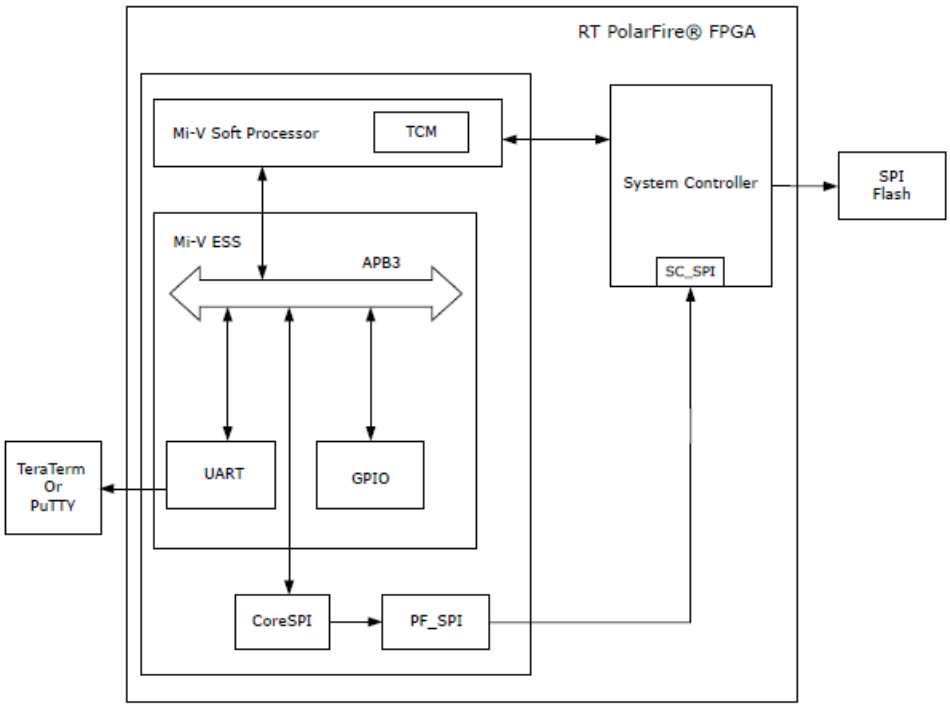
1. Download the reference design files from RT PolarFire: Building RISC-V Processer Subsystem.
2. Download and install Libero® SoC from the following link: Libero SoC v2024.1 or later.

Design Description (Ask a Question)

MIV_RV32 is a processor core designed to implement the RISC-V instruction set. The core can be configured to have AHB, APB3, and AXI3/4 bus interfaces for peripheral and memory accesses. The following figure shows the top-level block diagram of the Mi-V subsystem built on RT PolarFire® FPGA.

The user application to be executed on Mi-V processor can be stored in an external SPI Flash. At device power-up, the system controller initializes the designated TCM with the user application. The system Reset is released after the TCM initialization is completed. If the user application is stored in SPI Flash, the System Controller uses the SC_SPI interface for reading the user application from SPI Flash. The given user application prints the UART message “Hello World!” and blinks user LEDs on the board.

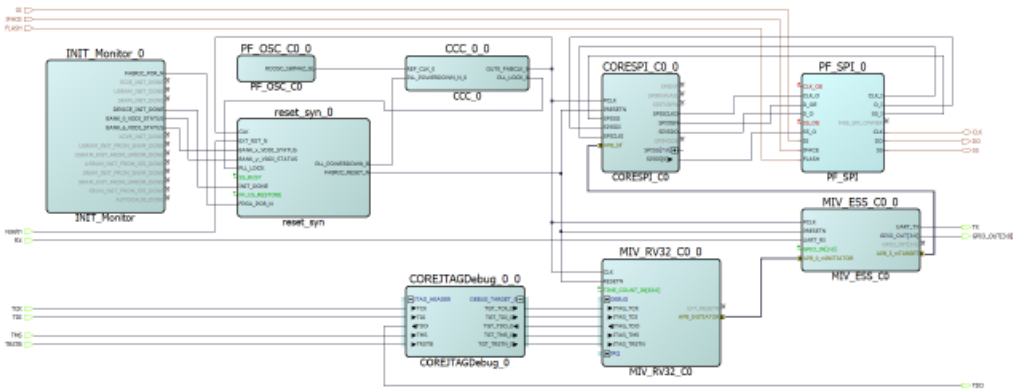
Figure 3-1. Block Diagram



Hardware Implementation (Ask a Question)

The following figure shows the Libero design of the Mi-V processor subsystem.

Figure 4-1. Mi-V Processor Subsystem



IP Blocks (Ask a Question)

The following table lists the IP blocks used in the Mi-V processor subsystem reference design and their function.

Table 4-1. IP Blocks Description

IP Name	Description
INIT_MONITOR	The RT PolarFire® Initialization Monitor gets the status of device and memory initialization
reset_syn	This is the CORERESET_PF IP instantiation which ge nerates a system-level synchronous Reset for the Mi-V subsystem
CCC_0	The RT PolarFire Clock Conditioning Circuitry (CCC) b lock takes an input clock of 160 MHz from the PF_OSC block and generates a 83.33 MHz fabric clock for the Mi-V processor subsystem and other peripherals.
MIV_RV32_C0 (Mi-V Soft Processor IP)	The Mi-V soft processor default Reset Vector Address value is 0×8000_0000. After the device reset, the proc essor executes the application from 0×8000_0000. TC M is the main memory of the Mi-V processor and is me mory mapped to 0×8000_0000. The TCM gets initializ ed with the user application which stored in the SPI Fla sh. In the Mi-V processor memory map, the 0×8000_0 000 to 0×8000_FFFF range is defined for TCM memory interface and the 0×7000_0000 to 0×7FFF_FFFF range is defined for the APB interface.
MIV_ESS_C0_0	This MIV Extended Subsystem (ESS) is used to suppo rt GPIO and UART
CoreSPI_C0_0	CoreSPI is used to program the external SPI Flash
PF_SPI	PF_SPI macro interfaces the fabric logic to the external SPI Flash, which is connected to System Controller
PF_OSC	PF_OSC is a on board oscillator which generates 160 MHz output clock

Important: All the IP user guides and handbooks are available from Libero SoC > Catalog

Memory Map (Ask a Question)

The following table lists the memory map of the memories and peripherals.

Table 4-2. Memory Map Description

Peripherals	Start Address
TCM	0x8000_0000
MIV_ESS_UART	0x7100_0000
MIV_ESS_GPIO	0x7500_0000

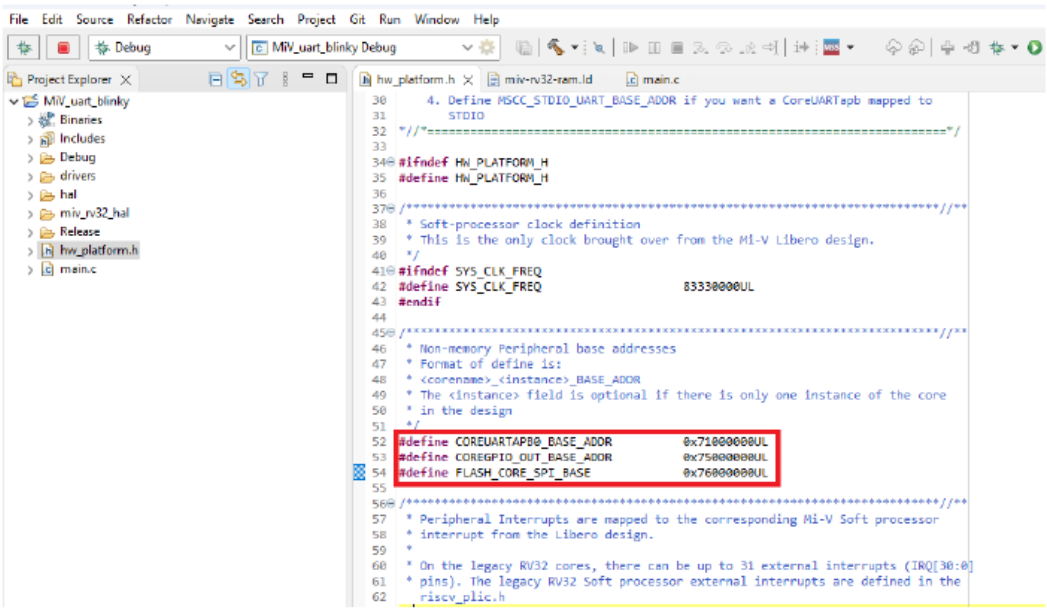
Software Implementation (Ask a Question)

Microchip provides SoftConsole toolchain to build a RISC-V user application executable (.hex) file and debug it. The reference design files include the Firmware workspace that contains the MiV_uart_blinky software project. The MiV_uart_blinky user application is programmed on an external SPI Flash using Libero® SoC. The given user

application prints the UART message “Hello World!” and blinks user LEDs on the board.

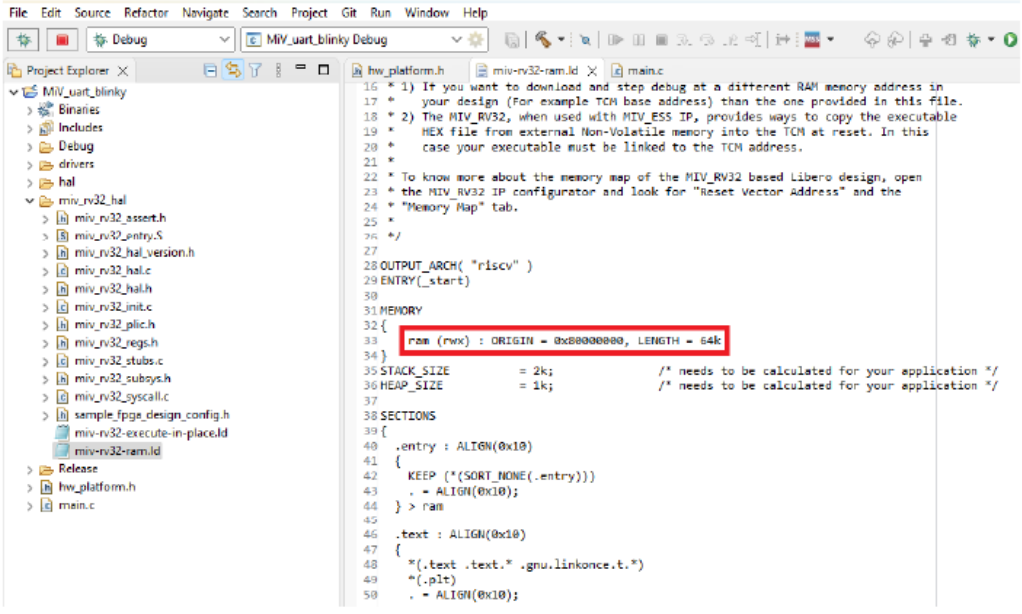
As per the Libero SoC design memory map, the UART and GPIO peripheral addresses are mapped to 0x71000000 and 0x75000000, respectively. This information is provided in the hw_platform.h file as shown in the following figure.

Figure 5-1. Peripheral Mapping



The user application must be executed from the TCM memory (code, data, and stack). Therefore, the RAM address in the linker script is set to the starting address of the TCM memory as shown in the following figure.

Figure 5-2. Linker Script



The linker script (miv-rv32-ram.ld) is available in the FW\MiV_uart_blinky\miv_rv32_hal folder of the design files. To build the user application, perform the following steps:

1. Create a Mi-V SoftConsole project
2. Download the MIV_RV32 HAL files and drivers from GitHub using the link as follows: **github.com/Mi-V-Soft-RISC-V/platform**
3. Import the firmware drivers

4. Create the main.c file with application code
5. Map firmware drivers and the linker script
6. Map memory and peripheral addresses
7. Build the application

For more information about these steps, see AN4997: PolarFire FPGA Building a Mi-V Processor Subsystem. The .hex file is created after successful build and it is used for design and memory initialization configuration in Running the Demo.

Setting Up the Demo (Ask a Question)

To set up the demo, perform the following steps:

1. Setting up the Hardware
2. Setting up the Serial Terminal (Tera Term)

Setting Up the Hardware (Ask a Question)

Important: Mi-V application debugging using SoftConsole debugger will not work if System Controller Suspend Mode is enabled. The System Controller Suspend Mode is disabled for this design to demonstrate Mi-V application.

To setup the hardware, perform the following steps:

1. Power off the board using the SW7 switch.
2. Open J31 jumper to use the external FlashPro programmer or Close J31 jumper to use the embedded FlashPro programmer.
   Important: Embedded Flash Pro Programmer can only be used for Programming through Libero or FPExpress it cannot be used for debugging Mi-V based Application.
3. Connect the host PC to the J24 connector using the USB cable.
4. To enable the SC_SPI, 1-2 pins of jumper J8 should be closed.
5. Connect the FlashPro programmer to J3 connector (JTAG header) and use another USB cable to connect the FlashPro programmer to the Host PC.
6. Ensure that the USB to UART bridge drivers are automatically detected, which can be verified through the device manager on the host PC.
   Important: As shown in Figure 6-1, the port properties of COM16 show that it is connected to USB serial port. Hence, COM16 is selected in this example. The COM port number is system specific. If the USB to UART bridge drivers are not installed, download and install the drivers from **www.microchip.com/en-us/product/mcp2200**.
7. Connect the power supply to J19 connector and switch ON the power supply using switch SW7.

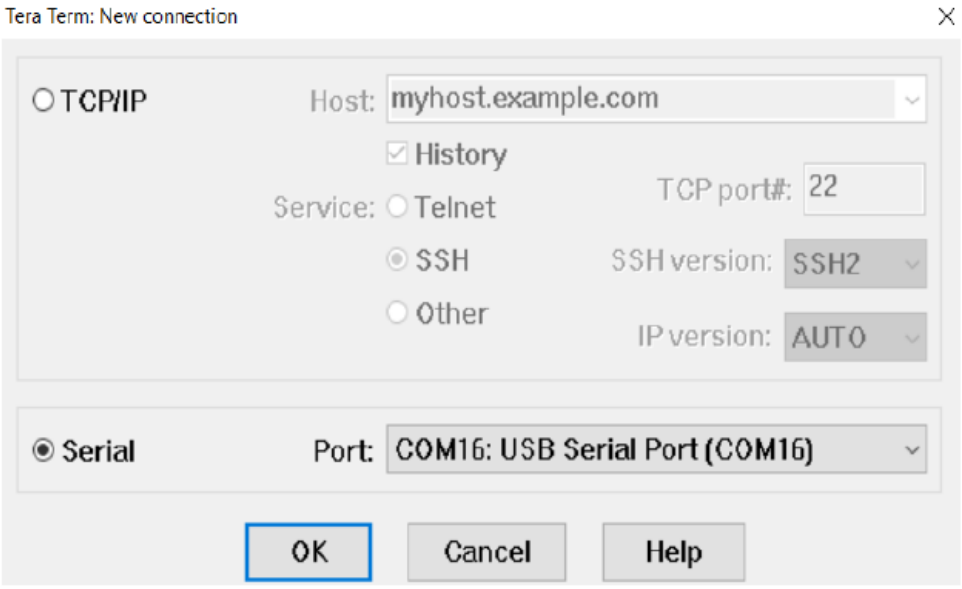
Setting Up the Serial Terminal (Tera Term) (Ask a Question)

The user application (MiV_uart_blinky.hex file) prints the “Hello World!” message on the serial terminal through the UART interface.

To set up the serial terminal, perform the following steps:

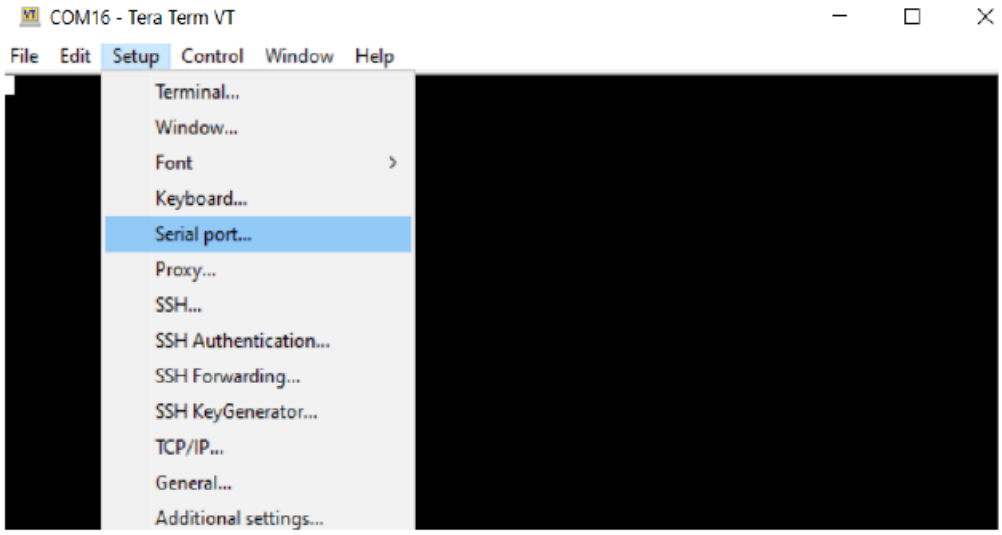
1. Launch Tera Term on the Host PC.
2. Select the identified COM Port in Tera Term as shown in the following figure.

Figure 6-1. Identifying the COM Port



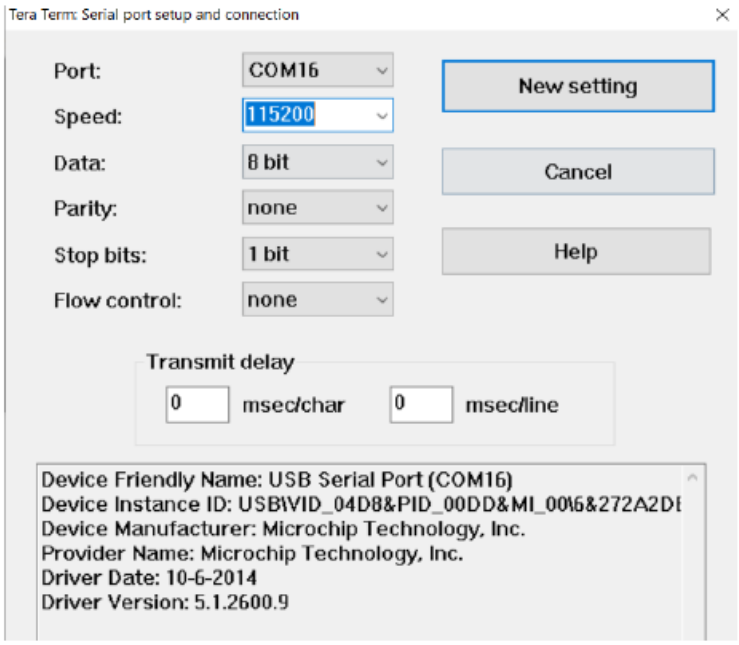
3. From the Menu bar, select Setup > Serial port to set up the COM port.

Figure 6-2. Setting Up the Serial Terminal



4. Set the Speed (baud) to 115200 and Flow Control to none and click on New setting option as shown in the following figure.

Figure 6-3. Setting Up the Baud Rate



After the serial terminal is set up, next step is to program the RT PolarFire® device.

Running the Demo (Ask a Question)

To run the demo, perform the following steps:

1. Generating the TCM Initialization Client
2. Programming the RT PolarFire® Device
3. Generating the SPI Flash Image
4. Programming the SPI Flash

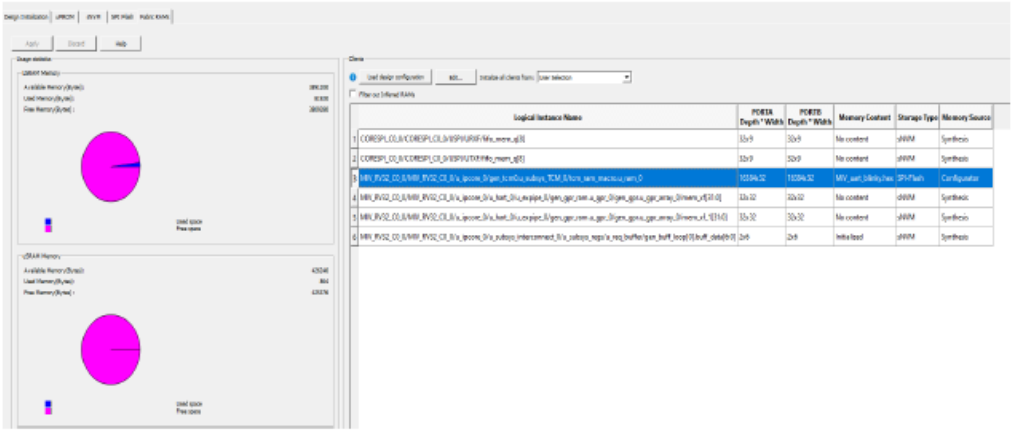
Generating the TCM Initialization Client (Ask a Question)

To initialize the TCM in RT PolarFire® using the system controller, a local parameters l_cfg_hard_tcm0_en in the miv_rv32_subsys_pkg.v file must be changed to 1'b1 before Synthesis. For more information, see the MIV_RV32 User Guide.

In Libero® SoC, the Configure Design Initialization Data and Memories option generates the TCM initialization client and adds it to sNVM, µPROM, or an external SPI Flash, based on the type of non-volatile memory selected. In this application note, the TCM initialization client is stored in the SPI Flash. This process requires the user application executable file (.hex file). The hex file (*.hex) is generated using SoftConsole application project. A sample user application is provided along with the design files. The user application file (.hex) is selected for creating the TCM initialization client using the following steps:

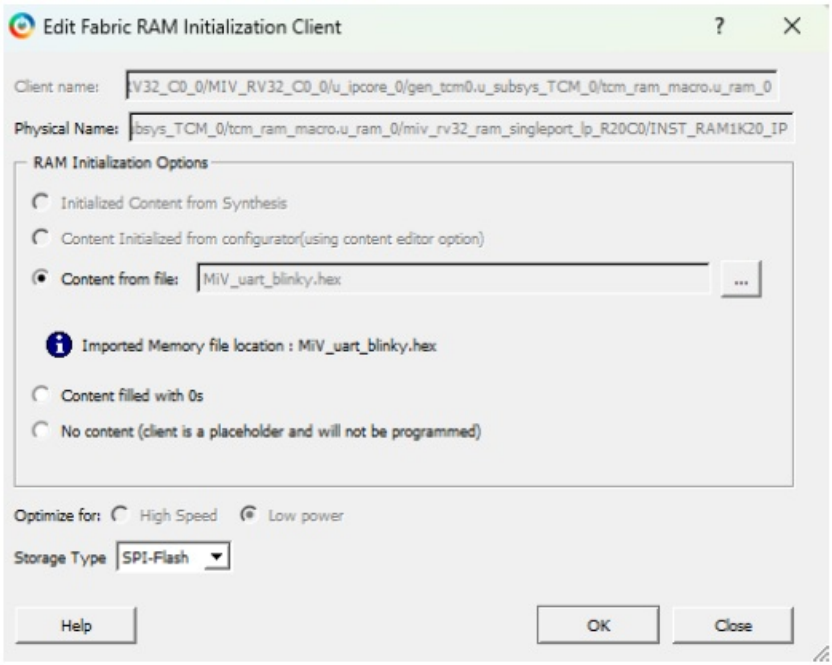
1. Launch Libero® SoC and run the script.tcl (Appendix 2: Running the TCL Script).
2. Select Configure Design Initialization Data and Memories > Libero Design Flow.
3. On the Fabric RAMs tab, select the TCM instance and double-click on it to open the Edit Fabric RAM Initialization Client dialog box, as shown in the following figure.
4.

Figure 7-1. Selecting the TCM Instance



In the Edit Fabric RAM Initialization Client dialog box, set Storage type to SPI-Flash. Then, select Content from file and click the Import (…) button as shown in the following figure.

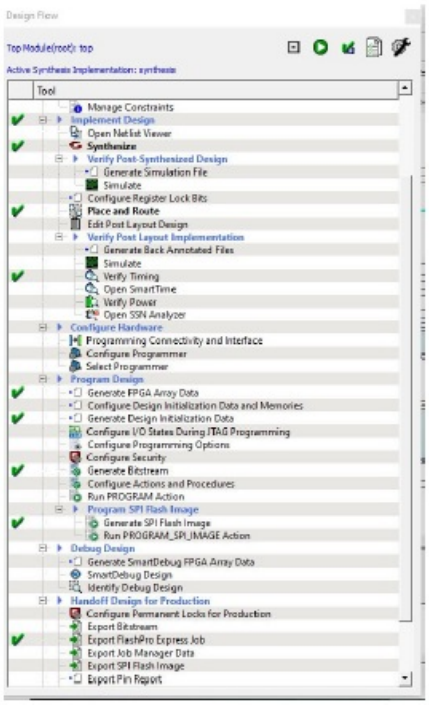
Figure 7-2. Importing the TCM Initialization Client



Programming the RT PolarFire Device (Ask a Question)

- The reference design files include the Mi-V processor subsystem project created using Libero® SoC. The RT PolarFire® device can be programmed using Libero SoC.
- The Libero SoC design flow is shown in the following figure.

Figure 7-3. Libero SoC Design Flow



To program the RT PolarFire device, open the Mi-V processor subsystem Libero project, which is created using the provided TCL scripts in Libero SoC, and double-click Run Program Action .

Generating the SPI Flash Image (Ask a Question)

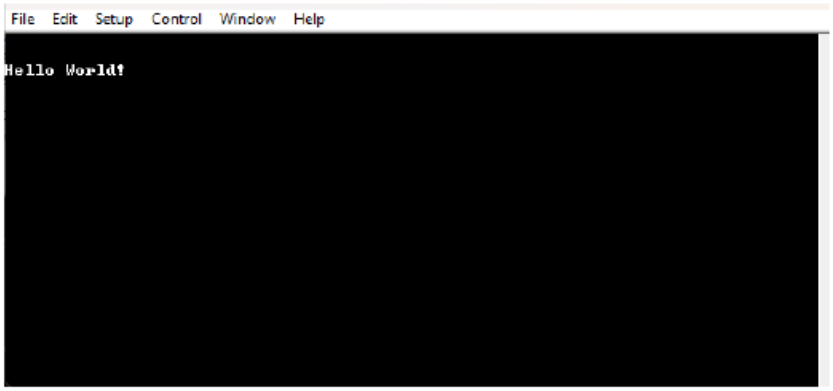
- To generate the SPI Flash image, double-click Generate SPI Flash Image on the Design Flow tab.
- When the SPI Flash image is generated successfully, a green tick mark appears next to Generate SPI Flash Image.

Programming the SPI Flash (Ask a Question)
To program the SPI Flash image, perform the following steps:

1. Double-click Run PROGRAM_SPI_IMAGE on the Design Flow tab.
2. Click Yes in the dialog box.

- When the SPI image is successfully programmed on to the device, a green tick mark appears next to Run PROGRAM_SPI_IMAGE.
- After SPI Flash programming is completed, the TCM is ready. As a result, LEDs 1, 2, 3, and 4 blink, then prints are observed on the serial terminal, as shown in the following figure.

Figure 7-4. UART Terminal



This concludes the demo.
The RT PolarFire® device and the SPI Flash can also be programmed using FlashPro Express, see Appendix 1: Programming the RT PolarFire Device and SPI Flash Using FlashPro Express.

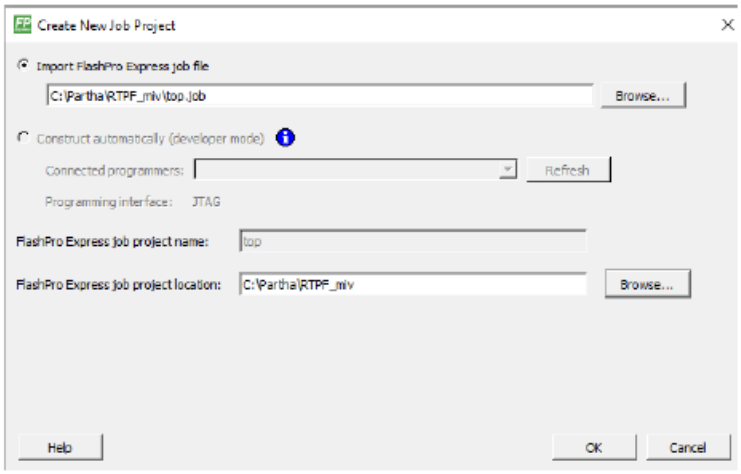
Appendix 1: Programming the RT PolarFire Device and SPI Flash Using FlashPro Express (Ask a Question)

The reference design files include a programming job file for programming the RT PolarFire® device using FlashPro Express. This job file also includes the SPI Flash image, which is the TCM initialization client. FlashPro Express programs both the RT PolarFire device and the SPI Flash with this programming .job file. The programming .job file is available at DesignFiles_directory\Programming_files.

To program the RT PolarFire device with the programming file using FlashPro Express, perform the following steps:

1. Set up the hardware, see Setting Up the Hardware.
2. On the host PC, launch the FlashPro Express software.
3. To create a new job project, click New or select New Job Project from FlashPro Express Job from the Project menu.
4. Enter the following in the dialog box:
    - Programming job file: Click Browse and navigate to the location where the .job file is located and select the file. The job file is available at DesignFiles_directory\Programming_files.
    - FlashPro Express job project location: Click Browse and navigate to the location where you want to save the project.

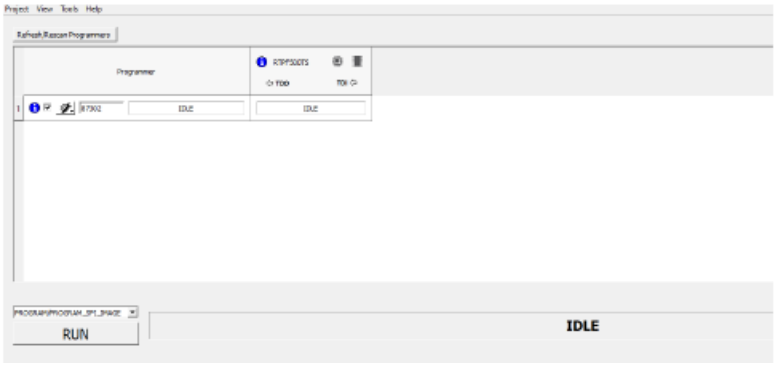
Figure 8-1. New Job Project from FlashPro Express Job



5. Click OK. The required programming file is selected and ready to be programmed.

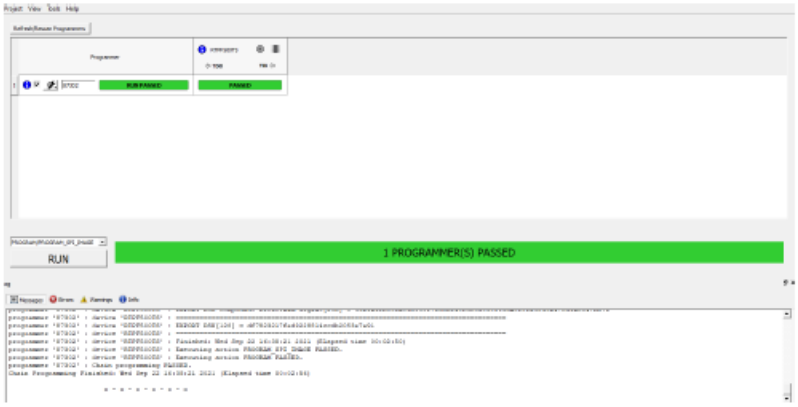
6. The FlashPro Express window appears as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, check the board connections and click Refresh/Rescan Programmers.

Figure 8-2. Refresh/Rescan Programmers



7. Click RUN. When the device is programmed successfully, a RUN PASSED status is displayed as shown in the following figure.

Figure 8-3. FlashPro Express—RUN PASSED



This concludes the RT PolarFire device and the SPI Flash programming. After programming the board, observe the “Hello World!” message printed on the UART terminal and the blinking of user LEDs.

Appendix 2: Running the TCL Script (Ask a Question)

TCL scripts are provided in the design files folder under directory HW. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, perform the following steps:

1. Launch the Libero software.
2. Select Project > Execute Script…..
3. Click Browse and select script.tcl from the downloaded HW directory.
4. Click Run.

After successful execution of TCL script, Libero project is created within HW directory.

- For more information about TCL scripts, see rtpf_an4229_df/HW/TCL_Script_readme.txt. For more information on TCL commands, see Tcl Commands Reference Guide. Contact Microchip

- Technical Support for any queries encountered, while running the TCL script.

Revision History (Ask a Question)

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 10-1. Revision History

Revision	Date	Description
B	10/2024	The following is the list of changes made in the revision B of the document: • Updated the board revision in Table 1-1 • Added Mi-V ESS and CoreSPI to the Figure 3-1 in Design Description section • Added MIV_ESS_C0_0 and CoreSPI_C0_0 blocks in the Table 4-1 in IP Blocks section • Updated the Start Address value in Table 4-2 • Updated Figure 5-1 and Figure 5-2 in the Software Implementation section • Added a note regarding system controller suspend mode, added jumper settings of SPI Enable and FlashPro programming (either embedded or external) in steps in Setting Up the Hardware section • Updated Figure 6-1, Figure 6-2, and Figure 6-3 in Setting Up the Serial Terminal (Tera Term) section • Updated Figure 7-1 and Figure 7-2 in the Generating the TCM Initialization Client section • Updated Figure 7-4 in Programming the SPI Flash section • Added Appendix 2: Running the TCL Script section
A	10/2021	The first publication of this document

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Application Note

Documents / Resources

	MICROCHIP AN4229 Risc V Processor Subsystem [pdf] User Guide AN4229, AN4229 Risc V Processor Subsystem, AN4229, Risc V Processor Subsystem, Processor Subsystem, Subsystem

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