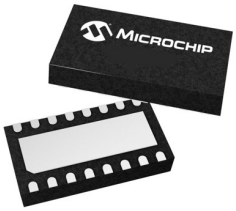

MICROCHIP AN3468 HDBaseT Type 3 Powered Device Front-End Owner's Manual

AN3468
Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Front-End Using PD702x0 and PD701x0 ICs

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Introduction

This application note provides guidelines for designing a Power over Ethernet (PoE) Powered Device (PD) system for IEEE® 802.3af, IEEE 802.3at, HDBaseT (PoH), and Universal Power Over Ethernet (UPoE) applications by using Microchip's family of front-end PD integrated circuits. The following table lists Microchip PD products offerings.

Table 1. Microchip Powered Device Products Offerings

Part	Type	Package	IEEE® 802.3af	IEEE 802.3at	HDBaseT (PoH)	UPoE
PD70100	Front end	3 mm × 4 mm 12L DFN	x	—	—	—
PD70101	Front end + PWM	5 mm × 5 mm 32L QFN	x	—	—	—
PD70200	Front end	3 mm × 4 mm 12L DFN	x	x	—	—
PD70201	Front end + PWM	5 mm × 5 mm 32L QFN	x	x	—	—
PD70210	Front end	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210A	Front end	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210AL	Front end	5 mm × 7 mm 38L QFN	x	x	x	x
PD70211	Front end + PWM	6 mm × 6 mm 36L QFN	x	x	x	x
PD70224	Ideal diode bridge	6 mm × 8 mm 40L QFN	x	x	x	x

Microchip offers standalone front-end PD devices that require an external PWM IC to convert the high PoE voltage down to the regulated supply voltage used by the application. Additionally, Microchip offers PD devices that integrate the front-end PD and the PWM into the product package. The scope of this application note is to describe the design of PoE PD front using Microchip front-end-only products (PD701x0 and PD702x0). This document also includes a description of key features and functions of Microchip's PD products, a brief overview of PoE functionality, standards and key technical considerations for a PoE PD design.
Front-end PD products provide the necessary detection, classification, power-up functions, and operating current levels compliant with the listed standards.
Microchip offers a complementary product for PoE PD applications, the PD70224 Ideal Diode Bridge, which is a low-loss alternative to the dual diode bridges for input polarity protection.
Microchip offers complete reference design packages and Evaluation Boards (EVBs). For access to these design packages, device data sheets, or application notes, please consult your local Microchip Client Engagement Manager or visit our website at **www.microchip.com/poe**.
For technical support, consult your local Embedded Solutions Engineers or go to **microchipsupport.force.com/s/**.

Microchip PoE Front-End PD Controller Key Features

The following are common features of all Microchip PoE

- PD controllers.
- PD detection signature
- Programmable PD classification signature
- Integrated isolation switch
- 24.9 k detection signature resistor disconnection when power is on, for power saving
- Inrush current limit (soft start)
- Integrated 10.5V start-up supply output for DC-DC converters
- Overload protection
- Internal discharge circuitry for DC-DC bulk capacitor
- Wide temperature operating range 40 °C to 85 °C
- On-Chip thermal protection

The following table lists features that vary across PoE PD controllers.

Table 2. Microchip PoE Front-End PD Controller Key Features

Part Number	IC Type	Standards	Max. Power (W)	Max. Current (A)	Max. Resistance (Ω)	FLAGS 1	WA Priority Pin 2	VAUX
PD70100	Front End	IEEE 802.3af	15.4	0.45	0.6	PGOOD	No	Yes
PD70200	Front End	IEEE 802.3af IEEE 802.3at	47	1.123	0.6	AT PGOOD 2-event	No	Yes
PD70210A/AL	Front End	IEEE 802.3af IEEE 802.3at PoH UPoE	95	2	0.3	AT 4P_AT HD 4P_HD 2/3 event	Yes	Yes
PD70210	Front End	IEEE 802.3af IEEE 802.3at PoH UPoE	95	2	0.3	AT 4P_AT HD 4P_HD PGOOD 2/3 event	No	Yes
PD70224	Ideal Diode Bridge	IEEE 802.3af IEEE 802.3at PoH UPoE	95	2	0.76	N/A	N/A	N/A

1. For detailed descriptions, see 4. General Operation Theory.
   a. AT—AT flag
   b. 4P_AT—4-pair AT flag
   c. HD—HDBaseT flag
   d. 4P_HD—4-pair HDBaseT
   e. PGOOD—Power Good flag
2. WA priority pin controls support of wall adapter functionality and enforces auxiliary supply priority to supply power to the load from an external DC source.

PoE Overview

PoE consists of a power source, referred to as Power Source Equipment (PSE), an Ethernet or Network cable (typically contained in an infrastructure) with maximum length of 100 meters, and a Powered Device (PD) that accepts both data and power from the Power Interface (PI) of the Ethernet cable. The PI is typically an eight pin RJ45 type connector. The PSE typically resides in an Ethernet Switch or Midspan. The PD resides in what is sometimes referred to as Data Terminal Equipment (DTE). The following figures show the diagrams of this arrangement.

Figure 1-1. Two-Pair Power over Data–Alternative A

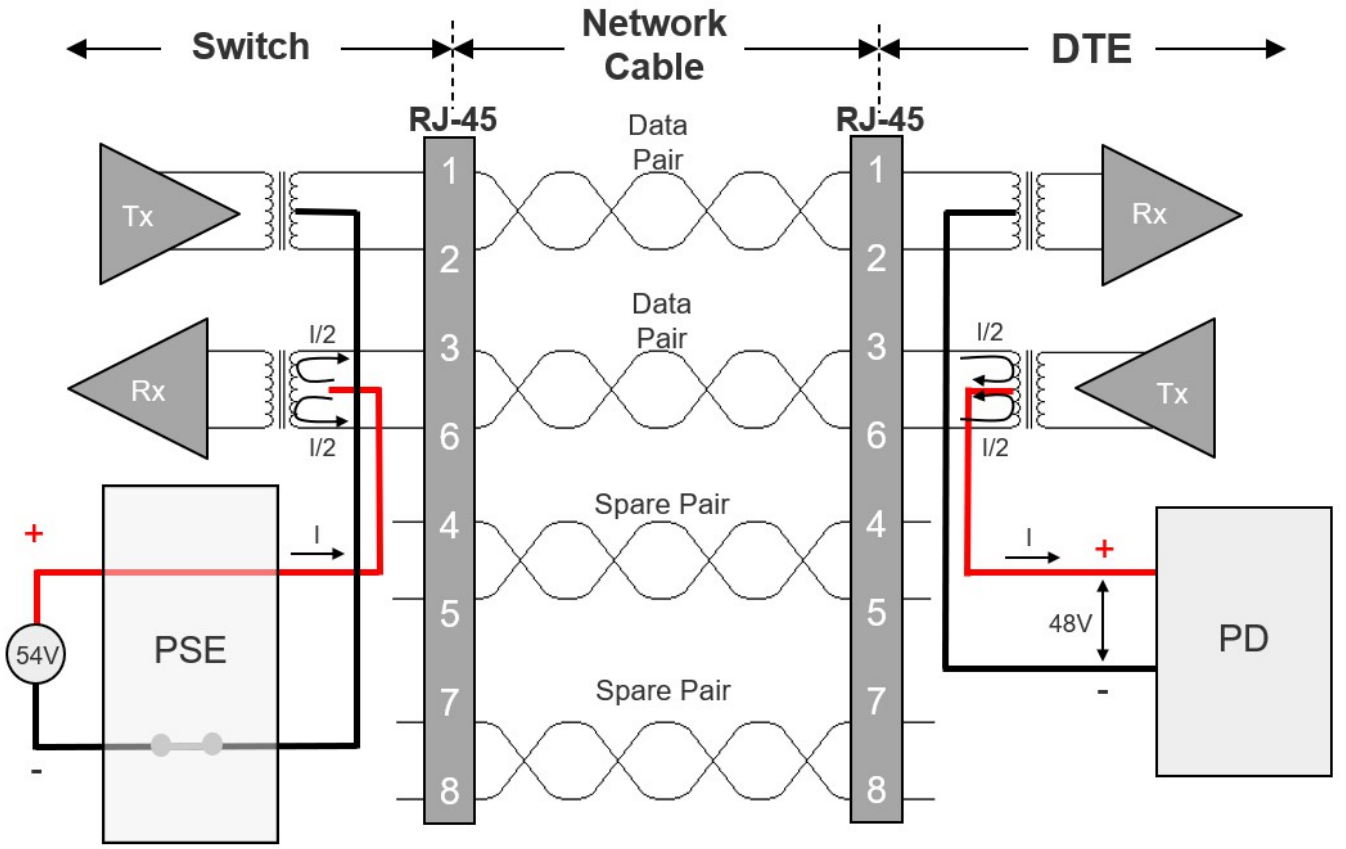


Figure 1-2. Two-Pair Power over Spare–Alternative B

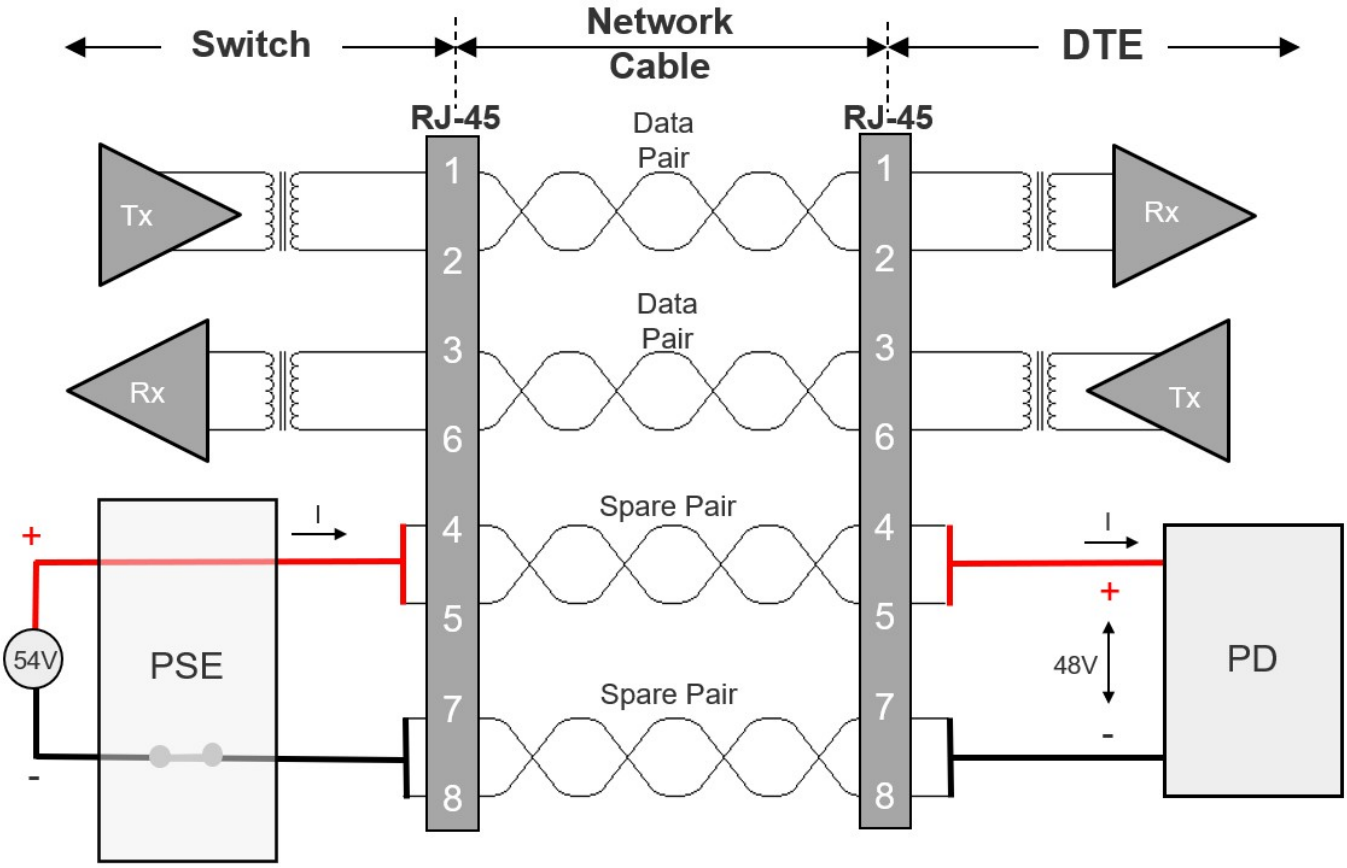
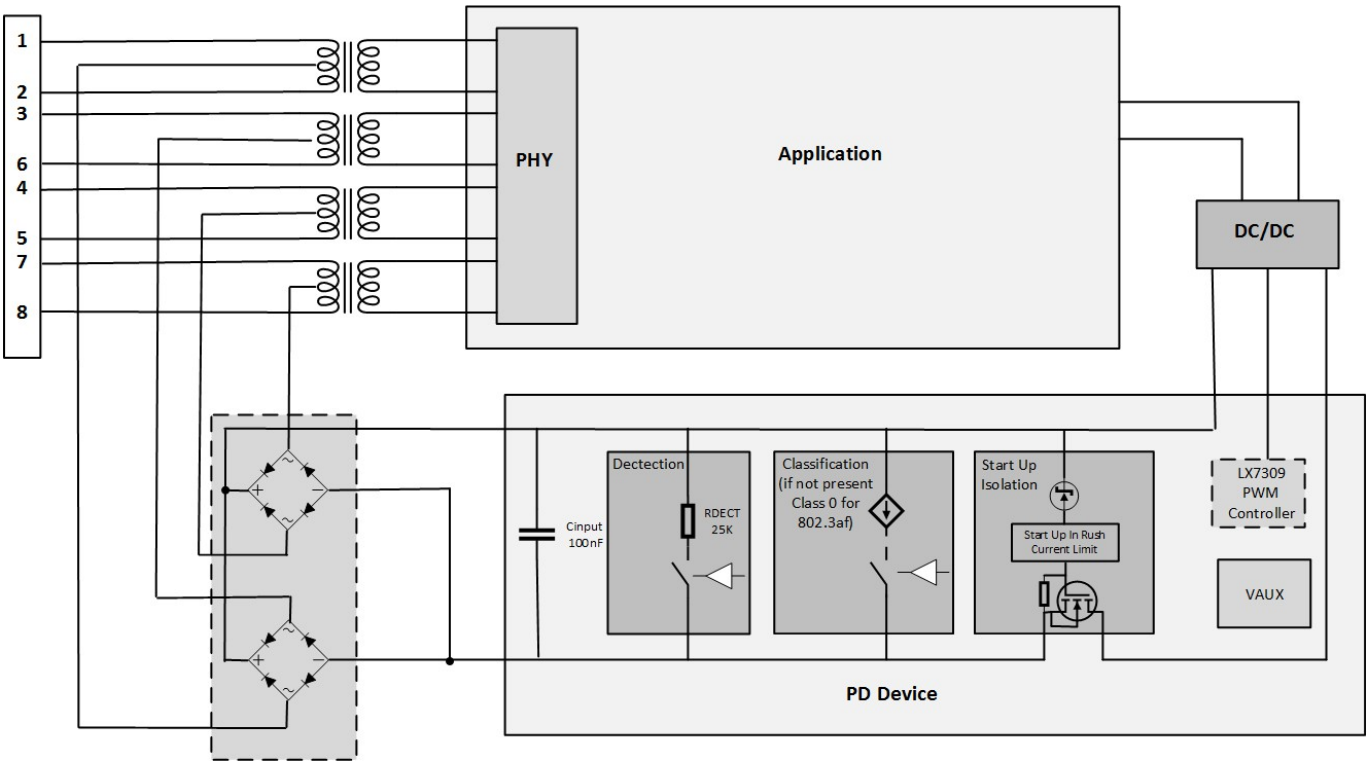


Figure 1-3. Basic PD Block Diagram



The PD provides the following functions.

- Polarity Protection–voltage polarity at the PI is not guaranteed by standards. Therefore, a diode bridge is used to ensure correct polarity at the PD input. For optimized power loss and PCB area, use the Microchip PD70224 Ideal Diode Bridge. Standard diode bridges can also be used.
- Detection–provides signature for detection.
- Classification–provides signatures for classification signatures.
- Start-Up–after detection and classification, provides a controlled power application.
- Isolation–the PoE domain must have 1500 VAC isolation from earth ground and from user accessible parts. It is recommended to provide this isolation via an isolated DC/DC convertor. With non-isolated designs, the end application has to provide this isolation. There is a perception that non-isolated design saves cost, but in reality this is not necessarily true because you still need to provide the controller's bias after initial start-up, which means a custom inductor with auxiliary bootstrap winding.
- VAUX–bias for DC/DC start-up. All Microchip PoE PD ICs have an available regulated voltage output, VAUX, to be used primarily as a start-up supply for an external DC/DC controller. VAUX is a low current, low duty cycle output, providing current momentarily until an external bootstrap supply can take over.
- PWM Controller and DC/DC–converts high PoE voltage down to regulated supply voltage used by the application. The PWM can be an external Microchip device or integrated into the Microchip PD package.

  The following tables compare PoE standards for the PSE and the PD. The HDBaseT (PoH) standard follows IEEE 802.3at type 2 cable types. However, due to its higher supported current, it limits the number of cables in a single cable bundle.

Table 1-1. IEEE 802.3af, 802.3at, and HDBaseT Standards for PSE

PSE Requirements	IEEE® 802.3af or IEEE 802.3at Type 1	IEEE 802.3at Type 2	2-Pair HDBaseT Type 3	4-Pair HDBaseT Type 3
Guaranteed power at PSE output	15.4W	30W	47.5W	95W
PSE output voltage	44V to 57V	50V to 57V	50V to 57V	50V to 57V
Guaranteed current at	350 mA DC with up	600 mA DC with up	950 mA DC with up	2x 950 mA DC with
PSE output	to 400 mA peaks	to 686 mA peaks	to 1000 mA peaks	up to 2000 mA peaks
Maximum cable loop resistance	200	12.50	12.50	12.50
Physical layer classification	Optional	Mandatory	Mandatory	Mandatory
Supported physical layer classification classes	Class 0 to 4	Class 4 mandatory	Class 4 mandatory	Class 4 mandatory
Data link classification	Optional	Optional	Optional	Optional
2-Events classification	Not required	Mandatory	Not required	Not required
3-Events classification	Not required	Not required	Mandatory	Mandatory
4-pair power feeding	Not allowed	Allowed	NA	Allowed
Communication	10/100 BaseT	10/100/1000 BaseT	10/100/1000/	10/100/1000/
Communication supported	10/100 BaseT (Midspan) 10/100/1000 BaseT (switch)	10/100/1000 BaseT including Midspans (Both type1 and type2)	10/100/1000/ 10000 BaseT	10/100/1000/ 10000 BaseT

Table 1-2. IEEE 802.3af, 802.3at, and HDBaseT Standards for PD

PD Requirements	IEEE 802.3af or IEEE 802.3at Type 1	IEEE 802.3at Type 2	HDBaseT Type 3
Guaranteed power at PD input after 100 m cable	12.95W	25.50W	72.40W
PD input voltage	37V to 57V	42.5V to 57V	38.125V to 57V
Maximum DC current at PD input	350 mA	600 mA	1.7A
Physical layer classification	Mandatory (No class= Class 0)	Mandatory	Mandatory
Supported physical layer classification classes	Class 0 to 4	Class 4 mandatory	Class 4 mandatory
Data link classification	Optional	Optional	Optional
2-Events classification	Not required	Mandatory	Optional
4-pair power receiving	Allowed	Allowed	Supports
Communication supported	10/100 BaseT (Midspan) 10/100/1000 BaseT (switch)	10/100/1000 BaseT including Midspans (both type 1 and type 2)	10/100/1000/10000 BaseT

DC voltage through wire pairs can be of either polarity. To accommodate all possible combinations of PoE power available at the PI, use of the PD70224 Ideal Diode Bridge or dual diode bridges on the PD side is required.
In the detection phase, standards define methods of determining whether a cable is connected to a standard compliant PD, that is a device capable of receiving power, connected to a non-power receiving capability device or disconnected.
These standards further define methods of determining power requirements or how much power the connected PoE-compliant PD is capable of receiving and methods by which the PD might determine the power level that is supported by the PSE. This is called the classification phase.
A compliant PSE does not apply operating power to the PI until the it has successfully detected a PoE compliant PD. During detection phase, a PSE applies a series of low voltage test pulses between 2.80V and 10.0V. In response to these pulses, a PoE-compliant PD must provide a valid signature, which requires differential resistance between 23.7 k and 26.3 k and input capacitance between 50 nF and 120 nF. To provide a valid detection resistance, all Microchip PoE PD controllers require an external 24.9 k resistor. This resistor is connected between the PD device's VPP and RDET pins. When a Microchip PD controller observes input voltage in the detection range 2.7V to 10.1V, it internally connects this resistor to the PI. After detection phase is over, the Microchip controller automatically disconnects the detection resistor to avoid extra power losses. A 100V ceramic capacitor must be connected between the VPP and VPN in pins of the PD device to provide a valid detection capacitance (recommended values 82 nF to 100 nF).
After a valid signature is detected, the PSE can start the classification phase. Classification is optional for 802.3af and 802.3at type 1 PSEs and PDs; and is mandatory for 802.3at type 2 and PoH. The PSE increases the voltage into a voltage range of 15.5V to 20.5V for a specified time duration. This is called a classification finger. If more than one finger is required, the classification fingers are separated by what is referred to as the mark voltage, where the PSE lowers voltage to the range between 6.3V to 10.1V, again for a specified period of time.
While the classification voltage or class finger is applied, the PD then must draw a constant current to signal its class. In Microchip controllers the classification signature is programmed by a resistor RCLS connected between the PD devices RCLS and VPN in pins. When input voltage is in the classification range, the PD draws current programmed by RCLS.
An IEEE 802.3at type 2 compliant PD is required to recognize the 2-event classification and provide to internal circuits the AT flag signal that indicates PD is connected to an AT type 2 compliant PSE.
A PoH type 3 compliant PD is required for recognizing the 3-event classification and provide to internal circuits the HDBaseT flag signal that indicates PD is connected to an HDBaseT type 3 compliant PSE.
If the port voltage present at the PI drop is below 2.8V, PSE class information resets and the PD must reset the

class dependent flag.

Microchip PoE PDs contain an isolating switch that disconnects the return side of the PD from the PI during detection and classification phases, or during power loss and overload. The PD turns the isolating switch on at PI voltage levels 42V or higher and turn off the isolating switch at PI voltage levels below 30.5V. They also actively limit the current during start-up to 350 mA or less.

The following figures show the basic PoE detection, classification, and power-up sequences for type 1 IEEE 802.3af and type 2 IEEE 802.3at, respectively. Class levels, their corresponding currents, and recommended RCLS resistors are listed in Table 1-3.

Figure 1-4. Basic PoE Detection, Classification, and Power-Up Sequences for IEEE 802.3af Standard

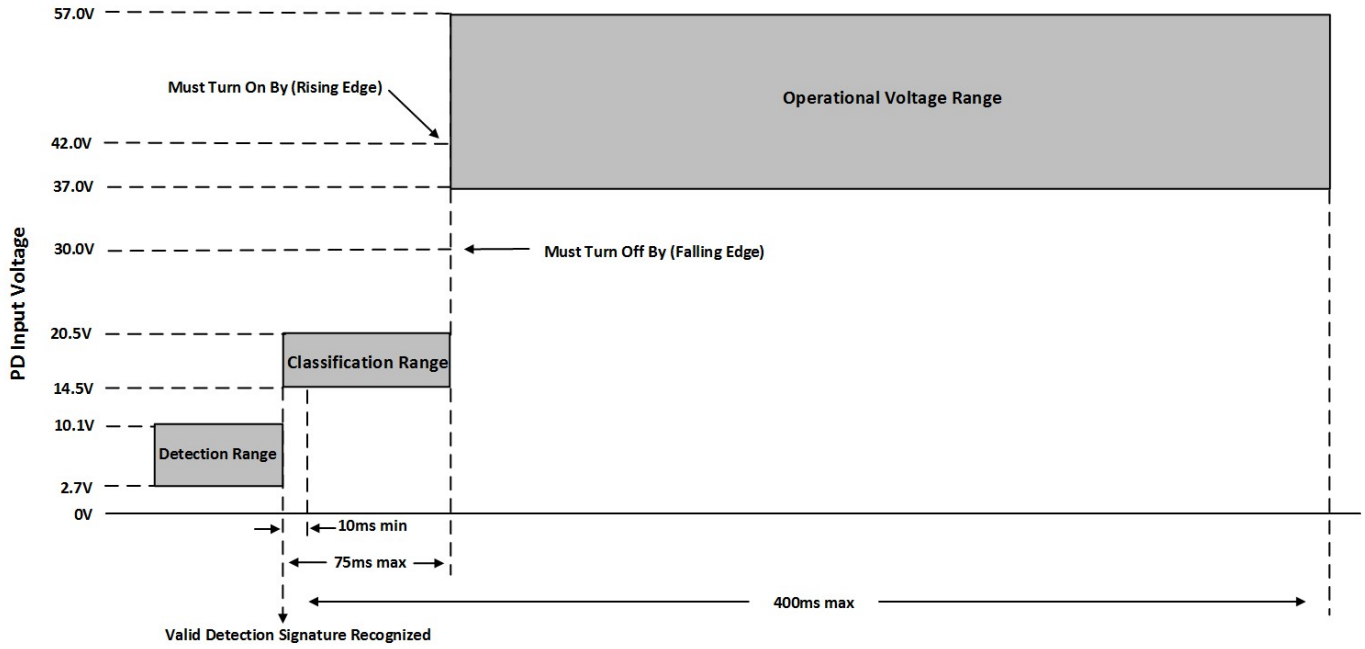


Figure 1-5. Basic PoE Detection, Classification, and Power-Up Sequences for 802.3at Standard

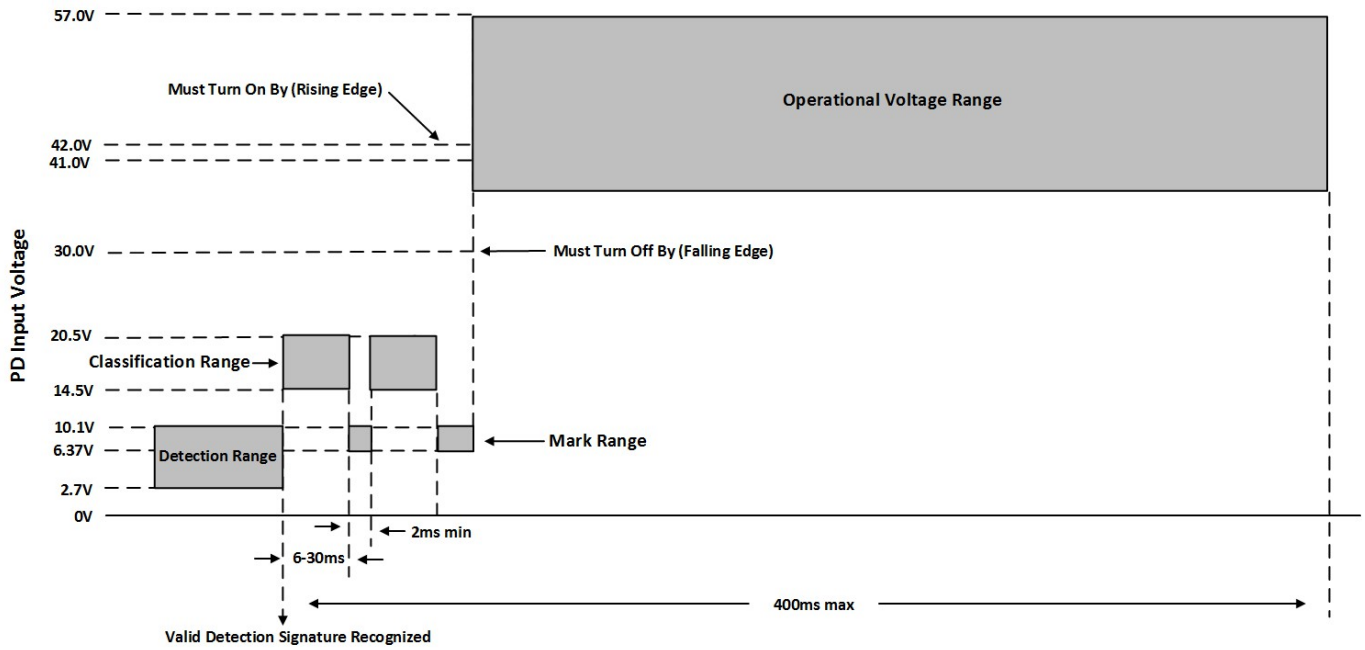


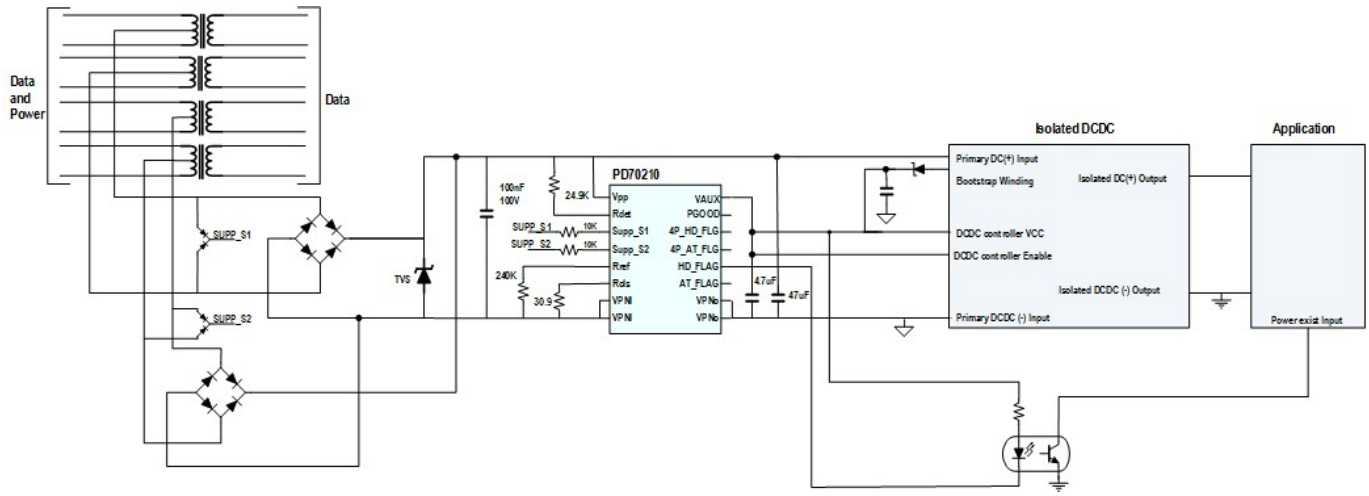
Table 1-3. Classification Current Definitions and Required Class Setting Resistors

Class	PD Current Draw During Classification			RCLASS Resistance Values, Ω
	Min	Nominal	Max.	
0	0 mA	NA	4 mA	Not installed
1	9 mA	10.5 mA	12 mA	133
2	17 mA	18.5 mA	20 mA	69.8
3	26 mA	28 mA	30 mA	45.3
4	36 mA	40 mA	44 mA	30.9

Note: PD input voltage during classification phase is 14.5V to 20.5V.

Using PD702x0 and PD701x0 ICs

The PD702x0 and PD701x0 ICs can be used for both 2-pair and 4-pair systems, as shown in the following figure. The output from the two diode bridges are connected to VPP (positive bus) and VPNIN (negative bus). Output connections to the DC/DC converter/application are made between VPP and VPNOUT. Figure 2-1. Typical 2- or 4-Pair Configuration with a Single PD70210/A/AL IC



In addition to the basic input/output connections, the following external components are required for a typical application:

- **Detection resistor:** Connect a 24.9 k ±1% resistor between VPP and RDET pin. This resistor is used to provide the detection signature. A low wattage type can be used as there is less than a 7 mW stress on this resistor while detection phase is active, and the resistor is disconnected after power is on.
- **Reference resistor:** A resistor setting bias current for internal circuitry has to be connected between RREF pin and VPNIN. Connect a 60.4 k ±1% resistor for PD70210/A/AL ICs and 240 k ±1% for PD70100/PD70200. This resistor must be located close to the IC. A low wattage type can be used (power dissipation is less than 1 mW).
- **Classification current resistor:** The value of the resistor connected between RCLASS pin and VPNIN determines the PD current draw during the classification phase. Values corresponding to IEEE compliant classification levels are provided in the previous table.
- **Input capacitor:** IEEE requires a capacitance between 50 nF and 120 nF be present between VPP and VPNIN

for a valid detection signature. For best performance and to protect the chip from sharp voltage transients, Microchip recommends using a ceramic capacitor 82 nF to 100 nF per 100V. It must be located as close as practical to the chip.

- **Input TVS:** If diode bridges are used, for basic protection against basic level voltage transients (<1 kV), both 10×700 µS or 1.2×50 µS, a 58V TVS (such as SMBJ58A or equivalent) must be connected between VPP pin and VPNIN. If the active bridge PD70224 is used or to meet surge requirements of IEC/EN 61000-4-5 (2014 Ed.3), ITU-T K21, and GR-1089, then see the **Microchip application note AN3410**.
- **SUPP_S1 and SUPP_S2 inputs** (PD70210/A/AL only): 10 k resistors must be connected in series to each of the input pins SUPP_S1 and SUPP_S2. The signals for these pins come from corresponding pins of the active bridge PD70224, or from an auxiliary rectifier if regular diode bridges are used as shown in the preceding figure. These inputs in PD70210/A/AL allow setting AT and 4-pair AT flags with some legacy 4-pair midspans that provide only one classification pulse on each pair set. If SUPP_S1 and SUPP_S2 pins left open, the status of the flags in PD70210/A/AL are per the following table.

Table 2-1. Status of PD70210/A/AL Flags when SUPP_S1 and SUPP_S2 Pins Not Connected

Number of Fingers (N-Event Classification)	AT Flag	HDBaseT Flag	4-Pair AT Flag	4-Pair HDBaseT Flag
1	Hi Z	Hi Z	Hi Z	Hi Z
2	0 V	Hi Z	Hi Z	Hi Z
3	0 V	0 V	Hi Z	Hi Z
4	0 V	0 V	0 V	Hi Z
5	0 V	0 V	0 V	Hi Z
6	0 V	0 V	0 V	0 V

- Power good (PD70100, PD70200, and PD70210 only): An open drain power good signal is available at the PGOOD pin. After start-up, a PGOOD flag generates low voltage with respect to VPNOUT to inform the application that the power rails are ready. Pull-up voltage on this pin is limited to 20V for PD70210 and to VPP voltage for PD7010x/PD7020x. Power good can also be pulled up by the bootstrap winding output of the DC-DC, in which case, it must be isolated via a Schottky diode from VAUX to prevent additional current draw from VAUX during start up.

  Note: If PGOOD is used to start-up an external application, the application must provide 80 ms inrush to operating state delay required by IEEE 802.3.
- Flags reporting PSE type: These flags can be sampled by the application to decide upon the maximum power to consume. All these flags are open drain pins. Pull-up voltage on all these pins is limited to 20V for PD70210/A/AL, and to VPP voltage for PD70200/PD70100. The flags can be pulled up by the bootstrap winding output of the DC-DC, in which case, it must be isolated through a Schottky diode from VAUX. Flags state is set only once at port startup and are asserted with at least 80 ms delay to indicate the application that inrush to operating state delay is over. If SUPP_S1 and SUPP_S2 pins are changing after port turn on, the flags do not change accordingly.

    - AT_FLAG (available on PD70210/A/AL and PD70200): This flag goes active low when a Type 2 PSE and PD mutually identify each other via classification.
    - HD_FLAG (available on PD70210/A/AL): This flag goes active low when a HDBaseT PSE and PD mutually identify each other via classification.
    - 4P_AT_FLAG (available on PD70210/A/AL): This flag goes active low when a 4-pair version of a PSE and PD mutually identify each other via classification.
    - 4P_HD_FLAG (available on PD70210/A/AL): This flag goes active low when a 4-pair (Twin) HDBaseT PSE
      and PD mutually identify each other via classification.
- VAUX output: VAUX is a low power regulated output available for use as a start-up supply for an external DC-DC converter controller. After start-up, VAUX must be supported from an auxiliary (bootstrapped) winding of the DC-DC converter. VAUX output requires ceramic capacitor of minimum 4.7 µF to be connected directly between VAUX pin and VPNOUT pin and placed physically close to the device.

Operation with an External DC Source

PD applications utilizing the PD70210A/AL IC provide an external auxiliary power source (DC wall adapter) priority function. In general, there are three methods of providing power with an external source:

- The external source is connected directly to the PD input (VPP to VPNIN). This requires the external source output voltage to be 42V minimum at no load and more than 36V at maximum load. The adapter must be isolated from VPP or VPNIN through an OR-ing diode. This configuration does not provide adapter priority and can be used with PD70210, PD70100, and PD70200.
- The external source is connected directly to PD output (between VPP and VPNOUT). The external source must be isolated from VPP or VPNOUT through an OR-ing diode. For adapter priority, only the PD70210A/AL must be used.
- The external source is connected directly to application's low voltage supply rails (output of DC-DC converter). The external source must be isolated from application power supply's output either through a switched connection, a diode, or a separate regulator that sources current only (does not sink current).

The following three figures show examples of PD70210A/AL configured with an external wall adapter. For more details and recommended values of voltage dividers, see AN3472: Implementing Auxiliary Power in PoE. Figure 3-1. Auxiliary Power Connected to PD70210 Input

Figure 3-1. Auxiliary Power Connected to PD70210 Input

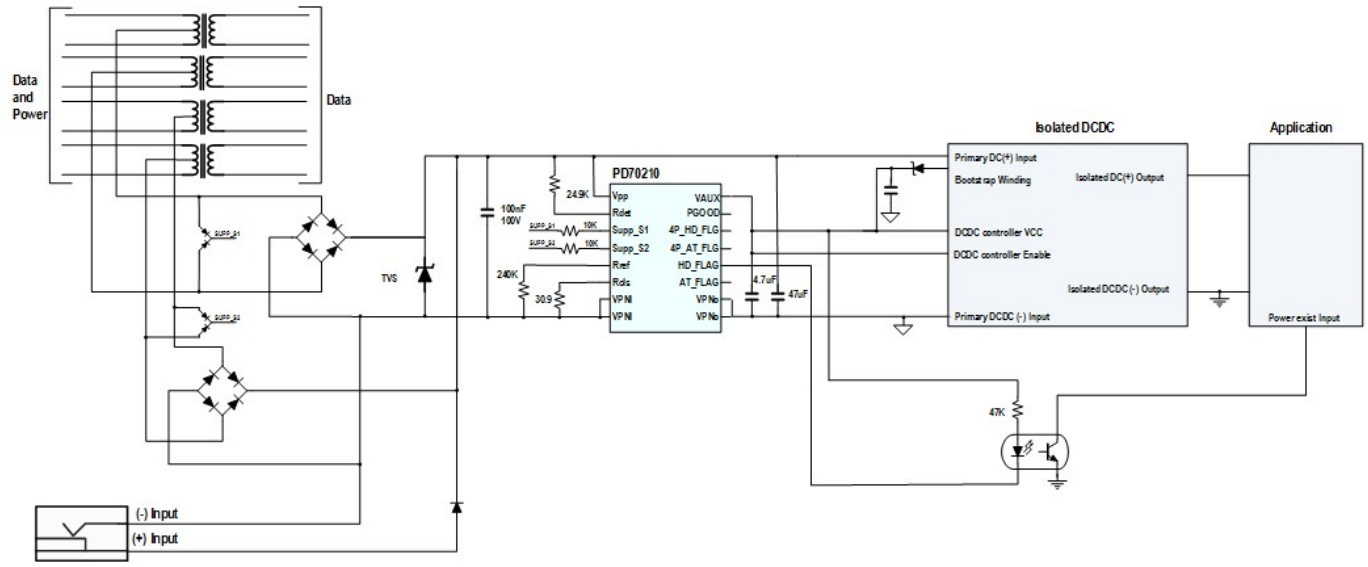


Figure 3-2. Auxiliary Power Connected to PD70210A Output

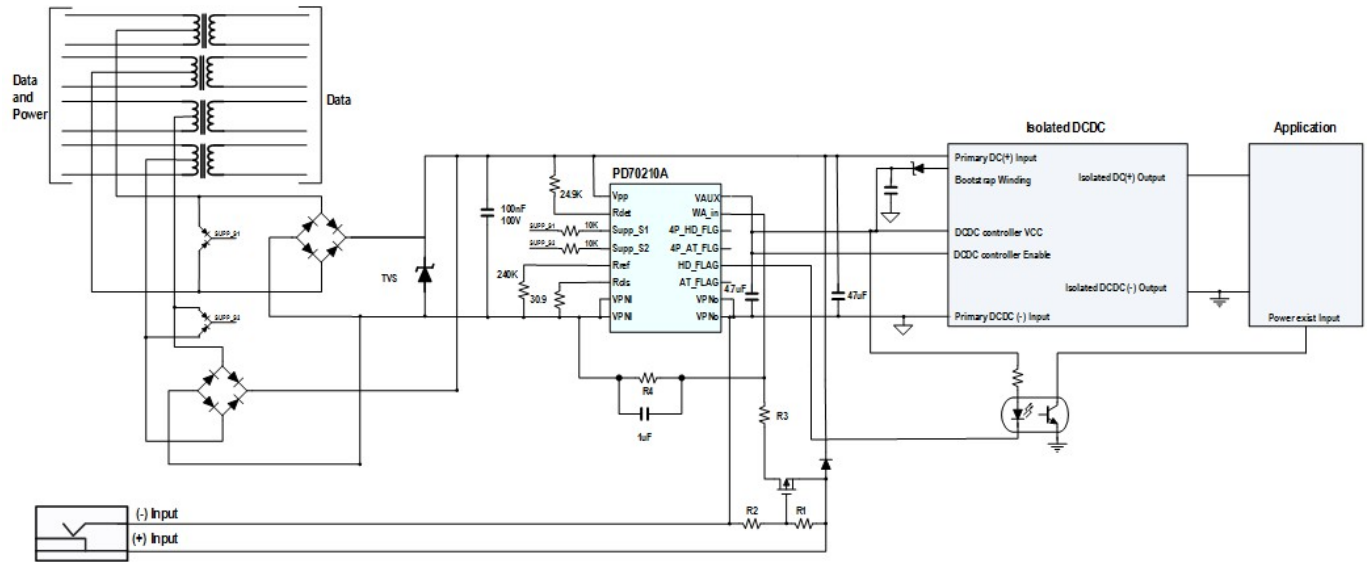
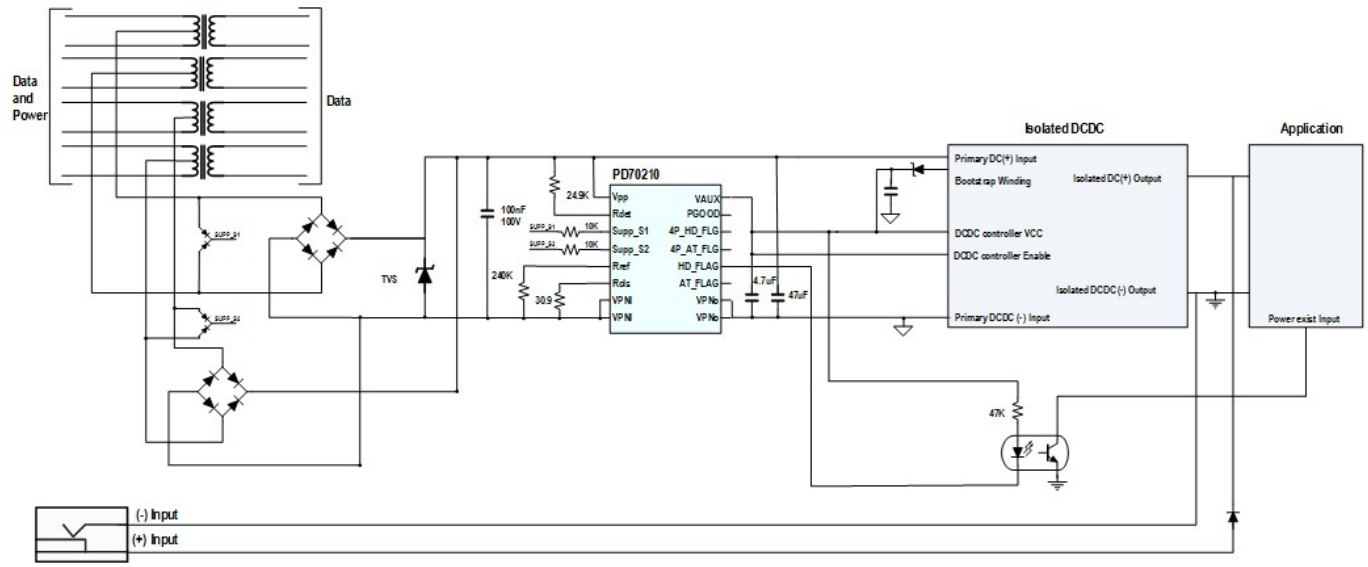


Figure 3-3. Auxiliary Power Connected to Application Supply



General Operation Theory

Event Thresholds

PD ICs switch between different states depending on the voltage between VPP and VPNIN pins.

- VPPVPNIN= 1.3V to 10.1V (rising voltage): Detection resistor RDET is connected between VPP and VPNIN.
- VPPVPNIN= 10.1V to 12.8V (rising voltage): Detection resistor RDET is disconnected from VPNIN.
- VPPVPNIN= 11.4V to 13.7V (rising voltage): Classification current source is connected between VPP and VPNIN. This threshold establishes the programmed current draw set by RCLASS. Current magnitude sets class level per IEEE 802.3at and HDBaseT standards. This function is optional for IEEE 802.3af compliant PDs and mandatory for IEEE 802.3at and HDBaseT compliant PDs. Classification current source remains connected during VPP rising voltage up to 20.9V.
- VPPVPNIN= 20.9V to 23.9V (rising voltage): Classification current source is disconnected. There is some hysteresis between enable and disable thresholds of classification current source.
- VPPVPNIN= 4.9V to 10.1V (falling voltage): This is the mark voltage range. IC will recognize VPPVPNIN voltage falling from classification current source connect threshold to mark threshold as one event of the 2 events classification signature. The number of class to mark level events will cause IC to set the relevant flags to their active low state.
- VPPVPNIN= 36V to 42V (rising voltage): Isolation switch is switched from Off state to Inrush Current Limit (Soft Start) mode. In this mode, the isolation switch limits the DC current to 240 mA (typical). The current limit circuitry during soft start mode monitors the voltage difference across the isolation switch (VPNOUTVPNIN) and maintains inrush current. During inrush current limit internal MOSFET operates in linear mode.
  When VPNOUTVPNIN drops to 0.7V or below, isolation switch inrush current limit is disabled, VAUX is enabled, the isolation switch is fully turned on with 2.2A (maximum) over current protection and relevant flags are asserted after flog delay, which is minimum 80 ms.
- VPPVPNIN= 30.5V to 34.5V (falling voltage): Isolation switch is turned off, establishing high impedance between VPNIN and VPNOUT. Bulk capacitor discharge function is enabled and stays enabled as long as difference between voltages VPP and VPNOUT remains between 30V and 7V. If auxiliary power source is used, its voltage either must be above 34.5V, or an isolation diode has to be added between VPNOUT and the return of auxiliary power source to prevent discharge current flow.
- VPPVPNIN= 2.8V to 4.85V (falling voltage): Detection resistor RDET is reconnected at this threshold. RDET is disconnected when VPPVPNIN voltage drops below 1.1V.

Inrush Current Limit

Inrush current limit is necessary for limiting the current during initial charge-up of bulk capacitors upon system start-up and is required by PoE standards. Large inrush currents can create large voltage sags at PI, which in turn can cause system functions tied to event thresholds (such as AT_FLAG) to reset to their initial states. Soft Start current limit will significantly reduce voltage sag upon start-up.
Start-up into a fully discharged bulk capacitor results in large power dissipation in the isolation switch for a period of time dependent on the size of the bulk capacitance. Maximum initial voltage drop across isolation switch can be about 42V. Maximum power dissipated by the isolation switch decreases as the bulk capacitor charges, eventually decreasing to a normal operating power dissipation when the switch is fully ON. The period of time required to switch from Soft Start mode to normal operation mode can be calculated using the following formula:
T = ((V 0.7) × C) / I
Where:
I= IC’s current during soft start (typically 240 mA)
C= Total input bulk capacitance
V= Initial VPNOUTVPNIN voltage at the beginning of soft start (VMAX = VPP)

Maximum value of bulk capacitor is 240 µF.

Bulk Capacitor Discharge

PD70210/A/AL ICs provide discharge of the application bulk capacitor when VPPVPNIN falling voltage drops below the isolation switch turn-off. This feature ensures that the application bulk capacitance does not discharge through the detection resistor, which can cause detection signature to fail and prevent PSE from starting the PD. While enabled, discharge function provides a minimum controlled discharge current of 22.8 mA, which flows through VPP pin, internally through isolation MOSFET's body diode, and out through VPNOUT pin. Discharge circuitry monitors voltage difference between VPPVPNOUT, and remains active while difference voltage is 7V (VPPVPNOUT) 30V. Use the following equation to calculate maximum time to discharge:
T = ((V 7V) × C)/0.0228
Where:
C= Total input bulk capacitance
V= Initial VPPVPNOUT voltage at isolation switch turn-off
Example: For an initial capacitor voltage of 32V, it takes 240 ms for a 220 µF capacitor to discharge to a 7V level. The discharge operation has a timer and it is active for at least 430 ms.

Auxiliary Voltage–VAUX

All Microchip PD ICs have an available regulated voltage output, VAUX, to be used primarily as a start-up supply for an external DC/DC controller. VAUX is a low current, low duty cycle output, providing current momentarily until an external bootstrap supply can take over. For stable operation connect 4.7 F or greater capacitor between VAUX and power ground pins.
VAUX output is regulated at nominal 10.5V, and supplies a peak current of 10 mA for 10 ms. (5 ms. for PD70200/PD70100). Continuous current is 4 mA for PD7021x and 2 mA for PD7020x/PD7010x. Typically, VAUX output is connected to a bootstrapped supply of higher voltage (such as a rectified auxiliary output from an isolated DC/DC converter transformer). VAUX output does not sink current. Once bootstrapped voltage exceeds VAUX output voltage level, VAUX output will no longer provide current and will be transparent to the operation of the DC-DC converter. It is recommended to design the rectified bootstrapped output under all operating conditions for a minimum output voltage of 12.5V.
During Soft Start mode or when isolation switch turned-off, VAUX output is disabled by falling VPP.

PGOOD Output

PD70210, PD70100, and PD70200 ICs provide an open drain output indicating power good status. This output asserts active low when the voltage between VPP and VPNOUT reaches approximately 40V. Upon assertion, PGOOD output switches to ground with a current sink capability of 5 mA. When VPPVPNIN voltage falls below the isolation switch turn-off threshold, PGOOD output sets back to high impedance state.
This output can be used to detect when PI voltage is in operating range.
PD70210A/AL do not contain PGOOD output. If such functionality is required, VAUX output can be used as an option. If you tie VAUX to the gate of an external small signal N-channel FET, and its source to VPNOUT, the drain of this FET can be used as PGOOD replacement.

WA_EN Input (PD70210A/AL Only)

This input pin is used for external power input connection between VPP and VPNOUT. See Figure 3-1. A resistor divider R1 and R2 is connected between VPP and VPNOUT. These resistors set the P-channel FET turn-on threshold. A 100V low signal P-ch FET gate and source must be connected to R1. The P-ch drain is connected to WA_EN input through R3 resistor. R4 resistor is connected between WA_EN and VPNIN. R3 and R4 set the level in which a valid WA input is detected. WA_EN input requires a standard logic level. When WA_EN input is high, the PD70210A/AL isolation switch is turned OFF and all the flags are asserted–changed to low level. The resistor selection guide is specified in application note AN3472: Auxiliary Power for PDs.

SUPP_S1 and SUPP_S2 Inputs (PD70210A/AL Only)

SUPP_S1 and SUPP_S2 inputs enable the PD to recognize the source of the power whether it is data, spare pairs, or both. Each of these inputs requires a common cathode dual diode to be connected to the relevant pair, if

the PD device samples a high level of 35V and above in this input it counts this pair as an active pair. These inputs are used when working with special PSE which having detection and classification on two pair only but having the power in all four pairs. SUPP_S1 and SUPP_S2 inputs must have 10 k resistor connected in serial to each of them. When these functions are not used, the SUPP_S1 and SUPP_S2 pins can be disconnected from external circuits and connected to VPNIN input or left floating.

PSE Type Flag Outputs

The PD702x0 and PD701x0 ICs provide an open drain outputs indicating the PSE type by its detected Classification pattern. The output is in a high impedance state until the isolation switch moves from Soft Start Current Limit mode to normal operation mode. It will then be asserted low, depending on the classification pattern that was recognized. Upon assertion, flags output switches to ground with a current sink capability of 5 mA. Flags output signals switch back to high impedance state when VPPVPNIN voltage falls below isolation switch turn-off threshold. The flags enable the PD designer to work with the flag that is relevant to the application. For each power that is detected, all of the lower power flags are also asserted (IE AT_FLAG is asserted AT level and for all power levels above AT). The available power level is specified in Table 2. As specified in the table, the PD counts the classification fingers event and by its count recognize the PSE type. SUPP_S1 and SUPP_S2 enable the PD to recognize a special AT level PSE which having the classification on two pair only but having the power in all four pairs. Therefore, if two fingers are recognized, then the PD device samples SUPP_S1 and SUPP_S2 inputs and if both are high, then the power is supplied to the four pairs and 4P_AT flag is asserted.

Table 5-1. Available PD Power Level and Flag Indication

Number of Class Fingers	SUPP_S1	SUPP_S2	PGOOD_FLAG	AT_FLAG	HD_FLAG	4P_AT_FLAG	4P_HD_FLAG	Available Power Level
1	X	X	0 V	Hi Z	Hi Z	Hi Z	Hi Z	802.3 AF level/ 802.3 AT Type 1 level
2	H	L	0 V	0 V	Hi Z	Hi Z	Hi Z	802.3 AT Type 2 level
2	L	H	0 V	0 V	Hi Z	Hi Z	Hi Z	802.3 AT Type 2 level
2	H	H	0 V	0 V	Hi Z	0 V	Hi Z	Dual 802.3 AT Type 2 level
3	L	H	0 V	0 V	0 V	Hi Z	Hi Z	HDBaseT Type 3 level
3	H	L	0 V	0 V	0 V	Hi Z	Hi Z	HDBaseT Type 3 level
3	H	H	0 V	0 V	0 V	0 V	Hi Z	HDBaseT Type 3 level
4	X	X	0 V	0 V	0 V	0 V	Hi Z	Dual 802.3 AT Type 2 level
5	X	X	RESERVED FOR FUTURE					NA
6	X	X	0 V	0 V	0 V	0 V	0 V	Twin HDBaseT Type 3 level

Thermal Protection

The PD702x0 and PD701x0 ICs provide thermal protection. Integrated thermal sensors monitor the internal temperatures of the isolation switch and classification current source. If the over-temperature threshold of either sensor is exceeded, that sensor's respective circuit will disable.
To ensure trouble free operation, it is important to make sure PD IC's exposed pad is mounted to a copper area on the PCB that provides an adequate heat sink.

PCB Layout Guidelines

IEEE 802.3at and HDBaseT standards specify certain isolation requirements which must be met by all PoE equipment. Isolation is specified at 1500 VRMS minimum between incoming data and power lines, and any signal, power, or chassis connection that can come into contact by the end user outside the application. On a typical FR4 PCB, this requirement is generally satisfied by creating an isolation barrier of a minimum 0.080 inch (2 mm) between adjacent traces requiring 1500 VRMS isolation.

Give the PCB design special attention to provide adequate heat sinking of the exposed pad (VPNOUT). All Microchip PD IC packages utilize the exposed pad to provide thermal cooling of the package, and as such requires PCB design to include sufficient copper area attached to the exposed pad. For multilayer boards, conductive vias to an adjacent plane layer can be used. Keep in mind that exposed pad is electrically connected to VPNIN and must be electrically isolated from VPNOUT.

When using vias to provide thermal conductivity between a plane layer and exposed pad, barrels must be 12 mils in diameter and (where possible) placed in a grid pattern. Barrel holes must be plugged or tented for proper solder paste release. When tented holes are used, solder mask inclusion area must be 4 mils (0.1 mm) larger than via barrel.

For single or dual layer boards, use large copper fills in direct contact with the exposed pad. Copper thickness of 2 oz improves thermal performance. If using copper traces of less than 2 oz, it is recommended to increase overall trace thickness by adding excess solder to trace areas where appropriate.

PCB design must provide wide, heavy copper traces for high current power lines. A 4-pair, extended-power PD can have maximum trace currents of 2A for the VPP and VPN terminals. Traces carrying current for VPP, VPNIN, and VPNOUT must be sized to provide the lowest temperature rise practical at the maximum current. For example, a minimum of 15 mils wide 2 oz copper accommodates up to 1.6A current with a maximum 10 °C temperature rise. If copper traces of less than 2 oz are used, increase the minimum width to accommodate maximum current with lowest temperature rise.

PoE signals contain voltages up to 57 VDC. Component working voltage must be considered, and components sized accordingly. Surface mount resistors are a good example: 0402 resistors have typical maximum working voltage specifications of 50V, whereas 0805 resistors are typically specified at 150V.

When used with the PD702x0 and PD701x0 ICs, the detection resistor RDET is only connected at PoE voltages up to 12.8V, and is disconnected otherwise, so it can be a low voltage type (0402).

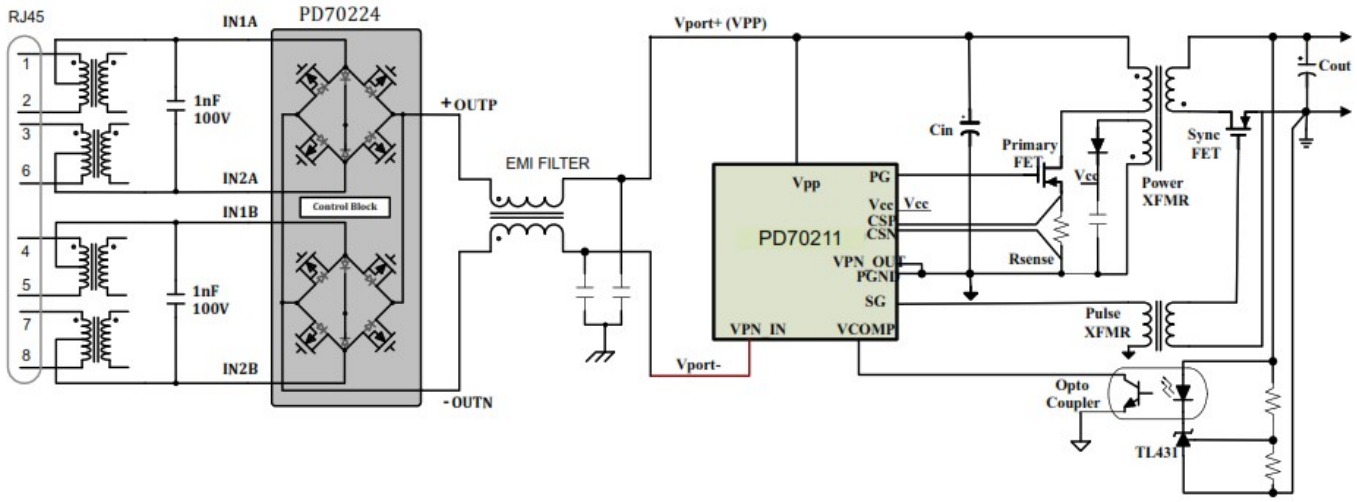
Note: For detailed layout guidelines, see Microchip Application Note AN3533.

EMI Considerations

To minimize conducted and radiated emission, and to “break” possible ground loops, it is recommended to place (or to leave provisions for) an EMI filter. This filter is typically placed between input rectifier bridge and PoE PD controller and includes a common mode choke and 2 kV common-mode capacitors, as shown in the following figure. An example of a practical implementation of such a filter is provided in PD7211EVB72FW-12 Evaluation Board User Guide. In that example, the following components are used in the filter:

- Common mode choke Pulse pan P0351
- Common mode capacitors Novice pan 1812B682J202NXT

Figure 8-1. Power Flow in a Typical PD70211-Based System



Reference Documents

All Microchip documentation is available online at www.microchip.com/poe.

- IEEE 802.3at-2015 standard, Section 33 (DTE Power via MDI)
- HDBaseT Specification
- PD70210/PD70210A/PD70210AL data sheet
- PD70211 data sheet
- PD70100/PD70200 data sheet
- PD70101/PD70201 data sheet
- PD70224 data sheet
- AN3410 Design for PD System Surge Immunity PD701xx_PD702xx
- AN3472 Implementing Auxiliary Power in PoE
- AN3471 Designing a Type 1/2 802.3 or HDBaseT Type 3 PD Front End Using PD702x1 and PD701x1 ICs
- AN3533 PD70210(A), PD70211 System Layout Guidelines

Revision History

Revision	Date	Description
B	04/2022	The following is the summary of changes made in this revision: • Updated Table 1. • Updated 7. PCB Layout Guidelines: Removed mentions of 0603 resistors. Added t he note. • Added 8. EMI Considerations. • Updated 9. Reference Documents.
A	06/2020	This is the initial issue of this document. Designing a Type1/2 802.3 or HDBaseT Typ e 3 Powered Device Front End Using PD702x0 and PD701x0 ICs was previously described in the following documents: • AN209: Designing a Type 1/2 802.3 or HDBT Type 3 PD Using PD70210/ PD70210 A ICs • AN193: Designing a Type 1/2 IEEE 802.3at/af Powered Device Front End Using PD 70100/PD70200

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Documents / Resources

	MICROCHIP AN3468 HDBaseT Type 3 Powered Device Front-End [pdf] Owner's Manual AN3468 HDBaseT Type 3 Powered Device Front-End, AN3468, HDBaseT Type 3 Powered Device Front-End, Powered Device Front-End, Front-End

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