MERRY HSN-M01BTM HyperX Embedded Wireless Module User Guide

Contents

MERRY HSN-M01BTM HyperX Embedded Wireless Module

Specifications

- **Model No.:** HSN-M01BTM
- **Part No.:** 89M131001001
- **Revision:** C

Product Information
This HyperX Embedded Wireless Module, model HSN-M01BTM, is designed to provide wireless connectivity for various devices.

Product Usage Instructions

Installation

1. Ensure your device is powered off before installing the module.
2. Locate the appropriate slot for the module.
3. Gently insert the module into the slot, ensuring proper alignment.
4. Secure the module in place according to the device's instructions.

Configuration
Once the module is installed, refer to the device's settings menu to configure wireless connectivity with the module.

Maintenance
Regularly check for software updates for the module to ensure optimal performance.

GENERAL PRODUCT SPECIFICATION FOR DEVICE

Product part number list – Merry (TBD)

ITEM	MODEL NO.	PART NO.	SHIP PLACE	TYPE
1	MX-131-001-01	89M131001001		

SCOPE
SCOPE this specification is intended to define the requirements for a Bluetooth module. The Bluetooth shall support V5.3, and mandatory features of V5 mandatory features and be backward-compatible with legacy versions.

FEATURES

Host processor subsystem

- ARM® Cortex®-M4 (CM4) with Floating Point Unit (FPU) application processor.
- Supports Memory Protection Unit (MPU).
- Supports Nested Vectored Interrupt Controller (NVIC) with 37 interrupt sources each with up to 16 levels of priority.
- Support Serial Wire Debug (SWD, 2 pins) and JTAG (5 pins) debug interface.
- Support breakpoints, watchpoints, stepping, vector catching, data matching. Complete debug features.
- 224KB Tightly Couple Memory (TCM) with zero wait state can be operated at CPU speed. Among them, 32KB can be programmed as L1 cache.
- Configurable L1 cache size: 32KB, 16KB, 8KB or 0KB, shared with TCM.
- Execute In Place (XIP) on flash memory.
- Wireless connectivity
- Compact design
- High-speed data transfer
- Easy integration

DSP processor subsystem

- Cadence® HiFi Mini ® Audio Engine DSP coprocessor with HiFi EP® extension
- 7-stage pipeline
- Maximum speed: 416MHz, and recommended speed: 399MHz to minimize de-sense
- Support Memory Management Unit (MMU) for memory protection with translation

- 32 maskable interrupts with 4 priority levels and a NMI (non-maskable Interrupt)
- 32KB instruction cache and 16kB data cache with high hit rate and zero wait state
- 256KB instruction RAM with zero wait state
- 512KB data RAM with zero wait state and two memory banks to increase co-access performance
- 432KB data ROM with zero wait state

Memory summary

- On-die memories (SRAMs) with up to 224KB at CPU clock speed with zero wait state.
- Low latency 640KB system RAM (SYSRAM) with maximum speed 208MHz (LPOSC)
- System in Package (SiP) 32Mb low-power flash memory with 0.1µA deep-down current (typical condition) and maximum speed 104MHz (LPOSC)

Platform

- Dynamic Voltage Scaling (DVS) on core power from 0.8 Volt to 0.9 Volt
- Two general DMA channels
- RTC timer
- Nine general purpose timers (GPT s)
- Watchdog timer (WDT)
- Crypto engine for AES/SHA1/SHA224/SHA256
- True random number generator
- Ambient temperature from -40°C to 85°C

Peripheral

- Two I2C interfaces up to 3.4MHz
- Two UART interfaces up to 26Mbps
- One SPI master interfaces up to 52MHz
- Five PWM channels
- 12-bit AUXADC channels

Connectivity (Bluetooth) features overview

- ULL Module offers a highly integrated Bluetooth radio and baseband processor.
- ULL Module is fully compliant with Bluetooth version 5.3. It is upgradable to later versions, including BR/EDR and Bluetooth LE1M/2M and offers enhanced data rates of up to 3Mbps.

Bluetooth RF

- Fully compliant with Bluetooth core specification 5.3.
- Low-IF architecture with high degree of linearity and high order channel filter.
- Integrated T/R switch and balun.
- Fully integrated PA provides 10dBm output power

- -96dBm sensitivity with interference rejection performance
- Hardware AGC dynamically adjusts the receiver performance in changing environments.

Bluetooth baseband

- Bluetooth specification V5.3 + dual mode + isochronous channel
- Up to four simultaneous active ACL links.
- Up to four simuacltaneous active Bluetooth LE links.
- Support for single SCO or eSCO link with CVSD/mSBC coding.
- Support for BLE1M/2M
- Up to simultaneous active ICO/ICL links (ICO+ICL links=4)
- Support for AWS (Advanced Wireless Stereo) for two headsets (Speaker1 and Speaker2) sync with phone and play audio at the same time
- AFH and PTA collaborative support for WLAN/Bluetooth coexistence.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission.
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption.
- Channel quality driven data rate adaptation.
- Channel assessment for AFH.

Power management unit (PMU) features overview

- Input range: 4.5V ~ 5.5V
- One SIDO regulator
- One Buck regulator
- Two LDO regulators

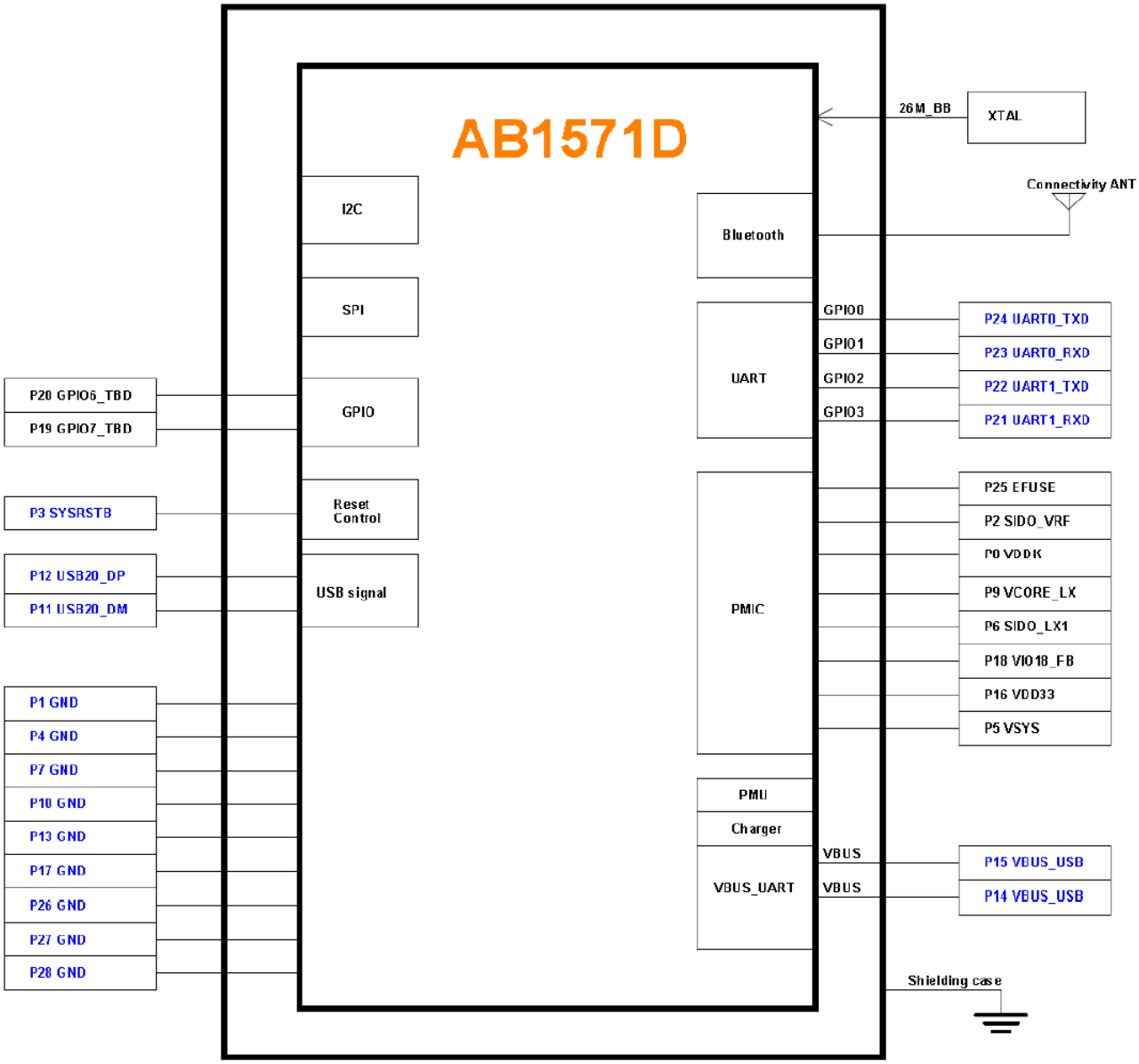
Compact size with

- (L) 14 x (W) 12 x (H) 2.1 mm.

INTRODUCTION

ULL module is a highly integrated System-in-Package (SiP) low-power Bluetooth chipset with an application processor, one digital signal processor (DSP), a Bluetooth transceiver, a power management unit (PMU), a 4MB flash. ULL module contains AB1571D chipset, ARM® Cortex®-M4F application processor that can operate in a range of frequencies between 1MHz up and 208MHz and achieve high performance and power efficiency with Level-one cache (L1 cache). The DSP subsystem is based on Cadence® HiFi Mini®Audio Engine DSPs integrated with total 768kB zero-latency memory, 32kB L1 cache and flexible frequency from 2MHz up to 416MHz. The Bluetooth subsystem contains RF and baseband circuits that are fully compliant with Bluetooth core specification 5.3. The PMU contains high power efficiency DC-to-DC buck converters and ultra-low quiescent current Low Dropout linear regulators (LDO) to provide a stable power source for the internal and external devices. The SiP package technology combine the main die, flash and PMU. This significantly reduces the product size and provides more features in the same space.

Block Diagram



AB1571D System architecture

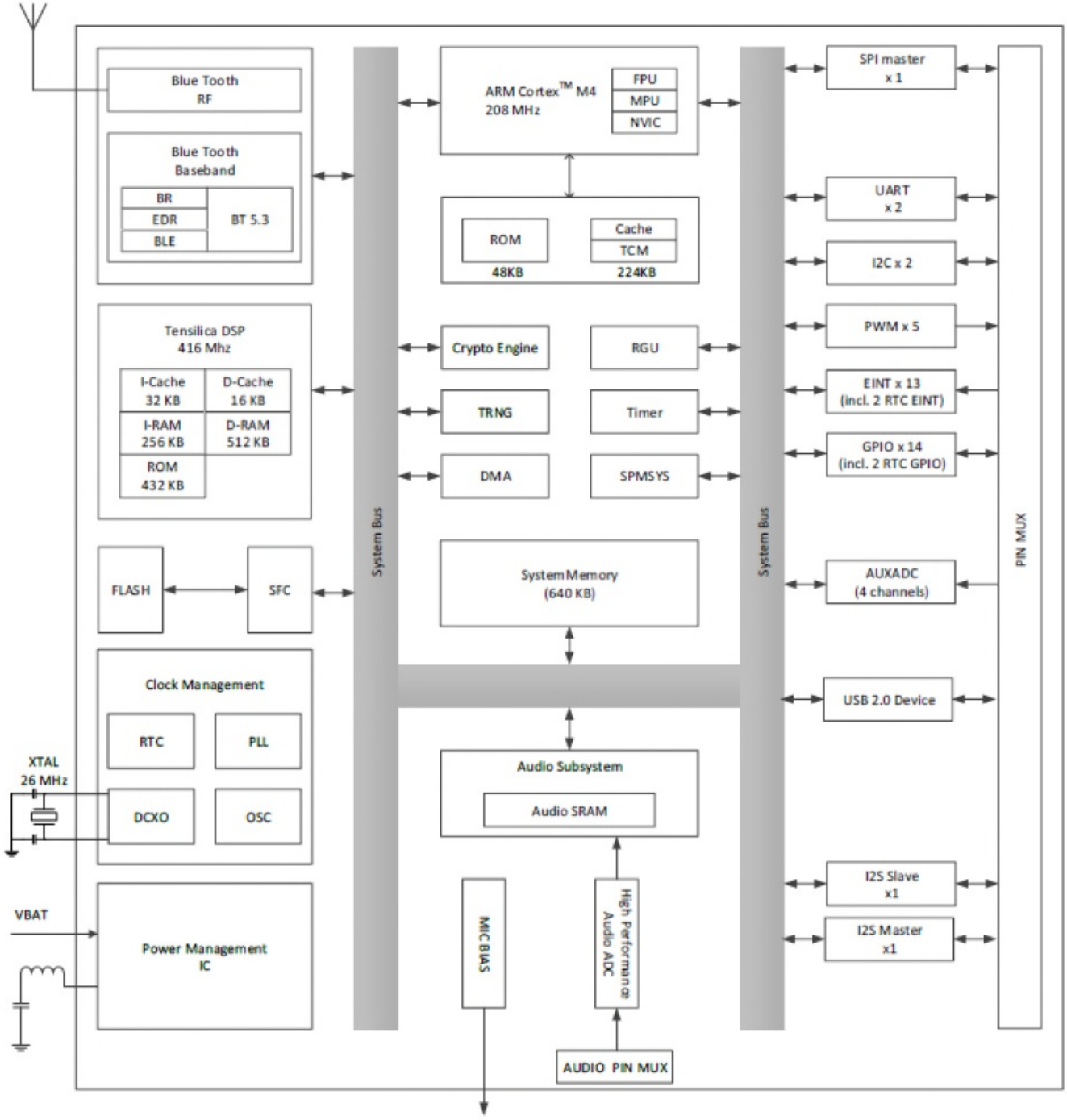


Figure 4.2-1 AB1571D chipset architecture

AB1571D Schematic

Schematic design notice of "18_AB1671_Main_Chip" page.

Note 11-1: Buck inductors and capacitors should be close to IC.

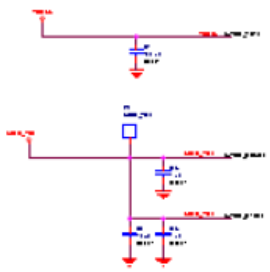
Note 11-2: VSYS pin cap = 22uF if IC Vi> 4.3V
VSYS pin cap = 10uF if IC Vi<= 4.3V

Note 60-1: The crystal should be close to IC.

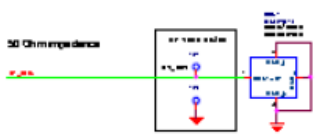
Note 2-1 Add LDO , 0.1 and change VBUS cap to 4.7uF
to solve USB hub Vbus drop-out issue
D1002:Vf< 1V, If> 150mA

Note 2-2 Modify VDIG18 cap to 2.2uF

RF_VDD



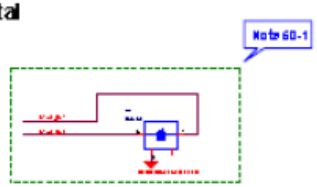
RFIO

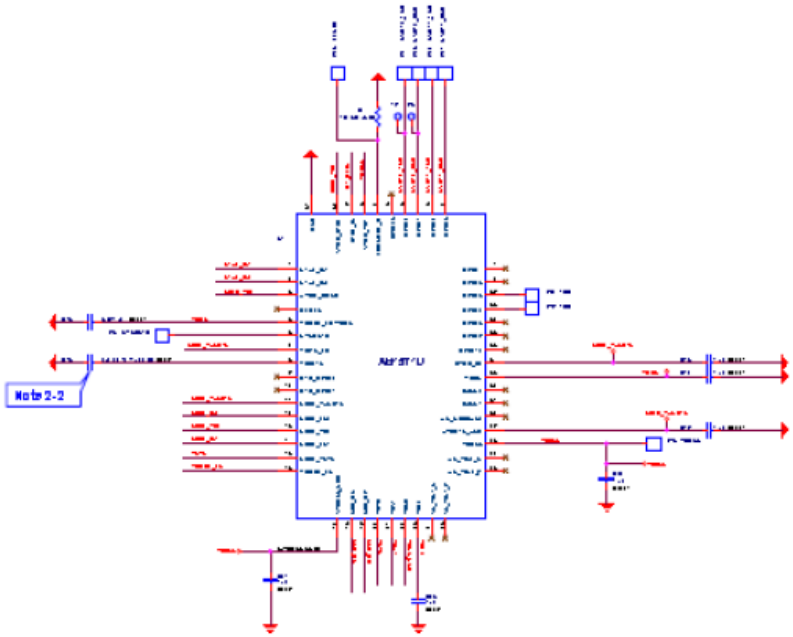


Reference GPIO Pinmux

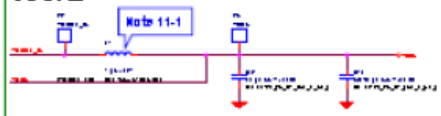
GPIO 0: UART0_TXD
GPIO 1: UART0_RXD
GPIO 2: UART1_TXD
GPIO 3: UART1_RXD
GPIO 4: I2C1_SCL
GPIO 5: I2C1_SDA
GPIO 6: TBD
GPIO 7: TBD
GPIO 8:
GPIO 10:
GPIO 23

Crystal

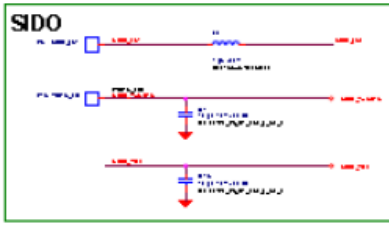




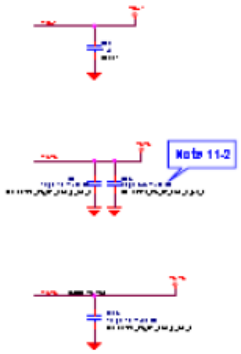
VCORE

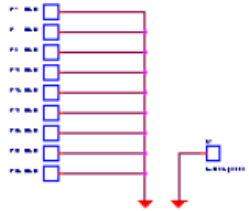


SIDO



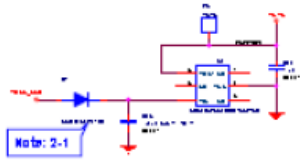
VBAT_and_VSYS





USB / VBUS

LDO Without discharge Function



Board Dimensions and Mechanical Interfaces

- Module length: 14 mm
- Module width: 12 mm
- PCB Thickness: 0.4 mm
- Total height components + PCB: 2.1 mm
- Deform Standard: <=0.138mm (<= 0.75% of the longest diagonal)

Top side with antenna connector positions

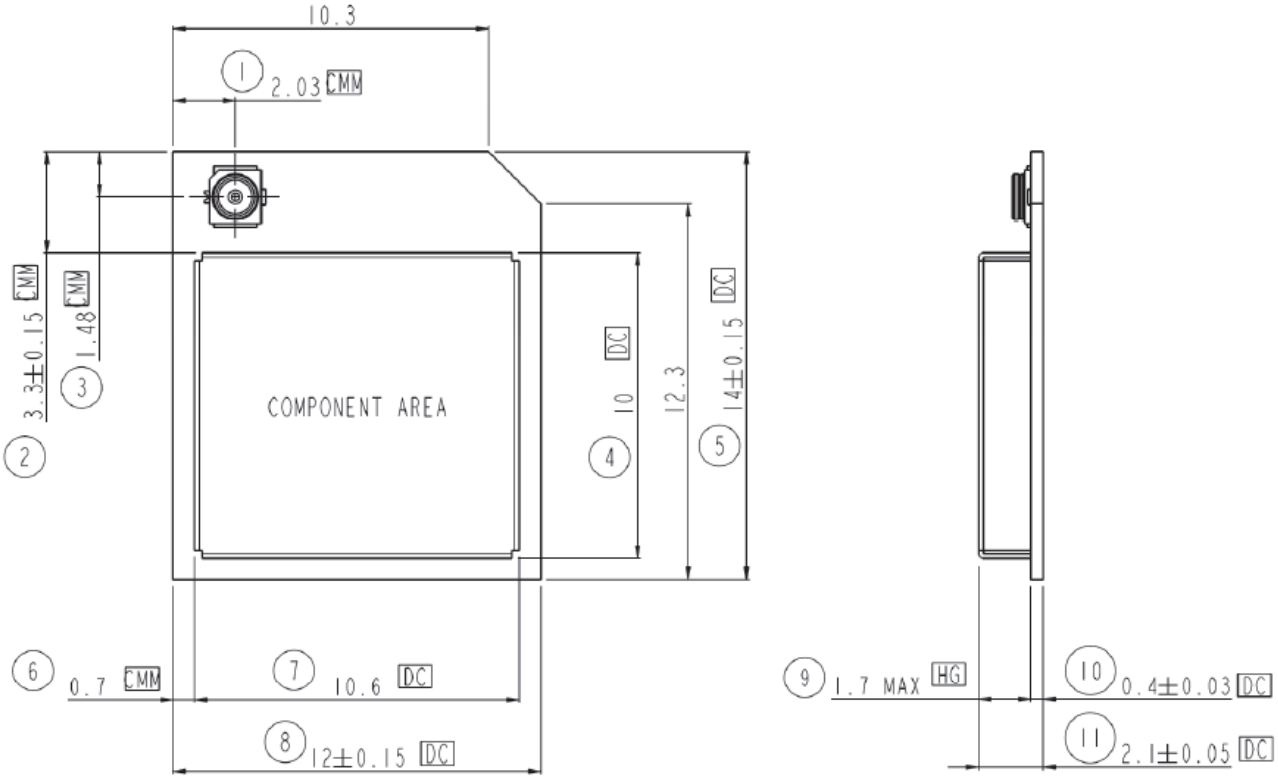


Figure 4.4-1 Dimensions and board assembly, top side

Bottom side

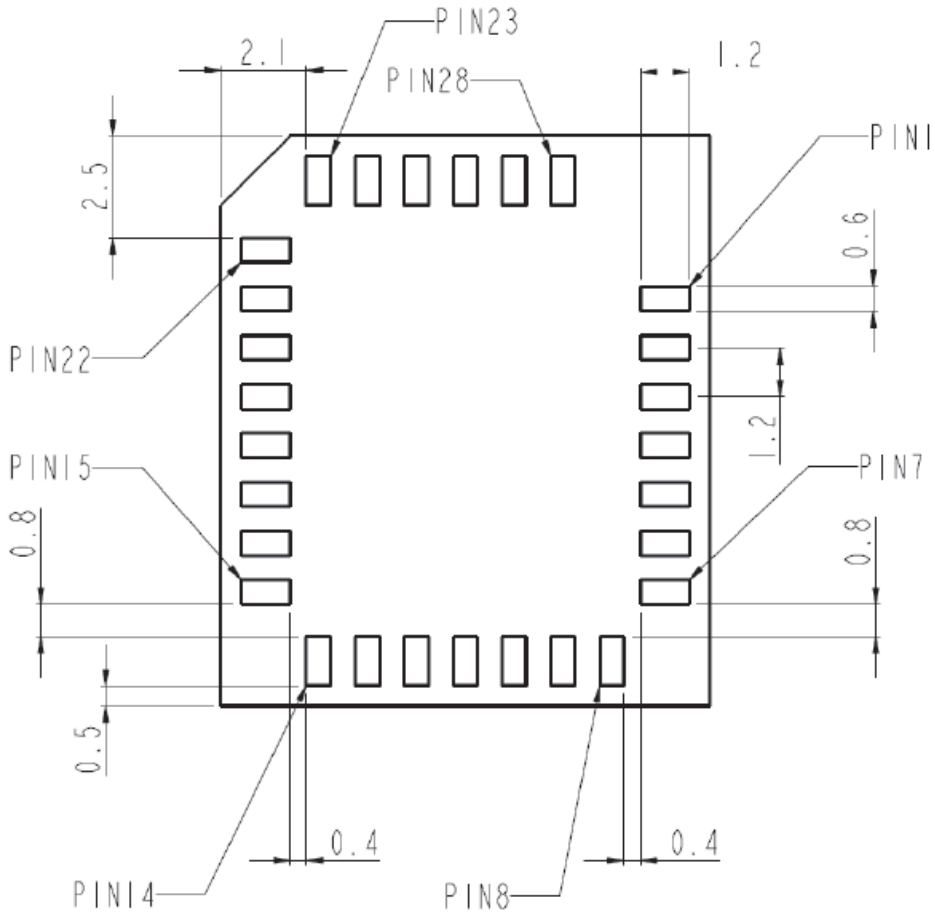


Figure 4.5-1 Module footprint for assembly on a carrier board

Pin Definition

Table 4.7-1. PIN DESCRIPTION*

PIN NUMBER	PIN NAME	PIN DESCRIPTION
P1	GND	Ground
P2	SIDO_VRF	VRF output voltage
P3	SYSRSTB	SYSRSTB Button
P4	GND	Ground
P5	VSYS	System Load Connection Connect VSYS to System Load
P6	SIDO_LX1	SW node of SIDO
P7	GND	Ground
P8	VDDK	Core Power
P9	VCORE_LX	SW node of VCORE
P10	GND	Ground
P11	USB20_DM	USB Signal DM
P12	USB20_DP	USB Signal DP
P13	GND	Ground
P14	VBUS_USB	Charger_Power_Input
P15	VBUS_USB	Charger_Power_Input
P16	VDD33	VLDO33_Output_Voltage
P17	GND	Ground
P18	VIO18_FB	BUCK VIO18 Feedback Pin
P19	GPIO7_TBD	General Purpose Input/Output
P20	GPIO6_TBD	General Purpose Input/Output
P21	UART1_RXD	Download Interface
P22	UART1_TXD	Download Interface
P23	UART0_RXD	Download Interface
P24	UART0_TXD	Download Interface
P25	eFUSE	Efuse power source
P26	GND	Ground
P27	GND	Ground
P28	GND	Ground

***Note:** Any adjustment or modification must be aligned with HP and receive the confirmation from HP before implementation

ELECTRICAL CHARACTERISTICS

The module operates at specific voltage and current levels as outlined in the electrical characteristics section of the manual.

Absolute maximum ratings – AB1571D

Table 5.1-1. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
AVDD_BTRF	BT RF1 supply	-0.5	1.18	V
AVDD_VBT	BT RF2 supply	-0.5	3.5	V
VBUS	VBUS from USB connector	-0.5	6.0	V
VSYS	System load connection. Connect VSYS to system lo ad.	-0.5	5	V
AVDD18_AUD	1.8V power	0	2.0	V
VDDK	Digital core power	-0.3	0.99	V

Table 5.1-2. Absolute maximum ratings for I/O power supply

Symbol or pin name	Description	Min.	Typ.1	Max.	Unit
DVDD_IO	Power supply for GPIO group 0	1.62	1.8	1.98	V

Table 5.1-3. Absolute maximum ratings for voltage input

Symbol or pin name	Description	Min.	Max.	Unit
VIN0	Digital input voltage for IO Type 0	-0.3	3.63	V
VIN1	Digital input voltage for IO Type 1	-0.3	3.63	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.63	V

Table 5.1-4. Absolute maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	°C

Operating conditions

General operating conditions

Table 5.2-1. AB1571D general operating conditions

Item	Description	Condition	Min.	Typ.	Max.	Unit
FCPU	Internal Cortex-M4 clock (including its cache and TCM)	VCORE = 0.8V	0	–	104	MHz
		VCORE = 0.9V	0	–	208	MHz
FDSP	Internal DSP clock (including DSP instruction RAM, data RAM and cache). Synchronous with FCPU.	VCORE = 0.8V	0	–	208	MHz
		VCORE = 0.9V	0	–	416	MHz
FBUS	Internal system memory and system bus clock. Synchronous with FCPU.	VCORE = 0.8V	0	–	104	MHz
		VCORE = 0.9V	0	–	208	MHz
FSFC	Internal SFC clock. Asynchronous with FCPU.	VCORE = 0 . 8 V , 0.9V	0	–	104	MHz

Table 5.2-2. AB1571D Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD_BTRF	BT RF1 supply	1.05	1.1	1.15	V
AVDD_VBT	BT RF2 supply	2.9	3.3	3.5	V
VBUS	VBUS from USB connector	4.5**(TBD)**	–	5.5**(TBD)**	V
VSYS	System load connection. Connect VSYS to system load. For preventing EOS, the resistance of system load should be always larger than 2.1ohm.	3.0	3.7-	5.0	V
AVDD18_AUD	Audio 1.8V power	1.68	1.8	1.95	V
VDDK	Digital core power (LV)	0.72	0.8	0.88	V
	Digital core power (HV)	0.81	0.9	0.99	V

Table 5.2-3. AB1571D Recommended operating conditions for voltage input

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN0	Digital input voltage for IO Type 0	0	–	DVDIO	V
VIN1	Digital input voltage for IO Type 1	0	–	DVDIO	V
VIN2	Digital input voltage for IO Type 2	0	–	DVDIO	V

Table 5.2-4. AB1571D Recommended operating conditions for operating temperature

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
Tc	Operating temperature	-40	–	85	°C

Input or output port characteristics

Table 5.2-5. AB1571D Electrical characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH0	Digital high input current for IO Type 0	PU/PD disabled DVDIO = 1.8V, DVDIO*0.65 < VIN0 <DVDIO+0.3V	-5	–	5	μA
		PU enabled	-40	–	5	μA
		DVDIO = 1.8V, DVDIO*0.75 < VIN0 < DVDIO				
		PD enabled DVDIO = 1.8V, DVDIO*0.75 < VIN0 < DVDIO	7	–	80	μA
DIIL0	Digital low input current for IO Type 0	PU/PD disabled DVDIO = 1.8V,-0.3V < VIN0 < DVDIO*0.35	-10	–	5	μA
		PU enabled, DVDIO = 1.8V0 < VIN0 < DVDIO*0.25	-70	–	-6	μA
		PD enabled, DVDIO = 1.8V0 < VIN0 < DVDIO*0.25	-5	–	40	μA
DIOH0	Digital high output current for IO Type 0	DVOH = 1.53V DVDIO = 1.8VMax. driving mode	8	–	–	mA
DIOL0	Digital low output current for IO Type 0	DVOL = 0.27VDVDIO = 1.8VMax. driving mode	8	–	–	mA
DRPU0	Digital I/O pull-up resistance for IO Type 0	DVDIO = 1.8VVIN0 = 0V	70	150	380	kΩ
DRPD0	Digital I/O pull-down resistance for IO Type 0	DVDIO = 1.8VVIN0 = 1.8V	70	150	380	kΩ
DVOH0	Digital output high voltage for IO Type 0	DVDIO = 1.8V	0.85*D VDIO	–	–	V
DVOL0	Digital output low voltage for IO Type 0	DVDIO = 1.8V	–	–	0.15*DVDIO	V
VIH0	Digital input high voltage for IO Type 0	DVDIO = 1.8V	0.75*DVDIO		DVDIO+0.3	

VIL0	Digital input low voltage for IO Type 0	DVDIO = 1.8V	-0.3		0.25*DVDIO	
DIIH1	Digital high input current for IO Type 1	PU/PD disabled DVDIO = 1.8V,DVDIO*0.65 < VIN2 < DVDIO+0.3V	-5	–	5	μA
		PU enabled, RSEL1 DVDIO = 1.8VDVDIO*0.75 < VIN2 < DVDIO	-40	–	5	μA
		PU enabled, RSEL2 DVDIO = 1.8VDVDIO*0.75 < VIN2 < DVDIO	-120	–	5	μA
		PD enabled, RSEL1 DVDIO = 1.8VDVDIO*0.75 < VIN2 < DVDIO	10	–	140	μA
		PD enabled, RSEL2 DVDIO = 1.8VDVDIO*0.75 < VIN2 < DVDIO	10	–	140	μA
DIIL1	Digital low input current for IO Type 1	PU/PD disabled, DVDIO = 1.8V,-0.3V < VIN2 < DVDIO*0.35	-10	–	5	μA
		PU enabled, RSEL1 DVDIO = 1.8V0 < VIN2 < DVDIO*0.25	-100	–	-15	μA
		PU enabled, RSEL2 DVDIO = 1.8V0 < VIN2 < DVDIO*0.25	-450	–	-60	μA
		PD enabled, RSEL1 DVDIO = 1.8V0 < VIN2 < DVDIO*0.25	-5	–	40	μA
		PD enabled, RSEL2 DVDIO = 1.8V0 < VIN2 < DVDIO*0.25	-5	–	40	μA
DIOH1	Digital high output current for IO Type 1	DVOH = 1.53VDVDIO = 1.8VMax. driving mode	8	–	–	mA

DIOL1	Digital low output current for IO Type 1	DVOL = 0.27VDVDIO = 1.8VMax. driving mode	8	–	–	mA
;DRPU1	Digital I/O pull-up resistance for IO Type 1RSEL1 :(GPIO_R1, GPIO_R0) = (0,1) RSEL2 : (GPIO_R1,GPIO_R0) = (1, 0)	DVDIO = 1.8V VIN2 = 0V, RSEL1	64	100	161	kΩ
		DVDIO = 1.8V VIN2 = 0V, RSEL2	14.5	21	35	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1RSEL1 :(GPIO_R1, GPIO_R0) = (0,1) RSEL2 :(GPIO_R1, GPIO_R0) = (1, 0)	DVDIO = 1.8V VIN2 = 1.8V, RSEL1	57	120	221	kΩ
		DVDIO = 1.8V VIN2 = 1.8V, RSEL2	577	120	221	kΩ
DVOH1	Digital output high voltage for IO Type 1	DVDIO = 1.8V	0.85*D VDD	–	–	V
DVOL1	Digital output low voltage for IO Type 1	DVDIO = 1.8V	–	–	0.15*DVDIO	V
VIH1	Digital input high voltage for IO Type 1	DVDIO = 1.8V	0.75*D VDIO		DVDIO+0.3	
VIL1	Digital input low voltage for IO Type 1	DVDIO = 1.8V	-0.3		0.25*DVDIO	
DIIH2	Digital high input current for IO Type 2	PU/PD disabled DVDIO = 1.8V, DVDIO*0.65 < VIN3 <DVDIO+0.3V	-5	–	5	µA

		PU enabled DVDIO = 1.8V,DVDIO*0.75 < VIN3 <DVDIO	-40		5	μA
		PD enabled DVDIO = 1.8V,DVDIO*0.75 < VIN3 <DVDIO	7		80	μA
DIIL2	Digital low input current for IO Type 2	PU/PD disabled DVDIO = 1.8V,-0.3V < VIN3 <DVDIO*0.35	-10	–	5	μA
		PU enabled DVDIO = 1.8V,0 < VIN3 < DVDIO*0.25	-70	–	-6	μA
		PD enabled DVDIO =1.8V,0 < VIN3 < DVDIO*0.25	-5	–	40	μA
DIOH2	Digital high output current for IO Type 2	DVOH = 1.53VDVDIO = 1.8VMax. driving mode	8	–	–	mA
DIOL2	Digital low output current for IO Type 2	DVOL = 0.27VDVDIO = 1.8VMax. driving mode	8	–	–	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	DVDIO = 1.8VVIN3 = 0V	70	150	380	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	DVDIO = 1.8VVIN3 = 1.8V	70	150	380	kΩ
DVOH2	Digital output high voltage for IO Type 2	DVDIO = 1.8V	0.85*D VDD	–	–	V
DVOL2	Digital output low voltage for	DVDIO = 1.8V	–	–	0.15*DVDIO	V

	IO Type 2					
VIH2	Digital input high voltage for IO Type 2	DVDIO = 1.8V	0.75*D VDIO		DVDIO+0.3	
VIL2	Digital input low voltage for IO Type 2	DVDIO = 1.8V	-0.3		0.25*DVDIO	

USB2.0 characteristics

USB2.0 high-speed device controller

USB20 controller support HS (480M)/FS(12M) is configured for supporting two endpoints to receive packets and four endpoints to send packets except for endpoint 0. These endpoints can be individually configured in the software to manage either Bulk transfers, Interrupt transfers or Isochronous transfers. There are four DMA channels and the embedded RAM size is configurable size up to 3264 bytes. The embedded RAM can be dynamically configured to each end point.

Feature list	Description
Speed	HS(480M)/FS(12M)
Enhanced feature	Generic Device
Endpoint	4 Tx 2 Rx
DMA channel	4
Embedded RAM	3264

USB20 interface characteristics

FS/LS mode

- The USB uses a differential output driver to drive the USB data signal on the USB cable. The static output swing of the driver in its low state must be below VOL (max) of 0.3V with a 1.5kΩ load to 3.6V and in its high state must be above the VOH (min) of 2.8V with a 15kΩ load to ground

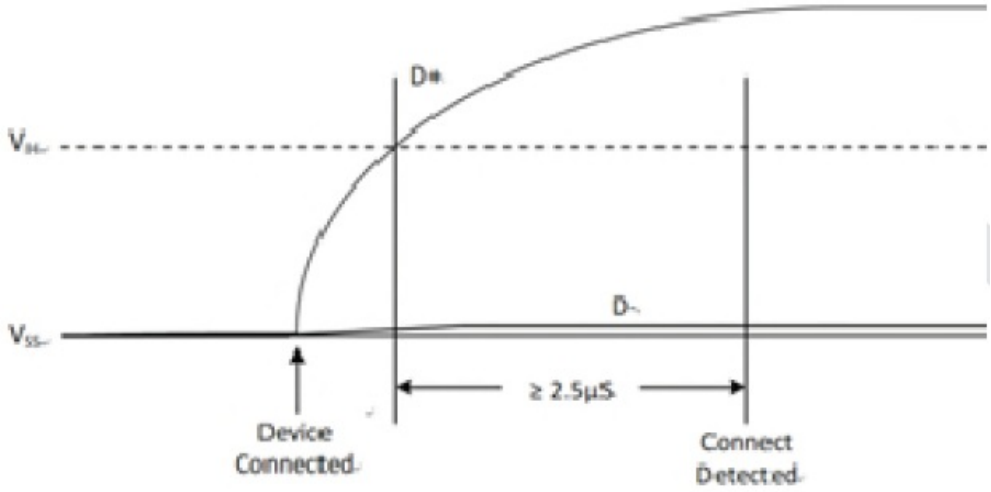


Figure 5.3-1. Full-speed Device Connect Detection

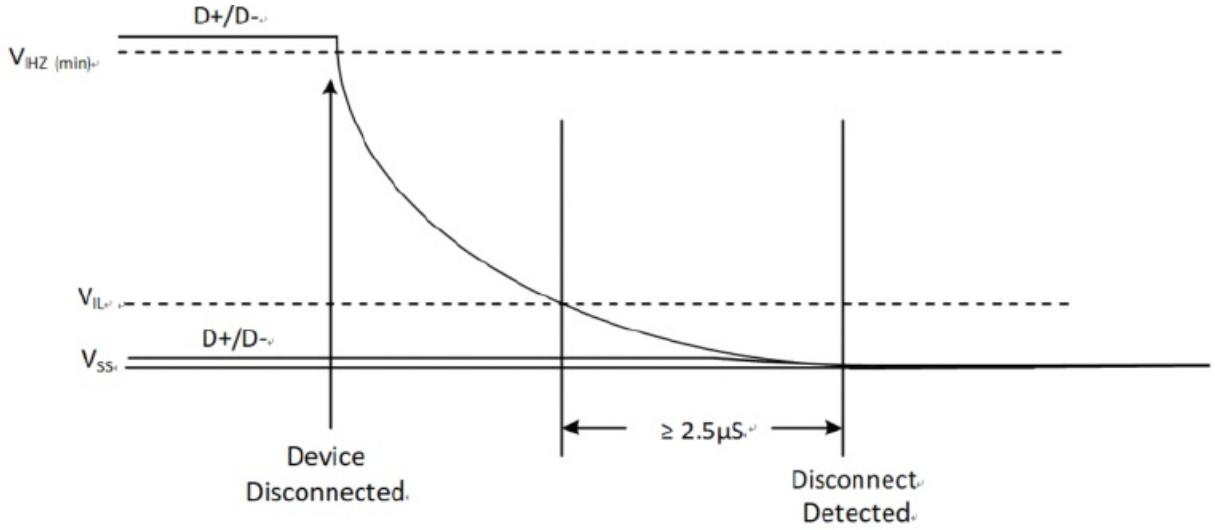


Figure 5.3-2. Disconnect Detection

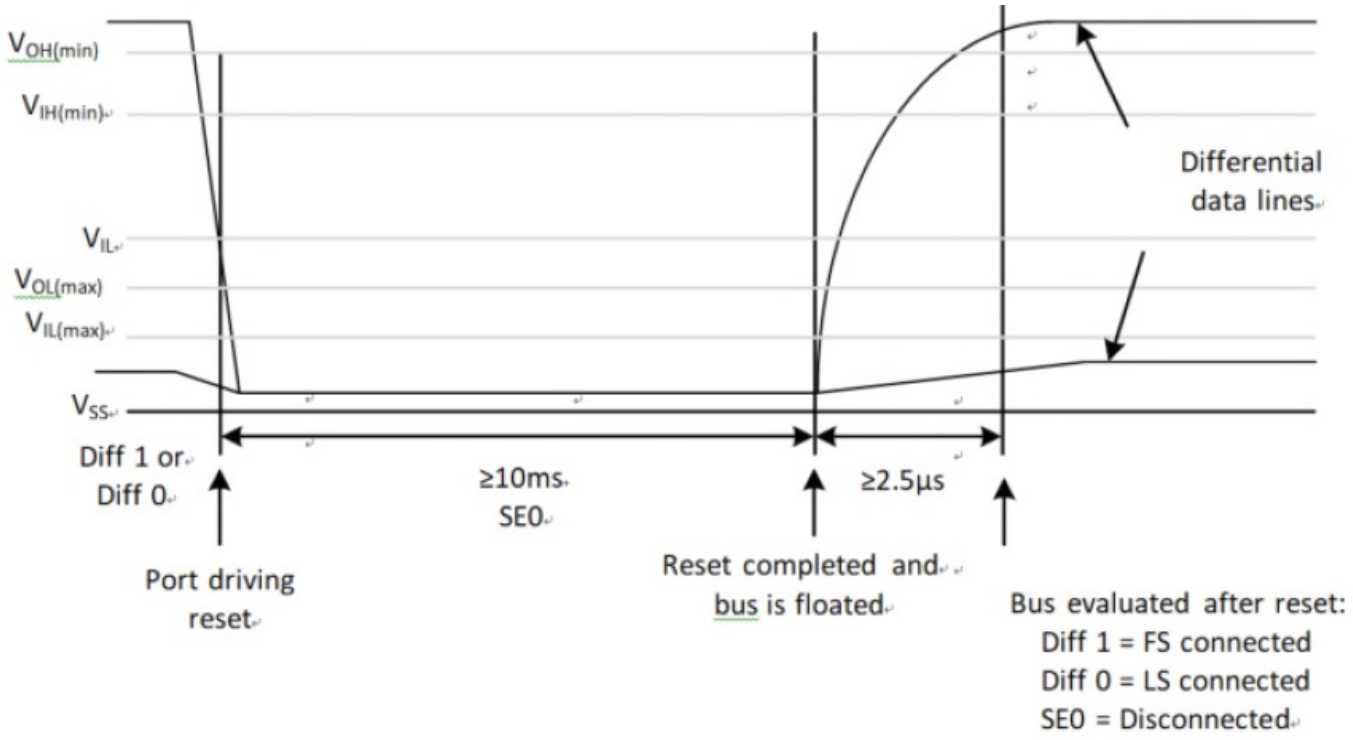


Figure 5.3-3. Bus State Evaluation after reset

HS mode

- High-speed capable devices must initially attach as full-speed devices and must comply with all full-speed connection requirements. Transition to high-speed signaling is accomplished by means of a low level electrical protocol which occurs during Reset. The differential output impedance of a high-speed capable driver is required to be 90 Ω±10%. When either the D+ or D- lines are driven high, VHSOH (the high-speed mode high-level output voltage driven on a data line with a precision 45Ω load to GND) must be 400 mV ±10%. On a line which is not driven, either because the transceiver is not transmitting or because the opposite line is being driven high, VHSOL (the high-speed mode low-level output voltage driven on a data line with a 45Ω load to GND) must be 0 V ± 10 mV.

Table 5.3-4. USB20 interface characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
D+/D-	VIH	High (driven)	2	–	V	
	VIHZ	High (floating)	2.7	3.6	V	
	VIL	Low		0.8	V	
	VOH	High (driven)	2.8	3.6	V	
	VOL	Low	0.0	0.3	V	
	VHSOH	High-speed data signaling high	360	440	mV	
	VHSOL	High-speed data signaling low	-10	10	mV	

USB timing sequence

Timing sequence have to follow USB spec that allow system timing feed no Device loss and abnormal issue count.

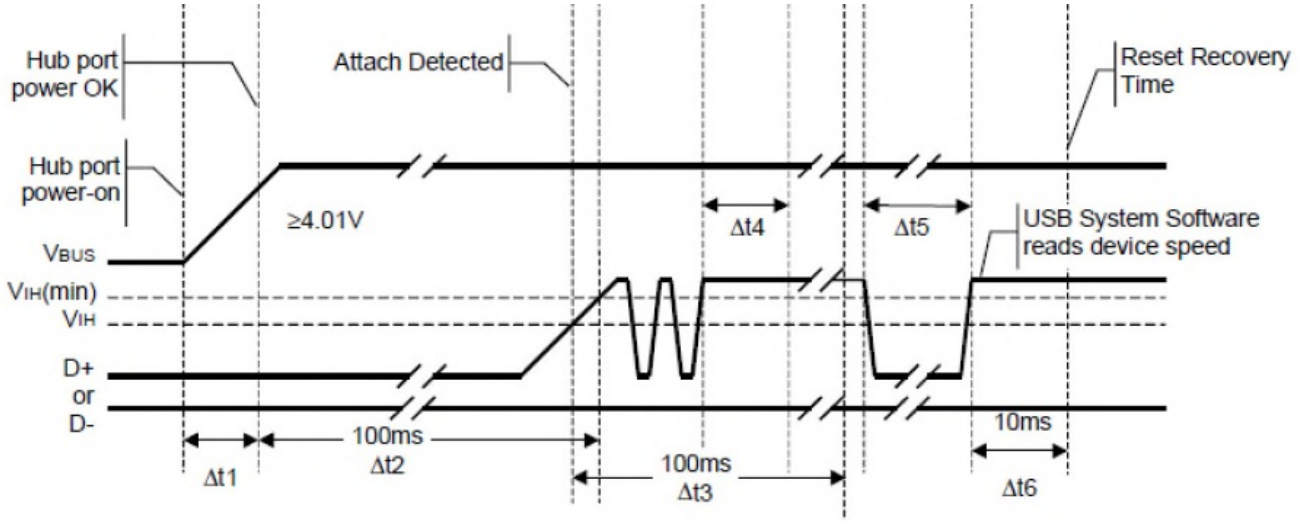


Figure 5.3-4. Power-on and Connection Events Timing

- Δt2:Max time from Vbus(up to 4.01V) to when a device has to signal attach.
- Δt3:Min time to ensure the electrical and mechanical connection is stable before system SW attempts to reset the attached device.
- Δt4:Setup time.
- Δt5:Min reset time 10ms.
- Δt6:Min time that USB system SW guarantees for reset recovery.

Bluetooth RF Subsystem

Bluetooth description

The ULL Module Bluetooth (BT) RF subsystem (as shown in Figure 6.4-1) consists of a highly integrated transceiver with tunable on-chip RF band pass filter (BPF) and BT TRX co-matching network. ULL Module adopts a low intermediate frequency (LIF) receiver architecture. The receiver, including the on-chip RF BPF and TRX co-matching network, consists of a LNA and single balanced passive mixer, a complex BPF and a pair of 10-bit SAR ADCs. The AB1571D BT receiver has best-in-class out-of-band blocking performance without the need of any external RF BPF. The direct conversion transmitter consists of a pair of 9-bit current DACs and passive LPFs, an active IQ modulator (IQM) and a Class AB push-pull PA. This PA is capable of transmitting +8dBm power for enhanced data rate (EDR) and +10dBm for basic data rate (BDR). The Class AB push-pull PA, together with on-chip RF BPF and TRX co- matching network, minimizes TX harmonic distortion products significantly, eliminating the need for an external RF BPF. The Δ-Σ fractional-N RF synthesizer is phase locked to 26MHz reference clock to generate the RF LO frequency. The BBPLL generates sampling clock for ADC and DAC as well as digital clock to BT modem. ULL Module implements various automatic calibration schemes to minimize changes in RF performance from chip-to- chip and temperature variations. No additional RF factory calibration is necessary

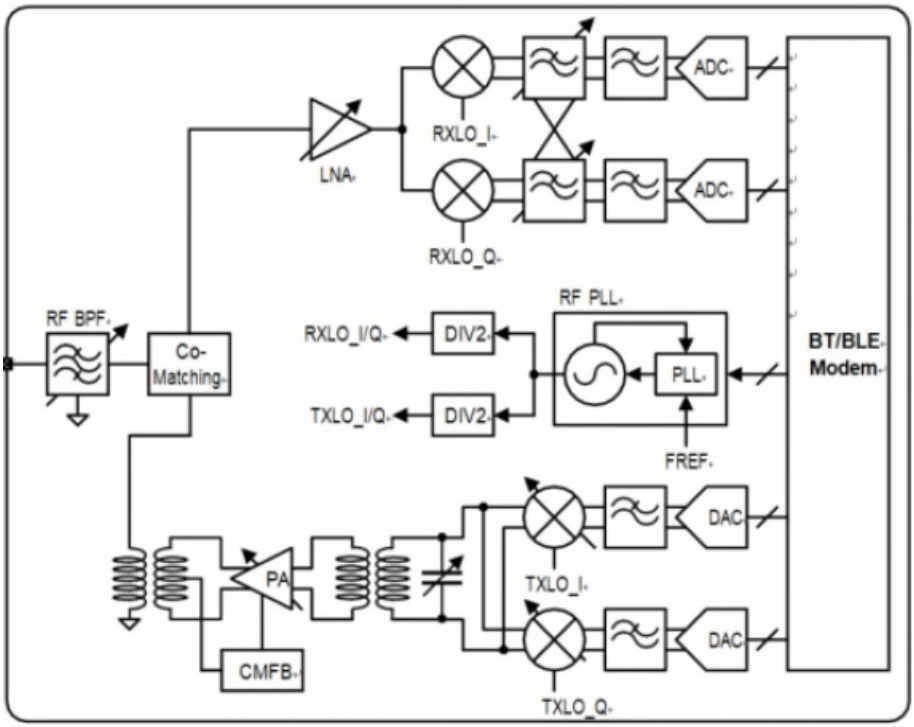


Figure 5.4-1. Bluetooth RF transceiver system

Functional specifications
Typical RF performances are specified for RF performance at module output for low/mid. /high channel, TA = +25oC, and under recommended operating conditions, unless stated otherwise.

Table 5.4-1. Recommended operating conditions

Description	Condition	Min	Typical	Max	Unit
AVDD_VBT Supply			3.3		V
AVDD_BTRF Supply			1.1		V
AVDD_DCXO Supply			1.1		V

Basic data rate – receiver specifications

Table 5.4-2. Basic Data Rate – receiver specifications

Description	Condition	Min	Typical	Max	Unit
Frequency range		2,402	–	2,480	MHz
Receiver sensitivity	BER < 0.1% (DH5)	–	-96[1](TBD)	-70	dBm
Max. detectable input power	BER < 0.1%	-20	-5	–	dBm
C/I co-channel selectivity	BER < 0.1%	–	6	11	dB
C/I 1 MHz adj. channel selectivity	BER < 0.1%	–	-7	0	dB
C/I 2 MHz adj. channel selectivity	BER < 0.1%	–	-40	-30	dB
C/I ³ 3 MHz adj. channel selectivity[2]	BER < 0.1%	–	-43	-40	dB
C/I image channel selectivity	BER < 0.1%	–	-20	-9	dB
C/I image 1 MHz adj. channel selectivity	BER < 0.1%	–	-35	-20	dB
Out-of-band blocking	30 to 2,000 MHz	-10	-4	–	dBm
	2,000 to 2,350 MHz	-27	-14	–	dBm
	2,350 to 2,400 MHz	-27	-18	–	dBm
	2,500 to 2,550 MHz	-27	-18	–	dBm
	2,550 to 3,000 MHz	-27	-14	–	dBm
	3,000 MHz to 12.75 GHz	-10	1	–	dBm
Intermodulation		-39	-30	–	dBm

Basic data rate – transmitter specifications

Table 5.4-3. Basic Data Rate – transmitter specification

Description	Condition	Min	Typical	Max	Unit
Frequency range		2,402	–	2,480	MHz
Maximum transmit power			10		dBm
Gain step		2	4	8	dB
Δf1avg (00001111)		140	157	175	kHz
Δf2max (10101010)		115	122	–	kHz
Δf1avg/Δf2avg		0.8	0.9	–	kHz
Initial carrier frequency drift		-75	10	75	kHz
Frequency drift	DH1	-25	15	25	kHz
	DH3	-40	18	40	kHz

	DH5	-40	18	40	kHz
Maximum drift rate		–	9		kHz/μs
Bandwidth 20dB of TX output spectrum		–	920	1,000	kHz
In-band spurious emission	±2 MHz offset	–	-45	-20	dBm
	±3 MHz offset	–	-50	-40	dBm
	> ±3 MHz offset	–	-50	-40	dBm
HD2	+10dBm TX Power		-45	-42	dBm
HD3	+10dBm TX Power		-47	-42	dBm

1. This value may have extra degradation due to spurs interference.
2. Except for spurious RF channels (≥ 3MHz interference), where the more relaxed C/I requirement of -17dB as defined by BT SIG specifications is applicable.

Enhanced data rate – receiver specifications

Table 5.4-4. Enhanced Data Rate –Receiver Specifications

Description	**Condition**	**Min**	**Typical**	**Max**	**Unit**
Frequency range		2,402	–	2,480	MHz
Receiver sensitivity	π/4 DQPSK, BER < 0.01% (2DH5)	–	-95.5[3](TBD)	-70	dBm
	8PSK, BER < 0.01%	–	-89[3](TBD)	-70	dBm
Maximum detectable input power	π/4 DQPSK, BER < 0.01% (3DH5)	-20	-5	–	dBm
	8PSK, BER < 0.01%	-20	-5	–	dBm
C/I co-channel selectivity	π/4 DQPSK, BER < 0.01%	–	9	13	dB
	8PSK, BER < 0.01%	–	16	21	dB
C/I 1MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	–	-12	0	dB
	8PSK, BER < 0.01%	–	-6	5	dB
C/I 2MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	–	-40	-30	dB
	8PSK, BER < 0.01%	–	-36	-25	dB
C/I [3] 3MHz adj. channel selectivity[4]	π/4 DQPSK, BER < 0.01%	–	-43	-40	dB
	8PSK, BER < 0.01%	–	-40	-33	dB
C/I image channel	π/4 DQPSK, BER < 0.01%	–	-20	-7	dB

selectivity	8PSK, BER < 0.01%	–	-15	0	dB
C/I image 1 MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	–	-40	-20	dB
	8PSK, BER < 0.01%	–	-30	-13	dB

Enhanced data rate – transmitter specifications

Table 5.4-5. Enhanced Data Rate – transmitter specifications

Description	Condition	Min	Typical	Max	Unit
Frequency range		2,402	–	2,480	MHz
Max. transmit power	π/4 DQPSK		8		dBm
	8PSK		8		dBm
Relative transmit power	π/4 DQPSK	-4	-1.5	1	dB
	8PSK	-4	-1.5	1	dB
Freq. stability ω0	π/4 DQPSK	-10	4	10	kHz
	8PSK	-10	4	10	kHz
Freq. stability ω1	π/4 DQPSK	-75	20	75	kHz
	8PSK	-75	20	75	kHz
| ω0+ω1|	π/4 DQPSK	-75	20	75	kHz
	8PSK	-75	20	75	kHz
RMS DEVM	π/4 DQPSK	–	8	20	%
	8PSK	–	8	13	%
99% DEVM	π/4 DQPSK	–	12	30	%
	8PSK	–	12	20	%
Peak DEVM	π/4 DQPSK	–	17	35	%
	8PSK	–	17	25	%
In-band spurious emission	π/4 DQPSK, ±1 MHz offset	–	-33	-26	dBm
	8PSK, ±1 MHz offset	–	-33	-26	dBm
	π/4 DQPSK, ±2 MHz offset	–	-30	-20	dBm
	8PSK, ±2 MHz offset	–	-30	-20	dBm
	π/4 DQPSK, ±3 MHz offset	–	-43	-40	dBm
	8PSK, ±3 MHz offset	–	-43	-40	dBm

- 3 This value may have extra degradation due to spurs interference.
- 4 Except for spurious RF channels (≥ 3MHz interference), where the more relaxed C/I requirements of -15dB (π/4 DQPSK) and – 10dB (8PSK) as defined by BT SIG specifications are applicable.

Bluetooth LE – receiver specifications

Table 5.4-6. Bluetooth LE 1M – receiver specifications

Description	Condition	Min	Typical	Max	Unit
Frequency range		2,402	–	2,480	MHz
Receiver sensitivity	PER < 30.8%	–	-99[5](TBD)	-70	dBm
Max. detectable input power	PER < 30.8%	-10	-5	–	dBm
C/I co-channel selectivity	PER < 30.8%	–	6	21	dB
C/I 1 MHz adj. channel selectivity	PER < 30.8%	–	-7	15	dB
C/I 2 MHz adj. channel selectivity	PER < 30.8%	–	-30	-17	dB
C/I [3] 3 MHz adj. channel selectivity[6]	PER < 30.8%	–	-33	-27	dB
C/I image channel selectivity	PER < 30.8%	–	-20	-9	dB
C/I image 1 MHz adj. channel selectivity	PER < 30.8%	–	-30	-15	dB
Out-of-band blocking	30MHz to 2,000MHz	–	–	-30	dBm
	2,001MHz to 2,339MHz	–	–	-35	dBm
	2,501MHz to 3,000MHz	–	–	-35	dBm
	3,001MHz to 12.75GHz	–	–	-30	dBm

Table 5.4-7. Bluetooth LE 2M – receiver specifications

Description	Condition	Min	Typical	Max	Unit
Frequency range		2,402	–	2,480	MHz
Receiver sensitivity	PER < 30.8%	–	-96[5](TBD)	-70	dBm
Max. detectable input power	PER < 30.8%	-10	-5	–	dBm
C/I co-channel selectivity	PER < 30.8%	–	6	21	dB
C/I 2 MHz adj. channel selectivity	PER < 30.8%	–	-7	15	dB
C/I 4 MHz adj. channel selectivity	PER < 30.8%	–	-30	-17	dB
C/I ³ 6 MHz adj. channel selectivity[3]	PER < 30.8%	–	-33	-27	dB
C/I image channel selectivity	PER < 30.8%	–	-20	-9	dB
C/I image 2 MHz adj. channel selectivity	PER < 30.8%	–	-30	-15	dB
Out-of-band blocking	30MHz to 2,000MHz	–	–	-30	dBm
	2,001MHz to 2,339MHz	–	–	-35	dBm
	2,501MHz to 3,000MHz	–	–	-35	dBm
	3,001MHz to 12.75GHz	–	–	-30	dBm

- 5 This value may have extra degradation due to spurs interference.
- 6 Except for spurious RF channels (≥ 3MHz interference), where the more relaxed C/I requirement of -17dB as defined by BT SIG specifications is applicable

Bluetooth LE – receiver specifications

Table 5.4-8. Bluetooth LE 1M – transmitter specification

Description	Condition	Min	Typical	Max	Unit
Frequency range		2,402	–	2,480	MHz
Output power			10		dBm
Modulation characteristic	Δf1avg (00001111)	235	250	265	kHz
	Δf2max (10101010)	185	215	–	kHz
	Δf1avg/Δf2avg	0.8	0.9	–	kHz
Carrier frequency offset and drift	Frequency offset	-150	±5	150	kHz
	Frequency drift	-50	±5	50	kHz
	Maximum drift rate	-20	±3	20	kHz/μs
In-band spurious emission	±2 MHz offset	–	-45	-20	dBm
	±3 MHz offset	–	-50	-30	dBm
	> ±3 MHz offset	–	-50	-30	dBm

Table 5.4-9. Bluetooth LE 2M – transmitter specification

Description	Condition	Min	Typical	Max	Unit
Frequency range		2,402	–	2,480	MHz
Output power			10		dBm
Modulation characteristic	Δf1avg (00001111)	450	500	550	kHz
	Δf2max (10101010)	370	454	–	kHz
	Δf1avg/Δf2avg	0.8	0.9	–	kHz
Carrier frequency offset and drift	Frequency offset	-150	±5	150	kHz
	Frequency drift	-50	±5	50	kHz
	Maximum drift rate	-20	±3	20	kHz/μs
In-band spurious emission	±2 MHz offset	–	-50	-20	dBm
	±3 MHz offset	–	-50	-30	dBm
	> ±3 MHz offset	–	-50	-30	dBm

FIRMWARE SPECIFICATION

FIRMWARE FEATURES

- The vendor shall provide a single firmware package that supports the wireless connection interface for audio devices and HID devices and the following features:
- Up to four simultaneous active Bluetooth LE links
- Up to four simultaneous active ACL links
- Support for Ultra Low Latency protocol and profiles

- Support for LC3plus codec
- Up to simultaneous active ICO/ICL links (ICO+ICL links=4)
- AFH and PTA collaborative support for 2.4GHz coexistence
- Support low latency mode when connected with well-matched wireless audio devices and human interface device
- Support firmware updates via chip USB interface
- Support FOTA to update the firmware for wireless peripheral audio devices and human interface devices
- Enter low power mode when the USB host is in low power mode
- Operating system control synchronization (audio/media/HID control)

Firmware Architecture Layout
Firmware architecture is the structured design of software permanently stored on hardware, typically in embedded systems. It defines how the software is organized, breaks it into modules with specific roles, and specifies communication between modules and hardware. The architecture considers scalability, security, performance, and error handling. It is crucial for ensuring efficient, reliable, and secure hardware control.

The following requirements for the firmware layout:

Board Support Package (BSP)

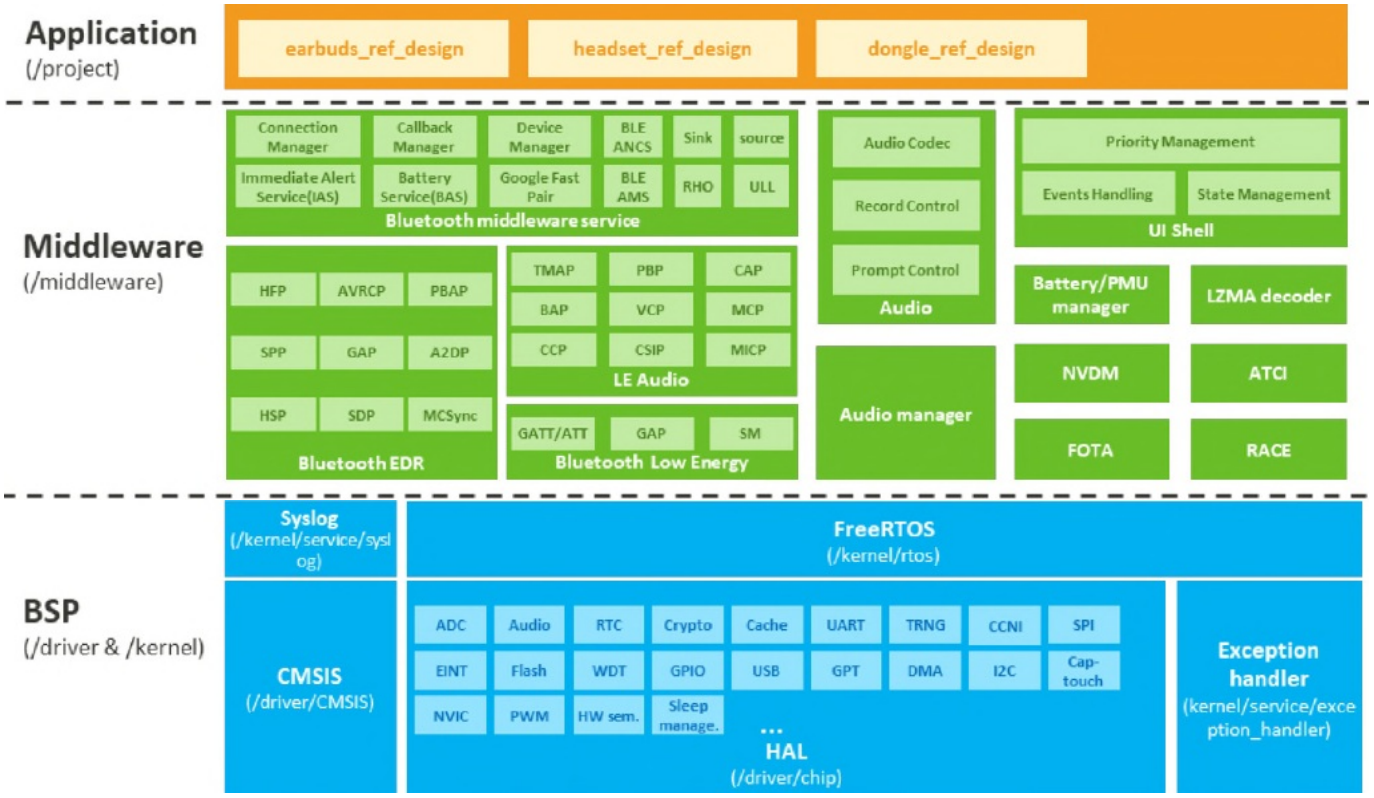
- Hardware drivers – Provide peripheral drivers for the platform, such as ADC, I2S, I2C, SPI, RTC, GPIO, UART, Flash, Security Engine, TRNG, GDMA, PWM, WDT and IRDA TX/RX.
- Hardware Abstraction Layer (HAL) – Provides the driver Application Programming Interface (API) encapsulating the low-level functions of peripheral drivers for the operating system (OS), Middleware features, and Application.
- Free RTOS – An OS with open-source software for the Middleware components and Applications.
- Syslog – This module implements system logging for development and debugging.

Middleware

- Ultra Low Latency service – Provides stack and protocol-layer access profiles for data transfer and management control:
    - Host Controller Interface (HCI)
    - Logical Link Control and Adaptation Layer Protocol (L2CAP)
    - Generic Access Profile (GAP)
    - Security Manager Protocol (SMP)
    - Ultra Low Latency Profile
    - Ultra Low Latency Service
- Audio – This module is for audio middleware implementation.
- Audio manager – This module is the Audio Manager control implementation, including all primary audio behavior management and most of the control for DSP.
- FOTA – Provides a mechanism to update the firmware.

Application

- Support Universal Serial Bus Device Class Definition for Audio Devices 1.0 or above
- Support Universal Serial Bus Device Class Definition for Human Interface Devices 1.11 or above
- Pre-configured projects using Middleware components for the interface toward the operating system for wireless audio devices and HIDs.
- The application layer enables running projects based on Middleware, FreeRTOS, and HAL layers. These layers provide rich features for application development



ULTRA LOW LATENCY PROTOCOL AND PROFILE

A set of protocols and profiles designed to minimize communication delays between connected devices. It targets scenarios where extremely low latency is crucial for HP's product portfolio. Firmware should provide Ultra Low Latency (ULL) protocol and profiles to optimize data transmission, ensuring information travels between devices with minimal delay. Achieving ultra-low latency is essential in applications where timely data exchange is critical for a seamless user experience, such as wireless audio devices and human interface devices.

Firmware Role And Responsibility In ULL Protocol

Firmware as ULL Serve in the Ultra-Low Latency version 2.0/2.1/2.2 (ULL V2.0/2.1/2.2) is a proprietary technology by IP Provider designed to achieve less than 20ms downlink voice/audio latency for wireless audio devices and low latency downlink for human interface device over Bluetooth LE when paired with compatible devices. The ULL Server, a device with USB-in/I2S-in audio and HID capabilities, encodes PCM audio data into IP Provider

FAQ

- **Q: How do I reset the module to factory settings?**

  A: To reset the module, locate the reset button on your device and hold it down for 10 seconds until the module restarts.
- **Q: What is the range of wireless connectivity for this module?**

  A: The range typically extends up to 30 meters in an open environment, but may vary based on interference and obstacles.

Documents / Resources

	MERRY HSN-M01BTM HyperX Embedded Wireless Module [pdf] User Guide HSN-M01BTM, 89M131001001, HSN-M01BTM HyperX Embedded Wireless Module, HSN-M01BTM, HyperX Embedded Wireless Module, Embedded Wireless Module, Wireless Module, Module

References

- User Manual