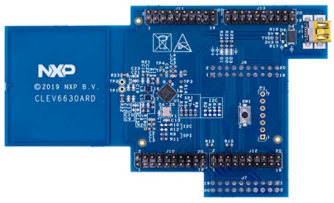
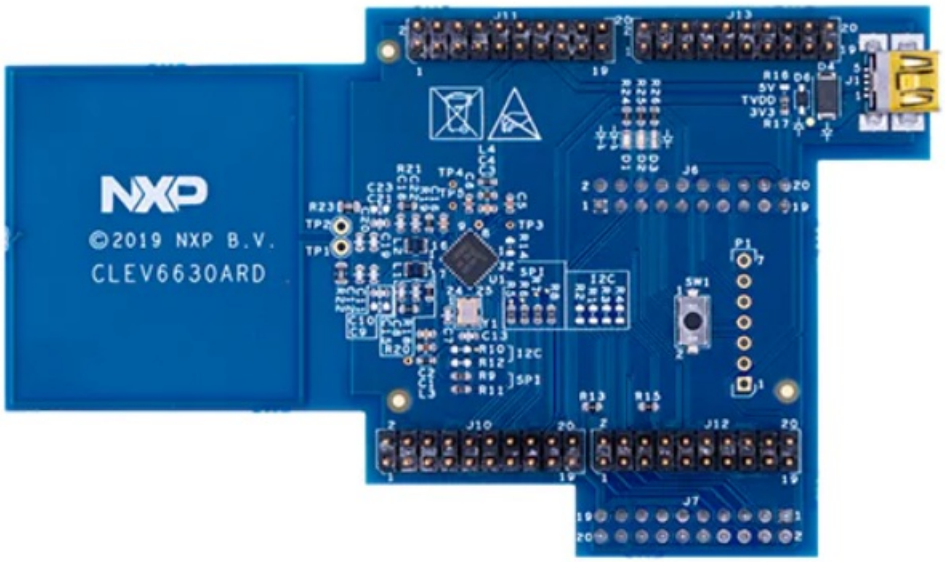


MATRIX CLRC663-NXP MIFARE Reader Module User Manual

Contents

MATRIX CLRC663-NXP MIFARE Reader Module



Product Information

Documentation Disclaimer

Matrix Comsec reserves the right to make changes in the design or components of the product as engineering and manufacturing may warrant. Specifications are subject to change without notice.

This is a general documentation for all variants of the product. The product may not support all the features and facilities described in the documentation.

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Version

Version 1 Release date: January 5, 2023

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8. Recommended Operating Conditions
9. Thermal Characteristics
10. Characteristics
11. Application Information
12. Handling Information
13. Regulatory Information
14. Disposal of Products/Components after End-Of-Life

Product Usage Instructions

Overview – CLRC663-NXP
The CLRC663-NXP is a multi-protocol NFC front-end IC that supports various operating modes.

Operating Modes:

- ISO/IEC 14443A
- MIFARE Classic IC-based cards and transponders

The CLRC663-NXP's internal transmitter can drive a reader/writer antenna designed to communicate with ISO/IEC 14443A and MIFARE Classic IC-based cards and transponders without additional active circuitry. The digital module manages the complete ISO/IEC 14443A framing and error detection functionality (parity and CRC).

Please refer to the corresponding sections in the user manual for detailed information on features, benefits, applications, quick reference data, block diagram, pinning information, limiting values, recommended operating conditions, thermal characteristics, characteristics, application information, handling information, regulatory information, and disposal of products/components after end-of-life.

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Version 1

Release date: January 5, 2023

Overview – CLRC663-NXP

The CLRC663-NXP multi-protocol NFC front-end IC supports the following operating modes:

- Read/write mode supporting ISO/IEC 14443 type A and MIFARE Classic communication mode
- Read/write mode supporting ISO/IEC 14443B
- Read/write mode supporting JIS X 6319-4 (comparable with FeliCa)1
- Passive initiator mode according to ISO/IEC 18092
- Read/write mode supporting ISO/IEC 15693
- Read/write mode supporting ICODE EPC UID/ EPC OTP
- Read/write mode supporting ISO/IEC 18000-3 mode 3/ EPC Class-1 HF

The CLRC663-NXP's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A and MIFARE Classic IC-based cards and transponders without additional active circuitry. The digital module manages the complete ISO/IEC 14443A framing and error detection functionality (parity and CRC). The CLRC663-NXP supports MIFARE Classic with 1 kB memory, MIFARE Classic with 4 kB memory, MIFARE Ultralight, MIFARE Ultralight C, MIFARE Plus and MIFARE DESFire products. The CLRC663-NXP supports higher transfer speeds of the MIFARE product family up to 848 kbit/s in both directions.
The CLRC663-NXP supports layer 2 and 3 of the ISO/IEC 14443B reader/writer communication scheme except anti-collision. The anti-collision needs to be implemented in the firmware of the host controller as well as in the upper layers.
The CLRC663-NXP is able to demodulate and decode FeliCa coded signals. The FeliCa receiver part provides the demodulation and decoding circuitry for FeliCa coded signals. The CLRC663-NXP handles the FeliCa framing and error detection such as CRC. The CLRC663-NXP supports FeliCa higher transfer speeds of up to 424 kbit/s in both directions.
The CLRC663-NXP is supporting the P2P passive initiator mode in accordance with ISO/IEC 18092.
The CLRC663-NXP supports the vicinity protocol according to ISO/IEC15693, EPC UID and ISO/IEC 18000-3 mode 3/ EPC Class-1 HF.

The following host interfaces are supported:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependent on pin voltage supply)
- I2C-bus interface (two versions are implemented: I2C and I2CL)

The CLRC663-NXP supports the connection of a secure access module (SAM). A dedicated separate I2C interface is implemented for a connection of the SAM. The SAM can be used for high secure key storage and acts as a very performant crypto-coprocessor. A dedicated SAM is available for connection to the CLRC663-NXP.

In this document, the term "MIFARE Classic card" refers to a MIFARE Classic IC-based contactless card.

Features and Benefits

- Includes NXP ISO/IEC14443-A and Innovatron ISO/IEC14443-B intellectual property licensing rights
- High performance multi-protocol NFC frontend for transfer speed up to 848 kbit/s
- Supports ISO/IEC 14443 type A, MIFARE Classic, ISO/IEC 14443 B and FeliCa reader modes
- P2P passive initiator mode in accordance with ISO/IEC 18092

- Supports ISO/IEC15693, ICODE EPC UID and ISO/IEC 18000-3 mode 3/ EPC Class-1 HF
- Supports MIFARE Classic product encryption by hardware in read/write mode. Allows reading cards based on MIFARE Ultralight, MIFARE Classic with 1 kB memory, MIFARE Classic with 4 kB memory, MIFARE DESFire EV1, MIFARE DESFire EV2 and MIFARE Plus ICs
- Low-Power Card Detection
- Compliance to EMV contactless protocol specification on RF level can be achieved
- Supported host interfaces:
- SPI up to 10 Mbit/s
- I2C-bus interfaces up to 400 kBd in Fast mode, up to 1000 kBd in Fast mode plus
- RS232 Serial UART up to 1228.8 kBd, with voltage levels dependent on pin voltage supply
- Separate I2C-bus interface for connection of a secure access module (SAM)
- FIFO buffer with size of 512 bytes for highest transaction performance
- Flexible and efficient power-saving modes including hard power down, standby and low-power card detection
- Cost saving by integrated PLL to derive system clock from 27.12 MHz RF quartz crystal
- 3.0 V to 5.5 V power supply (CLRC66301, CLRC66302) 2.5 V to 5.5 V power supply (CLRC66303)
- Up to 8 free programmable input/output pins
- Typical operating distance in read/write mode for communication to a ISO/IEC 14443 type A and MIFARE Classic card up to 12 cm, depending on the antenna size and tuning
- Two package options are available for the CLRC66303:
- HVQFN32: Package with wettable flanks easing the soldering process and quality control of soldered parts
- VFBGA36: Smallest package with optimized pin configuration for simple PCB layout
- The version CLRC66303 offers a more flexible configuration for Low-Power Card detection compared to the CLRC66301 and CLRC66302 with the new register LPCD_OPTIONS. In addition, the CLRC66303 offers new additional settings for the Load Protocol which fit very well to smaller antennas. The CLRC66303 is therefore the recommended version for new designs

Applications

- Industrial
- Access control
- Gaming

Quick Reference Data

CLR66301 and CLRC66302

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			3.0	5.0	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage		[1]	3.0	5.0	V_{DD}	V
$V_{DD(TVDD)}$	TVDD supply voltage			3.0	5.0	5.5	V
I_{pd}	power-down current	PDOWN pin pulled HIGH	[2]	-	8	40	nA
I_{DD}	supply current			-	17	20	mA
$I_{DD(TVDD)}$	TVDD supply current			-	100	250	mA
T_{amb}	operating ambient temperature			-25	+25	+85	°C
T_{stg}	storage temperature	no supply voltage applied		-55	+25	+125	°C

1. VDD(PVDD) must always be the same or lower voltage than VDD.

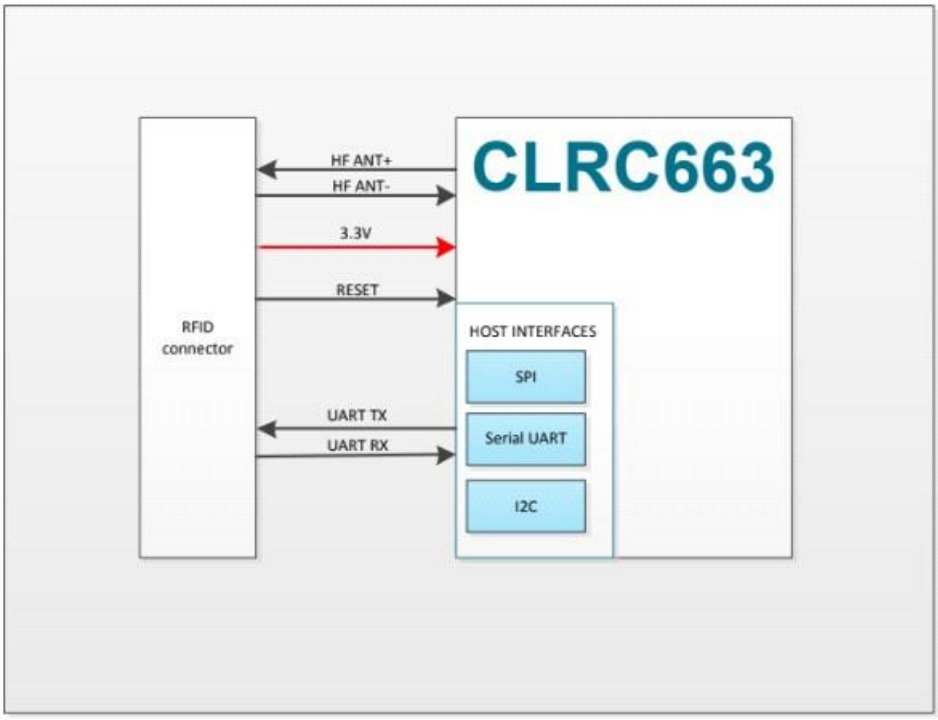
2. Ipd is the sum of all supply currents

CLRC66303

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			2.5	5.0	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage		[1]	2.5	5.0	V_{DD}	V
$V_{DD(TVDD)}$	TVDD supply voltage			2.5	5.0	5.5	V
I_{pd}	power-down current	PDOWN pin pulled HIGH	[2]	-	8	40	nA
I_{DD}	supply current			-	17	20	mA
$I_{DD(TVDD)}$	TVDD supply current	recommended operation		-	180	350	mA
		absolute limiting value		-	-	500	mA
T_{amb}	operating ambient temperature	device mounted on PCB which allows sufficient heat dissipation for the actual power dissipation of the device		-40	+25	+105	°C
T_{stg}	storage temperature	no supply voltage applied		-55	+25	+125	°C

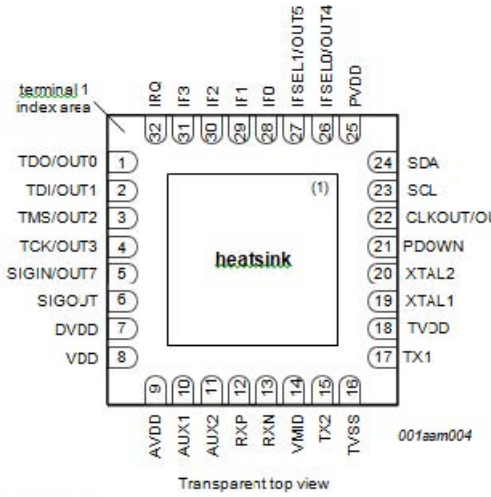
1. VDD(PVDD) must always be the same or lower voltage than VDD.
2. Ipd is the sum of all supply currents

Block Diagram



Pinning Information

Pin-out Diagram



1. VSS - heat sink connection

Pinning configuration HVQFN32 (SOT617-1)

Pin Description – HVQFN32

Pin	Symbol	Type	Description
1	TDO / OUT0	O	test data output for boundary scan interface / general purpose output 0
2	TDI / OUT1	I/O	test data input boundary scan interface / general purpose output 1
3	TMS / OUT2	I/O	test mode select boundary scan interface / general purpose output 2
4	TCK / OUT3	I/O	test clock boundary scan interface / general purpose output 3
5	SIGIN /OUT7	I/O	Contactless communication interface output. / general purpose output 7
6	SIGOUT	O	Contactless communication interface input.
7	DVDD	PWR	digital power supply buffer [1]
8	VDD	PWR	power supply
9	AVDD	PWR	analog power supply buffer [1]
10	AUX1	O	auxiliary outputs: Pin is used for analog test signal
11	AUX2	O	auxiliary outputs: Pin is used for analog test signal
12	RXP	I	receiver input pin for the received RF signal.
13	RXN	I	receiver input pin for the received RF signal.
14	VMID	PWR	internal receiver reference voltage [1]
15	TX2	O	transmitter 2: delivers the modulated 13.56 MHz carrier
16	TVSS	PWR	transmitter ground, supplies the output stage of TX1, TX2
17	TX1	O	transmitter 1: delivers the modulated 13.56 MHz carrier

18	TVDD	PWR	transmitter voltage supply
19	XTAL1	I	crystal oscillator input: Input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (fosc = 27.12 MHz)
20	XTAL2	O	crystal oscillator output: output of the inverting amplifier of the oscillator
21	PDOWN	I	Power Down (RESET)
22	CLKOUT / OUT 6	O	clock output / general purpose output 6
23	SCL	O	Serial Clock line
24	SDA	I/O	Serial Data Line
25	PVDD	PWR	pad power supply
26	IFSEL0 / OUT4	I	host interface selection 0 / general purpose output 4
27	IFSEL1 / OUT5	I	host interface selection 1 / general purpose output 5
28	IF0	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I2C, I2C-L
29	IF1	I/O	interface pin, multifunction pin: Can be assigned to host interface SPI, I^2C, I^2C-L
30	IF2	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
31	IF3	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
32	IRQ	O	interrupt request: output to signal an interrupt event
33	VSS	PWR	ground and heat sink connection

1. This pin is used for connection of a buffer capacitor. Connection of a supply voltage might damage the device.

Pin Description – VFBGA36

Symbol	**Pin**	**Type**	**Description**

IF2	A1	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
IF1	A2	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
IF0	A3	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
IFSEL1	A4	I	host interface selection 1 / general purpose output 5
PVDD	A5	PWR	pad power supply
PDOWN	A6	I	Power Down (RESET)
IRQ	B1	O	interrupt request: output to signal an interrupt event
TDI / OUT1	B2	I/O	test data input boundary scan interface / general purpose output 1
TMS / OUT2	B3	I/O	test mode select boundary scan interface / general purpose output 2
TDO / OUT0	B4	O	test data output for boundary scan interface / general purpose output 0
SCL	B5	I	Serial Clock line
XTAL2	B6	O	crystal oscillator output: output of the inverting amplifier of the oscillator
IF3	C1	I/O	interface pin, multifunction pin: Can be assigned to host interface RS232, SPI, I^2C, I^2C-L
TCK / OUT2	C2	I/O	test clock boundary scan interface / general purpose output 3
GND	C3	PWR	ground and heat sink connection
CLKOUT / OUT6	C4	O	clock output / general purpose output 6
SDA	C5	I/O	Serial Data Line

XTAL1	C6	I	crystal oscillator input: Input to the inverting amplifier of the oscillator. T his pin is also the input for an externally generated clock (fosc = 27.12 MHz)
DVDD	D1	PWR	digital power supply buffer [1]
SIGIN / OUT7	D2	I/O	Contactless communication interface output. / general purpose output 7
GND	D3	PWR	ground and heat sink connection
GND	D4	PWR	ground and heat sink connection
GND	D5	PWR	ground and heat sink connection
TVDD	D6	PWR	transmitter voltage supply
VDD	E1	PWR	power supply
AUX1	E2	O	auxiliary output: Pin is used for analog test signal
SIGOUT	E3	O	Contactless communication interface input.
AUX2	E4	O	auxiliary output: Pin is used for analog test signal
IFSEL0	E5	I	host interface selection 0 / general purpose output 4
TX1	E6	O	transmitter 1: delivers the modulated 13.56 MHz carrier
AVDD	F1	PWR	analog power supply buffer [1]
RXP	F2	I	receiver input pin for the received RF signal.
RXN	F3	I	receiver input pin for the received RF signal.
VMID	F4	PWR	internal receiver reference voltage [1]
TX2	F5	O	transmitter 2: delivers the modulated 13.56 MHz carrier
TVSS	F6	PWR	transmitter ground, supplies the output stage of TX1, TX2

1. This pin is used for connection of a buffer capacitor. Connection of a supply voltage might damage the device.

Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.0	V
$V_{DD(PVDD)}$	PVDD supply voltage			-0.5	+6.0	V
$V_{DD(TVDD)}$	TVDD supply voltage			-0.5	+6.0	V
$I_{DD(TVDD)}$	TVDD supply current	CLRC66301, CLRC66302		-	250	mA
		CLRC66303		-	500	mA
$V_{i(RXP)}$	input voltage on pin RXP			-0.5	+2.0	V
$V_{i(RXN)}$	input voltage on pin RXN			-0.5	+2.0	V
P_{tot}	tota power dissipation	per package		-	1125	mW
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]; 1500 Ω, 100 pF		-2000	2000	V
		charge device model (CDM)[2]		-500	500	V
$T_{j(max)}$	maximum junction temperature			-	+150	°C
T_{stg}	storage temperature	no supply voltage applied		-55	+150	°C

1. According to ANSI/ESDA/JEDEC JS-001.
2. According to ANSI/ESDA/JEDEC JS-002.

Recommended Operating Conditions

Exposure of the device to other conditions than specified in the Recommended Operating Conditions section for extended periods may affect device reliability.

Electrical parameters (minimum, typical and maximum) of the device are guaranteed only when it is used within the recommended operating conditions.

Operating conditions CLRC66301, CLRC66302

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			3.0	5.0	5.5	V
$V_{DD(TVDD)}$	TVDD supply voltage		[1]	3.0	5.0	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage	all host interfaces		3.0	5.0	5.5	V
$T_{j(max)}$	maximum junction temperature	-		-	-	+125	°C
T_{amb}	operating ambient temperature	in still air with exposed pin soldered on a 4 layer JEDEC PCB		-25	+25	+85	°C
T_{stg}	storage temperature	no supply voltage applied, relative humidity 45...75%		-45	+25	+125	°C

1. VDD(PVDD) must always be the same or lower than VDD.

Operating conditions CLRC66303

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			2.5	5.0	5.5	V
$V_{DD(TVDD)}$	TVDD supply voltage		[1]	2.5	5.0	5.5	V
$V_{DD(PVDD)}$	PVDD supply votage	all host nterfaces except I2C interface		2.5	5.0	5.5	V
		all host nterfaces incl. I2C interface		3.0	5.0	5.5	V
$T_{j(max)}$	maximum junction temperature	-		-	-	+125	°C
T_{amb}	operating ambient temperature	HVQFN32 package, in still air with exposed pin soldered on a 4 layer JEDEC PCB		-40	+25	+105	°C
		VFBGA36 package, in still air with exposed pin soldered on a 4 layer JEDEC PCB		-40	+25	+85	°C
T_{stg}	storage temperature	no supply voltage applied, relative humidity 45...75%		-45	+25	+125	°C

1. VDD(PVDD) must always be the same or lower than VDD.

Thermal Characteristics

Thermal characteristics HVQFN32

Symbol	Parameter	Conditions		Package	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in still air with exposed pin soldered on a 4 layer JEDEC PCB		HVQFN32	40	K/W

Thermal characteristics VFBGA36

Symbol	Parameter	Conditions		Package	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in still air with exposed pin soldered on a 4 layer JEDEC PCB		VFBGA36	65	K/W

Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Current consumption							
I_{DD}	supply current	$I_{DD} = A_{VDD}+D_{VDD}$; modem on (transmitter and receiver are switched on)		-	17	20	mA
		$I_{DD} = A_{VDD}+D_{VDD}$; modem off (transmitter and receiver are switched off)		-	0.45	0.5	mA
$I_{DD(PVDD)}$	PVDD supply current	no load on digital pins, leakage current only		-	0.5	5	µA
$I_{DD(TVDD)}$	TVDD supply current	CLRC6630˙HN, CLRC66302HN		-	100	250	mA
		CLRC66303HN		-	250	350	mA
I_{pd}	power-down current	All OUTx pins floating					
		ambient temp = +25 °C		-	40	400	nA
		ambient temp = -40°C... +85°C		-	1.5	2.1	µA
		CLRC66303: ambient temp = +105 °C		-	3.5	5.2	µA
I_{stby}	standby current	All OUTx pins floating					
		ambient temp = 25 °C, $I_{VDD}+I_{TVDD}+I_{PVDD}$		-	3	6	µA
		ambient temp = -40°C... +105°C, $I_{stby} = I_{VDD}+I_{TVDD}+I_{PVDD}$		-	5.25	26	
$I_{LPCD(sleep)}$	LPCD sleep current	All OUTx pins floating					
		LFO active, no RF field on, ambient temp = 25 °C	[1]	-	3.3	6.3	µA
$I_{LPCD(average)}$	LPCD average current	All OUTx pins floating, TxLoad = 50 ohms. LPCD_FILTER = 0; Rfon duration = 10 us, RF-off duration 300ms; V_{TVDD} = 3.0V; T_{amb} = 25°C; $I_{LPCD} = I_{VDD}+I_{TVDD}+I_{PVDD}$					
		LPCD_TX_HIGH = 0,		-	12	-	µA
		LPCD_TX_HIGH = 1		-	23	-	
t_{RFON}	RF-on time during LPCD	LPCD_TX_HIGH = 0; TVDD=5.0 V T=25°C;		-	10	-	µs
		LPCD_TX_HIGH = 1; TVDD=5.0 V; T=25°C		-	50	-	µs

Buffer capacitors on AVDD,DVDD

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_L	external buffer capacitor	AVDD		220	470	-	nF
C_L	external buffer capacitor	DVDD		220	470	-	nF
I/O pin characteristics SIGIN/OUT7, SIGOUT, CLKOUT/OUT6, IF SEL0/OUT4, IF SEL1/OUT5, TCK/OUT3, TMS/OUT2, TDI/ OUT1, TDO/OUT0, IRQ, IF0, IF1, IF2, SCL2, SDA2							
I_{LI}	input leakage current	output disabled		0.0	50	500	nA
V_{IL}	low-level input voltage			-0.5	-	0.3 x $V_{DD(PVDD)}$	V
V_{IH}	high-level input voltage			0.7 x $V_{DD(PVDD)}$	$V_{DD(PVDD)}$	$V_{DD(PVDD)}$ + 0.5	V
V_{OL}	low-level output voltage			0.0	0.0	0.4	V
V_{OH}	high-level output voltage	If pins are used as output OUTx, I_{OH} = 4 mA driving current for each pin		$V_{DD(PVDD)}$-0.4	$V_{DD(PVDD)}$	$V_{DD(PVDD)}$	V
C_i	input capacitance			0.0	2.5	4.5	pF
Pin characteristics PDOWN							
V_{IL}	low-level input voltage			0.0	0.0	0.4	V
V_{IH}	high-level input voltage			0.6 x V_{PVDD}	$V_{DD(PVDD)}$	$V_{DD(PVDD)}$	V
Pull-up resistance for TCK, TMS, TDI, IF2							
R_{pu}	pull-up resistance			50	72	120	KΩ
Pin characteristics AUX 1, AUX 2							
V_o	output voltage			0.0	-	1.8	V
C_L	load capacitance			0.0	-	400	pF

Pin characteristics RXP, RXN							
$V_{i(p)}$	input voltage			0	1.65	1.8	V
C_i	input capacitance			2	3.5	5	pF
$V_{mod(pp)}$	modulation voltage	$V_{mod(pp)} = V_{i(pp)(max)} - V_{i(pp)(min)}$		-	2.5	-	mV
Pins TX1 and TX2							
V_o	output voltage			$V_{ss(TVSS)}$	-	$V_{DD(TVDD)}$	V
R_o	output resistance	CLRC66301, CLRC66302: T=25°C, $V_{DD(TVDD)}$ = 5.0V		-	1.5	-	Ω
		CLRC66303: T=25°C, $V_{DD(TVDD)}$ = 5.0V		-	1.2	-	Ω
Clock frequency Pin CLKOUT							
f_{clk}	clock frequency	configured to 27.12 MHz		-	27.12	-	MHz
δ_{clk}	clock duty cycle			-	50	-	%
Crystal connection XTAL1, XTAL2							
$V_{o(p-p)}$	peak-to-peak output voltage	pin XTAL1		-	1.0	-	V

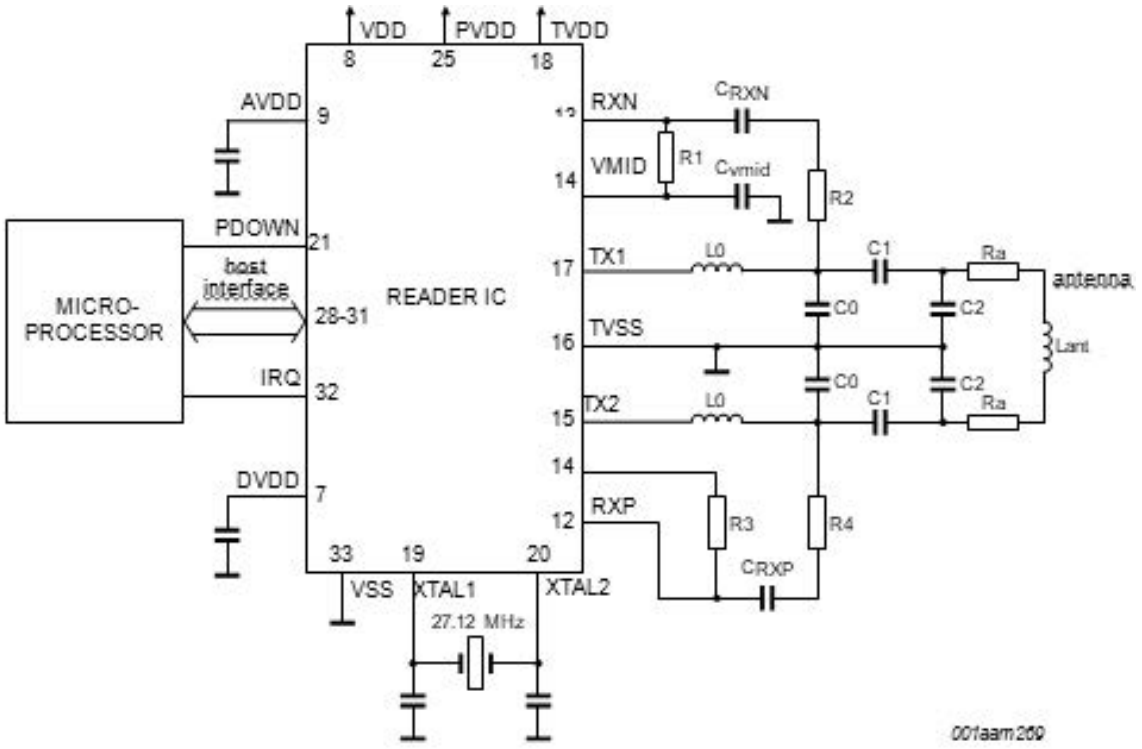
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_i	input voltage	pin XTAL1		0.0	-	1.8	V
C_i	input capacitance	pin XTAL1		-	3	-	pF
Crystal requirements							
f_{xtal}	crystal frequency	ISO/IEC14443 compliancy		27.12-14kHz	27.12	27.12+14kHz	MHz
ESR	equivalent series resistance			-	50	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	50	100	µW
Input characteristics I/O Pin Characteristics IF3-SDA in I^2C configuration							
I_{LI}	input leakage current	output disabled		-	2	100	nA
V_{IL}	LOW-level input voltage			-0.5	-	+0.3 $V_{DD(PVDD)}$	V
V_{IH}	HIGH-level input voltage			0.7 $V_{DD(PVDD)}$	-	$V_{DD(PVDD)}$ + 0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA		-	-	0.3	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; Standard mode, Fast mode		4	-	-	mA
		V_{OL} = 0.6 V; Standard mode, Fast mode		6	-	-	mA
$t_{f(o)}$	output fall time	Standard mode, Fast mode, C_L < 400 pF		-	-	250	ns
		Fast mode +; C_L < 550 pF		-	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			0	-	50	ns
C_i	input capacitance			-	3.5	5	pF

C_L	load capacitance	Standard mode		-	-	400	pF
		Fast mode		-	-	550	pF
t_{EER}	EEPROM data retention time	T_{amb} = +55 °C		10	-	-	year
N_{EEC}	EEPROM endurance (number of programming cycles)	under all operating conditions		5×10^5	-	-	cycle

Application Information

A typical application diagram using a complementary antenna connection to the CLRC663-NXP is shown in the following figure.

The antenna tuning and RF part matching is described in the application note [1] and [2].



Typical application antenna circuit diagram

Antenna design description

The matching circuit for the antenna consists of an EMC low pass filter (L0 and C0), a matching circuitry (C1 and C2), and a receiving circuits (R1 = R3, R2 = R4, C3 = C5 and C4 = C6;), and the antenna itself. The receiving circuit component values need to be designed for operation with the CLRC663-NXP. A re-use of dedicated antenna designs done for other products without adaptation of component values will result in degraded performance.

EMC low pass filter

The MIFARE product-based system operates at a frequency of 13.56 MHz. This frequency is derived from a quartz oscillator to clock the CLRC663-NXP and is also the basis for driving the antenna with the 13.56 MHz energy carrier. This will not only cause emitted power at 13.56 MHz but will also emit power at higher harmonics. The international EMC regulations define the amplitude of the emitted power in a broad frequency range. Thus, an appropriate filtering of the output signal is necessary to fulfill these regulations.

Remark: The PCB layout has a major influence on the overall performance of the filter.

Antenna matching

Due to the impedance transformation of the given low pass filter, the antenna coil has to be matched to a certain impedance. The matching elements C1 and C2 can be estimated and have to be fine-tuned depending on the design of the antenna coil.

The correct impedance matching is important to provide the optimum performance. The overall quality factor has to be considered to guarantee a proper ISO/IEC 14443 communication scheme. Environmental influences have to be considered as well as common EMC design rules. For details, refer to the NXP application notes.

Receiving circuit

The internal receiving concept of the CLRC663-NXP makes use both side-bands of the subcarrier load modulation of the card response via a differential receiving concept (RXP, RXN). No external filtering is required. It is recommended using the internally generated VMID potential as the input potential of pin RX. This DC voltage level of VMID has to be coupled to the Rx-pins via R2 and R4. To provide a stable DC reference voltage capacitances C4, C6 has to be connected between VMID and ground. Refer to the figure above.

Considering the (AC) voltage limits at the Rx-pins the AC voltage divider of R1 + C3 and R2 as well as R3 + C5 and R4 has to be designed. Depending on the antenna coil design and the impedance matching, the voltage at the antenna coil varies from antenna design to antenna design. Therefore the recommended way to design the

receiving circuit is to use the given values for R1(= R3), R2 (= R4), and C3 (= C5) from the above mentioned application note, and adjust the voltage at the RX-pins by varying R1(= R3) within the given limits.
Remark: R2 and R4 are AC-wise connected to ground (via C4 and C6).

Antenna coil
The precise calculation of the antenna coils' inductance is not practicable but the inductance can be estimated using the following formula. We recommend designing an antenna either with a circular or rectangular shape.

$$L_1 = 2 \cdot I_1 \cdot \left(\ln\left(\frac{I_1}{D_1}\right) + -K \right) N_1^{1,8}$$

(4)

- I1 – Length in cm of one turn of the conductor loop
- D1 – Diameter of the wire or width of the PCB conductor respectively
- K – Antenna shape factor (K = 1.07 for circular antennas and K = 1.47 for square antennas)
- L1 – Inductance in nH
- N1 – Number of turns
- Ln: Natural logarithm function

The actual values of the antenna inductance, resistance, and capacitance at 13.56 MHz depend on various parameters such as:

- antenna construction (Type of PCB)
- hickness of conductor
- distance between the windings shielding layer
- metal or ferrite in the near environment

Therefore a measurement of those parameters under real life conditions, or at least a rough measurement and a tuning procedure are highly recommended to guarantee a reasonable performance. For details, refer to the above mentioned application note.

Handling Information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

Regulatory Information

FCC STATEMENT
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio

communications. However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
This device is intended only for host manufacturers under the following conditions:

- The transmitter module may not be co-located with any other transmitter or antenna;
- The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module.
- The antenna must be either permanently attached or employ a 'unique' antenna coupler.

As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

List of applicable FCC rules
FCC Part 15 Subpart C 15.225

Specific operational use conditions
The module MI-FARE READER MODULE is a module with NFC function.
Operation Frequency: 13.56MHz
Type: LOOP Antenna

1. When connect MI-FAR MODULE to the host device, the host device must be power off.
2. Make sure the module pins correctly installed
3. Make sure that the module does not allow users to replace or demolition

   Matrix MIFARE Reader Module User Manual

Limited module procedures
Describe alternative means that the grantee uses to verify the host meets the necessary limiting conditions When RF exposure evaluation is necessary, state how control will be maintained such that compliance is ensured, Class II for new hosts, etc.

Trace antenna designs
This MI-FARE READER MODULE complies with FCC's RF radiation exposure limits set forth for an uncontrolled environment. The antenna(s) used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter.

RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users 'body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application. The FCC ID of the module cannot be used on the final product. In these circumstances, the host manufacturer will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization

Antennas
Antenna specification

- Height: 23mm,width: 59mm
- Trace width: 0.508mm
- Trace gap: – 0.508mm
- Turns: 4
- Inductance: 1.66μH

The operating frequency of MI-FARE READER MODULE module is 13.56Mhz

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a 'unique' antenna coupler.
As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Label and compliance information
Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID:2ADHN-CLRC663" with their finished product.

Information on test modes and additional testing requirements
The module is connected with the controlled board when testing.

Additional testing, Part 15 Subpart B disclaimer
The MI-FARE READER MODULE is only FCC authorized for the specific rule parts (FCC Part 15.225) list on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuitry.

This device is intended only for OEM integrators under the following conditions:

- The transmitter module may not be co-located with any other transmitter or antenna.
- The module shall be only used with the external antenna(s) that has been originally tested and certified with this module.

As long as the conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Validity of using the module certification
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no

longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End product labeling
The final end product must be labeled in a visible area with the following: “Contains Transmitter Module FCC ID: 2ADHN-CLRC663.
If the size of the end product is smaller than 8x10cm, then additional FCC part 15.19 statement is required to be available in the users manual: This device complies with Part 15 of FCC rules.

Operation is subject to the following two conditions:

- This device may not cause harmful interference and
- This device must accept any interference received, including interference that may cause undesired operation.

Disposal of Products/Components after End-Of-Life

Main components of Matrix products are given below:

- Soldered Boards: At the end-of-life of the product, the soldered boards must be disposed through e- waste recyclers. If there is any legal obligation for disposal, you must check with the local authorities to locate approved e-waste recyclers in your area. It is recommended not to dispose-off soldered boards along with other waste or municipal solid waste.
- Batteries: At the end-of-life of the product, batteries must be disposed through battery recyclers. If there is any legal obligation for disposal, you may check with local authorities to locate approved batteries recyclers in your area. It is recommended not to dispose off batteries along with other waste or municipal solid waste.
- Metal Components: At the end-of-life of the product, Metal Components like Aluminum or MS enclosures and copper cables may be retained for some other suitable use or it may be given away as scrap to metal industries.
- Plastic Components: At the end-of-life of the product, plastic components must be disposed through plastic recyclers. If there is any legal obligation for disposal, you may check with local authorities to locate approved plastic recyclers in your area.

After end-of-life of the Matrix products, if you are unable to dispose-off the products or unable to locate e-waste recyclers, you may return the products to Matrix Return Material Authorization (RMA) department.

Make sure these are returned with:

- proper documentation and RMA number
- proper packing
- pre-payment of the freight and logistic costs.

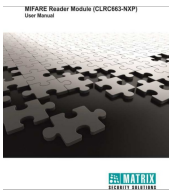
Such products will be disposed-off by Matrix.

“SAVE ENVIRONMENT SAVE EARTH”

MATRIX COMSEC

Head Office:
394-GIDC, Makarpura, Vadodara – 390010, India.
Ph: (+91)18002587747
E-mail: Tech.Support@MatrixComSec.com
www.matrixaccesscontrol.com

Documents / Resources

	MATRIX CLRC663-NXP MIFARE Reader Module [pdf] User Manual 2ADHN-CLRC663, 2ADHNCLRC663, CLRC663-NXP MIFARE Reader Module, CLRC663-NXP, CLRC663-NXP Reader Module, MIFARE Reader Module, Reader Module, Reader, Module

References

- Biometric Attendance and Access Control System - Matrix
- Biometric Attendance and Access Control System - Matrix
- Product Registration - Matrix Comsec