M5STACK STAMPS3 Development Board User Manual

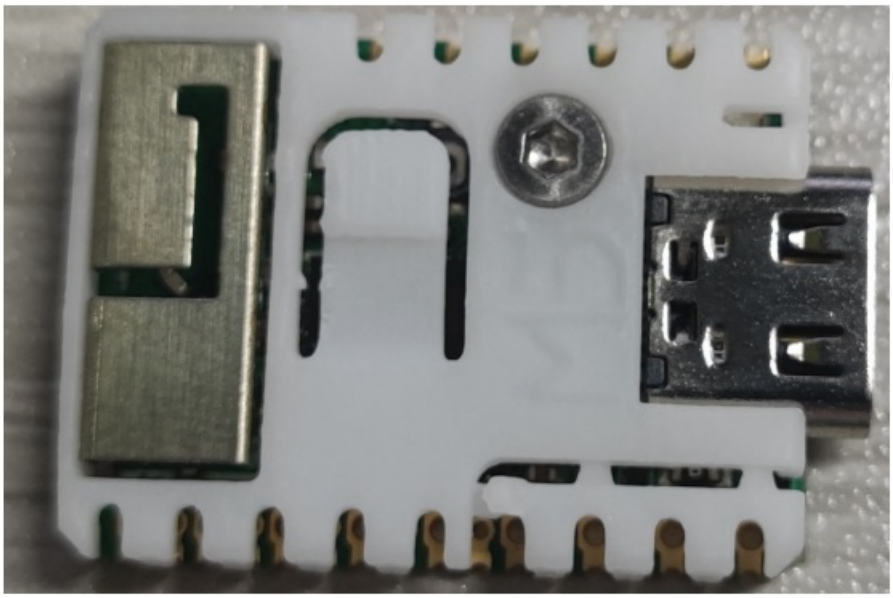
Contents

M5STACK

M5STACK STAMPS3 Development Board

Outline

StampS3 is a development board based on the ESP32-S3 chip. The board is equipped with a button and USB-C port, as well as WS2812LED and 2.4g antenna.

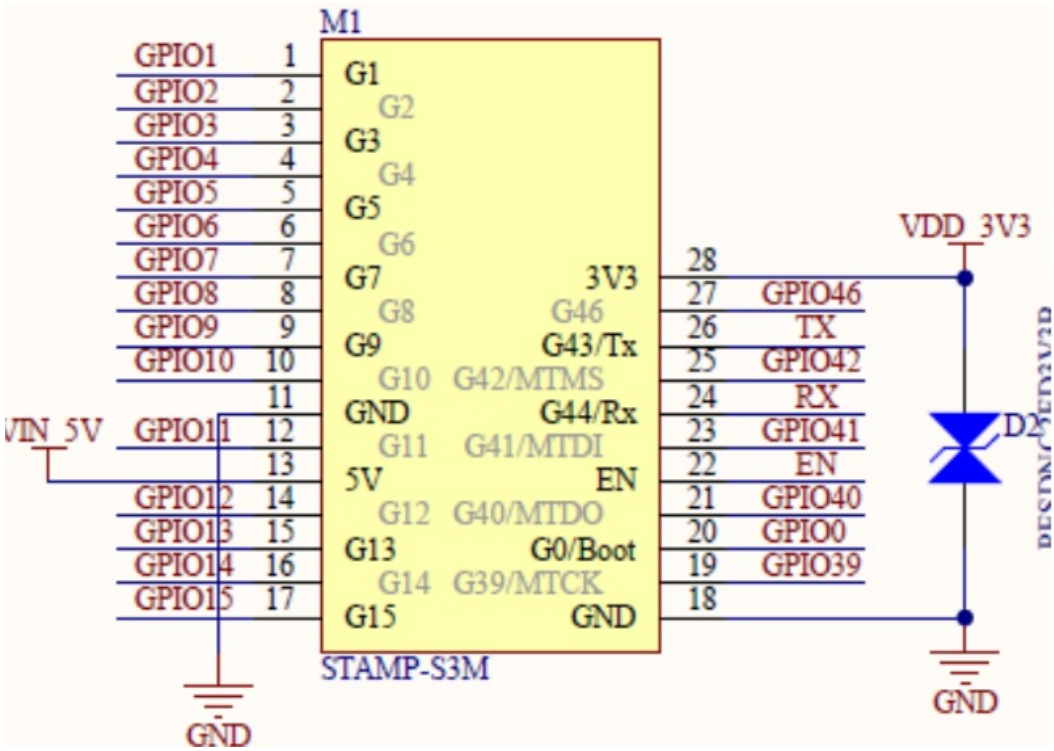


Hardware Composition
StampS3 hardware :ESP32-S3 chip, color LED, buttons, MUN3CAD01-SC DCDC.
The Esp32-s3 is a single chip with integrated 2.4ghz Wi-Fi and Bluetooth 5 (LE) in Long Range mode. The Esp32-s3 uses an Xtensa® 32-bit LX7 dual-core processor with a maximum of 240mhz, 512KB of TCM (SRAM) built in, 45 programmable GPIO pins, and rich communication interfaces. Esp32-s3 supports higher capacity octal SPI Flash and off-chip RAM, and supports user-configured data caching and instruction caching.
The power management chip is Cyntec MUN3CAD01-SC. Operating voltage range 2.7V~5.5V, supply current 1A.
StampS3 comes with everything you need to program ESP32, everything you need to do and develop

PIN DESCRIPTION

USB INTERFACE
StampS3 is configured with type-c USB interface and supports THE USB2.0 standard communication protocol

GPIO INTERFACE



StampS3 is equipped with 28p stamp hole pad, in which pins 11 and 18 are connected to GND, and pin 13 has a voltage of 5V, which can supply power to the development board or other devices when connecting external USB. Pin 28 is 3.3V output of the development board, and other pins are GPIO interface.

FUNCTIONAL DESCRIPTION

This chapter describes the ESP32-S3 various modules and functions.

CPU AND MEMORY

Xtensa® dual-core 32-bit LX7 microprocessor,up to 240 MHz

- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC
- SPI, Dual SPI, Quad SPI, Octal SPI, QPI and OPI interfaces that allow connection to multiple flash and external RAM
- Flash controller with cache is supported
- Flash in-Circuit Programming (ICP) is supported

STORAGE DESCRIPTION

External Flash and RAM

ESP32-S3 supports SPI, Dual SPI, Quad SPI, Octal SPI, QPI and OPI interfaces that allow connection to multiple external flash and RAM. The external flash and RAM can be mapped into the CPU instruction memory space and read-only data memory space. The external RAM can also be mapped into the CPU data memory space. ESP32-S3 supports up to 1GB of external flash and RAM, and hardware encryption/decryption based on XTS-AES to protect users'programs and data in flash and external RAM.

Through high-speed caches, ESP32-S3 can support at a time up to:

- External flash or RAM mapped into 32 MB instruction space as individual blocks of 64 KB
- External RAM mapped into 32 MB data space as individual blocks of 64 KB. 8-bit, 16-bit, 32-bit, and 128-bit reads and writes are supported. External flash can also be mapped into 32 MB data space as individual blocks of 64 KB, but only supporting 8-bit, 16-bit, 32- bit and 128-bit reads

CPU CLOCK
The CPU clock has three possible sources:

- External main crystal clock
- Internal fast RC oscillator (typically about 17.5 MHz, and adjustable)
- PLL clock

  The application can select the clock source from the three clocks above.

  The selected clock source drives the CPU clock directly, or after division, depending on the application. Once the CPU is reset, the default clock source would be the external main crystal clock divided by 2.

RTC AND LOWPOWER MANAGEMENT
With the use of advanced power-management technologies, ESP32-S3 can switch between different power modes. (see table1)

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- Modemsleep mode: The CPU is operational and the clock speed can be reduced. The wireless baseband and radio are disabled, but wireless connection can remain active.
- Lightsleep mode: The CPU is paused. The RTC peripherals, as well as the ULP coprocessor can be woken up periodically by the timer. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip. Wireless connection can remain active. Users can optionally decide what peripherals to shut down/keep on (refer

  to Figure 1), for power-saving purpose.
- Deepsleep mode: CPU and most peripherals are powered down. Only the RTC memory is powered on and RTC peripherals are optional. Wi-Fi connection data are stored in the RTC memory. The

  ULP coprocessor is functional.

Current Consumption in LowPower Modes: TABLE 1

Work mode	Description	Typ (μA)
Light-sleep	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance.	240[1]
Deep-sleep	RTC memory and RTC peripherals are powered on.	8
	RTC memory is powered on. RTC peripherals are powered off.	7
Power off	CHIP_PU is set to low level. The chip is powered off.	1

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SPI	Voltage applied to power supply pins per power domain	–0.3	3.6	V
I_{output} *	Cumulative IO output current	—	1500	mA
T_{STORE}	Storage temperature	–40	150	°C

1. VIO to the power supply pad, Refer ESP32 Technical Specification Appendix IO_MUX, as SD_CLK of Power supply for VDD_SDIO.

WIFI RADIO AND BASEBAND
The ESP32-S3 Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- 802.11n 0.4 µs guard-interval
- Data rate up to 150 Mbps
- RX STBC (single spatial stream)
- Adjustable transmitting power
- Antenna diversity:

  ESP32-S3 supports antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

BLUETOOTH LE RF TRANSMITTER (TX)

SPECIFICATIONS

Table 3: Transmitter Characteristics Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–25.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	2.50	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	2.00	—	kHz
	Max $\lvert f_n - f_{n-5} \rvert$	—	1.39	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.80	—	kHz
Modulation characteristics	$\Delta\, f1_{avg}$	—	249.00	—	kHz
	Min $\Delta\, f2_{max}$ (for at least 99.9% of all $\Delta\, f2_{max}$)	—	198.00	—	kHz
	$\Delta\, f2_{avg}/\Delta\, f1_{avg}$	—	0.86	—	—
In-band spurious emissions	±2 MHz offset	—	–37.00	—	dBm
	±3 MHz offset	—	–42.00	—	dBm
	>±3 MHz offset	—	–44.00	—	dBm

BLUETOOTH LE RF RECEIVER (RX)

SPECIFICATIONS

Table 35: Receiver Characteristics Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–97.5	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	9	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–3	—	dB
	F = F0 – 1 MHz	—	–3	—	dB
	F = F0 + 2 MHz	—	–28	—	dB
	F = F0 – 2 MHz	—	–30	—	dB
	F = F0 + 3 MHz	—	–31	—	dB
	F = F0 – 3 MHz	—	–33	—	dB

Documents / Resources

M5STACK-STAMPS3 M5STACK	M5STACK STAMPS3 Development Board [pdf] User Manual STAMPS3, Development Board, STAMPS3 Development Board, Board