M5STACK M5Core2 V1.1 ESP32 IoT Development Kit Owner's Manual

Contents

M5STACK

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Product Information

Year	2020
Version	V0.01

Outline
M5Core2 1.1 is an ESP32 board based on the ESP32-D0WDQ6-V3 chip and features a 2-inch TFT screen. The board is made of PC+ABC.

Hardware Composition
The hardware components of CORE2 include

- ESP32-D0WDQ6-V3 chip
- TFT screen
- Green LED
- Button

- GROVE interface
- TypeC-to-USB interface
- Power Management chip
- Battery

The ESP32-D0WDQ6-V3 chip is a dual-core system with two Harvard Architecture Xtensa LX6 CPUs. It has embedded memory, external memory, and peripherals located on the data bus and/or the instruction bus of these CPUs. The address mapping of the two CPUs is symmetric, except for some minor exceptions. Multiple peripherals in the system can access embedded memory via DMA.

TFT Screen
The TFT screen is a 2-inch color screen driven by ILI9342C with a resolution of 320 x 240. It operates at a voltage range of 2.6~3.3V and has a working temperature range of -10~5°C.

Power Management Chip
The Power Management chip used is X-Powers's AXP192. It operates at an input voltage range of 2.9V~6.3V and supports a charging current of 1.4A.

Functional Description
This chapter describes the various modules and functions of the ESP32-D0WDQ6-V3 chip.

CPU and Memory
The ESP32-D0WDQ6-V3 chip features Xtensa single-/dual-core 32-bit LX6 microprocessors with a maximum speed of up to 600MIPS. The CPU has 448 KB ROM, 520 KB SRAM, and an additional 16 KB SRAM in RTC. It supports multiple flash/SRAM chips through QSPI.

Storage Description

- The ESP32 supports multiple external QSPI flash and static random access memory (SRAM) with hardware-based AES encryption for user program and data protection.
- The ESP32 accesses external QSPI Flash and SRAM through caching. It can map up to 16 MB of external Flash code space into the CPU, supporting 8-bit, 16-bit, and 32-bit access, and code execution. It can also map up to 8 MB external Flash and SRAM to the CPU data space, supporting 8-bit, 16-bit, and 32-bit access. The Flash supports only read operations, while the SRAM supports both read and write operations.

PIN DESCRIPTION

USB INTERFACE
M5CAMREA Configuration Type-C type USB interface, support USB2.0 standard communication protocol.

GROVE INTERFACE
4p disposed pitch of 2.0mm M5CAMREA GROVE interfaces, internal wiring and GND, 5V, GPIO32, GPIO33 connected.

FUNCTIONAL DESCRIPTION

This chapter describes the ESP32-D0WDQ6-V3 various modules and functions.

CPU AND MEMORY
Xtensa single-/dual-core32-bitLX6microprocessor(s), upto600MIPS (200MIPSforESP32-S0WD/ESP32-U4WDH, 400 MIPS for ESP32-D2WD)

- 448 KB ROM
- 520 KB SRAM
- 16 KB SRAM in RTC
- QSPI supports multiple flash/SRAM chips

STORAGE DESCRIPTION

External Flash and SRAM
ESP32 support multiple external QSPI flash and static random access memory (SRAM), having a hardware-based AES encryption to protect the user programs and data.

- ESP32 access external QSPI Flash and SRAM by caching. Up to 16 MB external Flash code space is mapped into the CPU, supports 8-bit, 16-bit and 32-bit access, and can execute code.
- Up to 8 MB external Flash and SRAM mapped to the CPU data space, support for 8-bit, 16-bit and 32-bit access. Flash supports only read operations, SRAM supports read and write operations.

CRYSTAL
External 2 MHz~60 MHz crystal oscillator (40 MHz only for Wi-Fi/BT functionality)

RTC MANAGEMENT AND LOW POWER CONSUMPTION
ESP32 uses advanced power management techniques may be switched between different power saving modes. (See Table 5).

• Power saving mode

- Active Mode: RF chip is operating. Chip may receive and transmit a sounding signal.
- Modem-sleep mode: CPU can run, the clock may be configured. Wi-Fi /Bluetooth baseband and RF
- Light-sleep mode: CPU suspended. RTC and memory and peripherals ULP coprocessor operation. Any wake-up event (MAC, host, RTC timer or external interrupt) will wake up the chip.
- Deep-sleep mode: only the RTC memory and peripherals in a working state. Wi-Fi and Bluetooth connectivity data stored in the RTC. ULP coprocessor can work.
- Hibernation Mode: 8 MHz oscillator and a built-in coprocessor ULP are disabled. RTC memory to restore the power supply is cut off. Only one RTC clock timer located on the slow clock and some RTC GPIO at work. RTC

RTC clock or timer can wake up from the GPIO Hibernation mode.

• **Deep-sleep mode**

- Related sleep mode: power save mode switching between Active, Modem-sleep, Light-sleep mode. CPU, Wi-Fi, Bluetooth, and radio preset time interval to be awakened, to ensure connection Wi-Fi / Bluetooth.
- Ultra Low-power sensor monitoring methods: the main system is Deep-sleep mode, ULP coprocessor is periodically opened or closed to measure sensor data. The sensor measures data, ULP coprocessor decide whether to wake up the main system.

Functions in different power consumption modes: **TABLE 5**

Power consumption mode	Active	Modem-sleep	Light-sleep	Deep-sleep	Hibernation
Sleep mode	Associated sleep mode			Ultra low-power Sensor measures data	-
CPU	open	open	pause	close	close
Wi-Fi/Bluetooth Radio	open	open	close	close	close
RTC memory	open	open	open	open	close
ULP coprocessor	open	open	open	open/close	close

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

Note

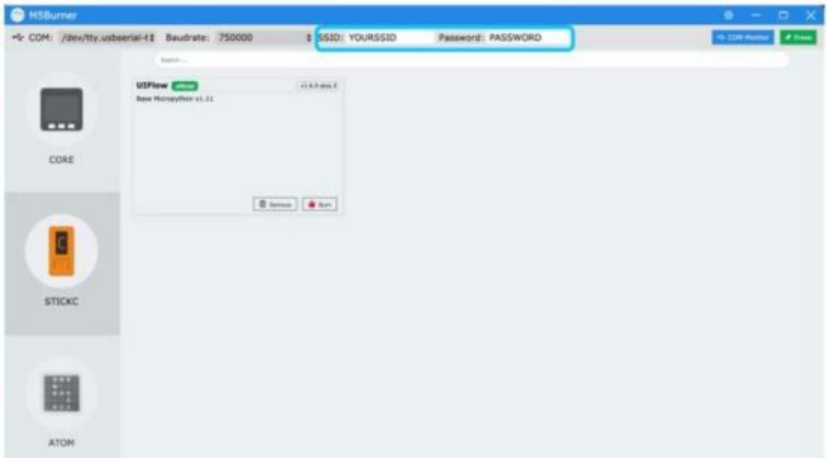
- This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.
- This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.
- If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures
    - Reorient or relocate the receiving antenna.
    - Increase the separation between the equipment and receiver.
    - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
    - Consult the dealer or an experienced radio/TV technician for help.
- This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Configure WIFI

UIFlow provides both offl.ine and web veruon of the programmer. When using the web version, we need to configure a WiFi connection for the device. The following de.scribes two ways to configure \Vlfi connection for the device (Bum configuration and A.P hotspot configuration).

Burn configuration WiFi{recommend)

I O U!Flow-1.5.4 and versions above can write WiFi inlormat1on directly through M5Burner .



AP hotspot configuration WiFi

1. Press and tlold the power button on the left to turn on the machine. If W1FI Is not configured, the system will automat1ca!ly enter the network configurallon mode when it Is turned on for the first t,me. Suppose you want to re-enter the network configuration mode alter runn,ng other programs. you can refer to the operation below. Alter the UIFlow Logo appears at startup, quickly click the Home button (center MS button) to enter the configuration page. Press the button on the right side of the fuselage to switch the option to Setting, and press the Home button to confirm. Press the right button to switch the option to WIFi Setting, press the Home button to confirm, and start the configuration.

2. After successfully connecting to the hotspot w,th your mot>tle phone, open the mobile phone browser to scan the QR code on the screen or directly access 192.188.4.1. enter the page to fill in your personal WIFI information. and ciick Configure to record your WiFi information. The device wm restart automatteally after successfully configuring and enter programming mode.

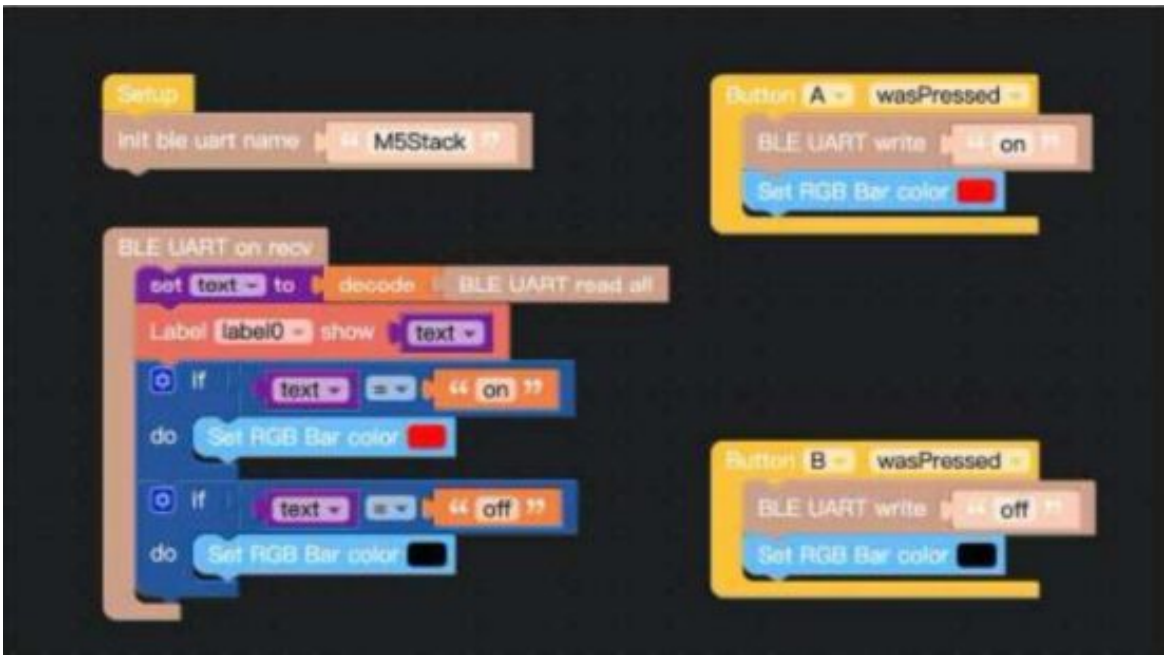
Note: Special characters such as “space” are not allowed in the configured W,Fi 1rtformat10n.

BLEUART Function Description

Establish Bluetooth connection and enable Bluetooth passthrough service.

Instructions

Bluetooth gastrough connection and scad co / off control LED



Documents / Resources

M5Core2 v1.1 M5STACK	M5STACK M5Core2 V1.1 ESP32 IoT Development Kit [pdf] Owner's Manual M5CORE2V11, 2AN3WM5CORE2V11, M5Core2 V1.1 ESP32 IoT Development Kit, M5Core2 V1.1, ESP32 IoT Development Kit, IoT Development Kit