M5STACK 19777 Core Ink Development Kit User Manual

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User Manual

Contents

OUTLINE

CORE PINK is an ESP32 board that is based on the ESP32-PICO-D4 module, and contained 1.54-inch eINK. The board is made of PC+ABC.

Hardware Composition

The hardware of COREINK: ESP32-PICO-D4 chip, eLNK, LED, Button, GROVE interface, TypeC-to-USB interface, RTC, Power Management chip battery.
ESP32- PICO-D4 is a System-in-Package (SiP) module that is based on ESP32, providing complete Wi-Fi and Bluetooth functionalities. The module integrates a 4-MB SPI flash. ESP32-PICO-D4 integrates all peripheral components seamlessly, including a crystal oscillator, flash, filter capacitors, and RF matching links in one single package.

1.54” E-Paper Display
The display is a TFT active matrix electrophoretic display, with an interface and a reference system design. The 1 . 54 ” active area contains 200×200 pixels, and has1bit white/black full display capabilities. An integrated circuit contains a gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOMand border are supplied with each panel

PIN DESCRIPTION

USB INTERFACE
COREINK Configuration Type-C type USB interface, support USB2.0 standard communication protocol.

GROVE INTERFACE
4p disposed pitch of 2.0mm COREINK GROVE interfaces, internal wiring and GND, 5V, GPIO4, GPIO13 connected.

FUNCTIONAL DESCRIPTION

This chapter describes the ESP32-PICO-D4 various modules and functions.

CPU AND MEMORY

ESP32-PICO-D4 contains two low-power Xtensa® 32-bit LX6 MCU. On-chip memory comprising:

- 448-KB of ROM, and the program starts for the kernel function calls
- For a 520 KB instruction and data storage chip SRAM (including flash memory 8 KB RTC)
- RTC flash memory of 8 KB SRAM, when the RTC can be started in Deep-sleep mode, and for storing data accessed by the main CPU
- RTC slow memory, of 8 KB SRAM, can be accessed by the coprocessor in Deep-sleep mode
- Of 1 kbit of use, which is a 256-bit system-specific (MAC address and a chipset); the remaining 768 bits are reserved for the user program, these Flash programs include encryption and chip ID

STORAGE DESCRIPTION

External Flash and SRAM

ESP32 support multiple external QSPI flash and static random access memory (SRAM), having a hardware-based AES encryption to protect the user programs and data.

- ESP32 access external QSPI Flash and SRAM by caching. Up to 16 MB of external Flash code space is mapped into the CPU, supports 8-bit, 16-bit, and 32-bit access, and can execute code.
- Up to 8 MB of external Flash and SRAM mapped to the CPU data space, support for 8-bit, 16-bit, and 32-bit access. Flash supports only read operations, and SRAM supports read and write operations.

ESP32-PICO-D4 4 MB of integrated SPI Flash, the code can be mapped into CPU space, support for 8-bit, 16-bit, and 32-bit access, and can execute code. Pin GPIO6 ESP32 of, GPIO7, GPIO8, GPIO9, GPIO10, and GPIO11 for connecting module integrated SPI Flash, not recommended for other functions.

CRYSTAL

- ESP32-PICO-D4 integrates a 40 MHz crystal oscillator.

RTC MANAGEMENT AND LOW POWER CONSUMPTION

ESP32 uses advanced power management techniques that may be switched between different power-saving modes. (See Table 5).

- Power saving mode

  – Active Mode: RF chip is operating. The chip may receive and transmit a sounding signal.

  – Modem-sleep mode: The CPU can run, and the clock may be configured. Wi-Fi / Bluetooth baseband and RF

  – Light-sleep mode: CPU suspended. RTC and memory and peripherals ULP coprocessor operation. Any wake-up event (MAC, host, RTC timer, or external interrupt) will wake up the chip.

  – Deep-sleep mode: only the RTC memory and peripherals are in a working state. Wi-Fi and Bluetooth connectivity data are stored in the RTC. ULP coprocessor can work.

  – Hibernation Mode: 8 MHz oscillator and a built-in coprocessor ULP are disabled. RTC memory to restore the power supply is cut off. Only one RTC clock timer is located on the slow clock and some RTC GPIO at work. RTC RTC clock or timer can wake up from the GPIO Hibernation mode.

- Deep-sleep mode

  – related sleep mode: power saves mode switching between Active, Modem-sleep, and Light-sleep mode. CPU, Wi-Fi, Bluetooth, and radio preset time interval to be awakened, to ensure connection Wi-Fi / Bluetooth.

  – Ultra Low-power sensor monitoring methods: the main system is in Deep-sleep mode, ULP coprocessor is periodically opened or closed to measure sensor data. The sensor measures data, ULP coprocessor decides whether to wake up the main system.

Power consumption mo de	Active	Modem-sleep	Light-sleep	Deep-sleep	Hibernation
Sleep mode	Associated sleep mode			Ultra-low-power Se nsor measures data	
CPU	open	open	pause	close	close
Wi-Fi/Bluetooth Radio	open	open	close	close	close
RTC memory	open	open	open	open	close
ULP coprocessor	open	open	open	open/close	close

ELECTRICAL CHARACTERISTICS

LIMIT PARAMETERS

Table 8: Limiting values

Symbol	**Parameter**	**Min**	**Max**	**Unit**
VDD33	Power supply voltage	– 0.3	4.	V
1 out put[1]	Cumulative I0 output current	–	1,100	mA
T store	Storage temperature	-40	150	ºC

1. VIO to the power supply pad, Refer to ESP32 Technical Specification Appendix

IO_MUX, as SD_CLK of Power supply for VDD_SDIO.

Press and hold the side power button for two seconds to start the device. Press and hold for more than 6 seconds to turn off the device. Switch to the photo mode through the Home screen, and the avatar that can be obtained through the camera 0is displayed on the TFT screen. The USB cable must be connected when working, and the lithium battery is used for short-term storage to prevent power failure.

FCC Statement
Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

Note:
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.
This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

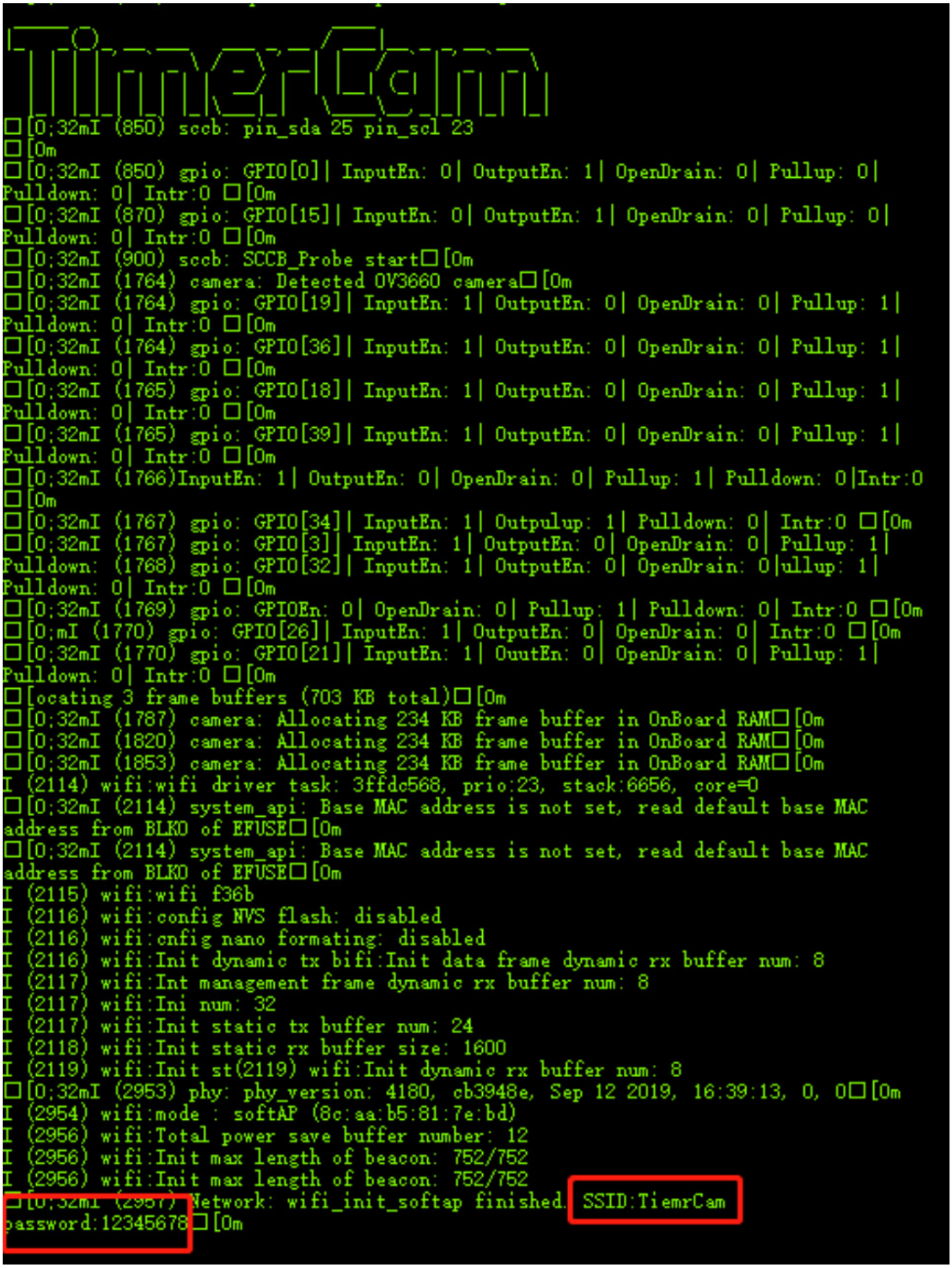
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator& your body.

ESP32TimerCam/TimerCameraF/TimerCameraX Quick Start

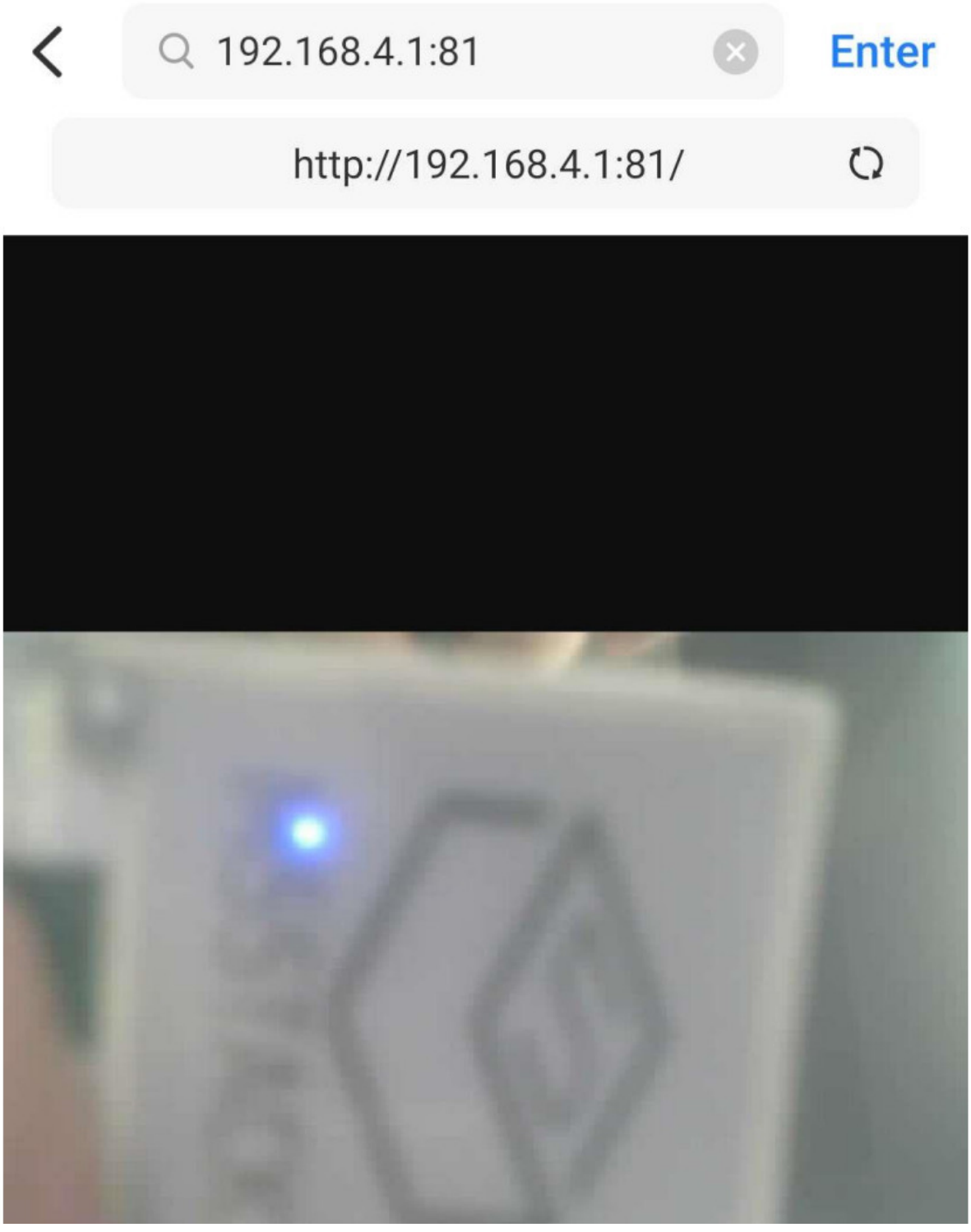
With preloaded firmware, your ESP32TimerCam,/TimerCameraF/TimerCameraX would run right after power on.

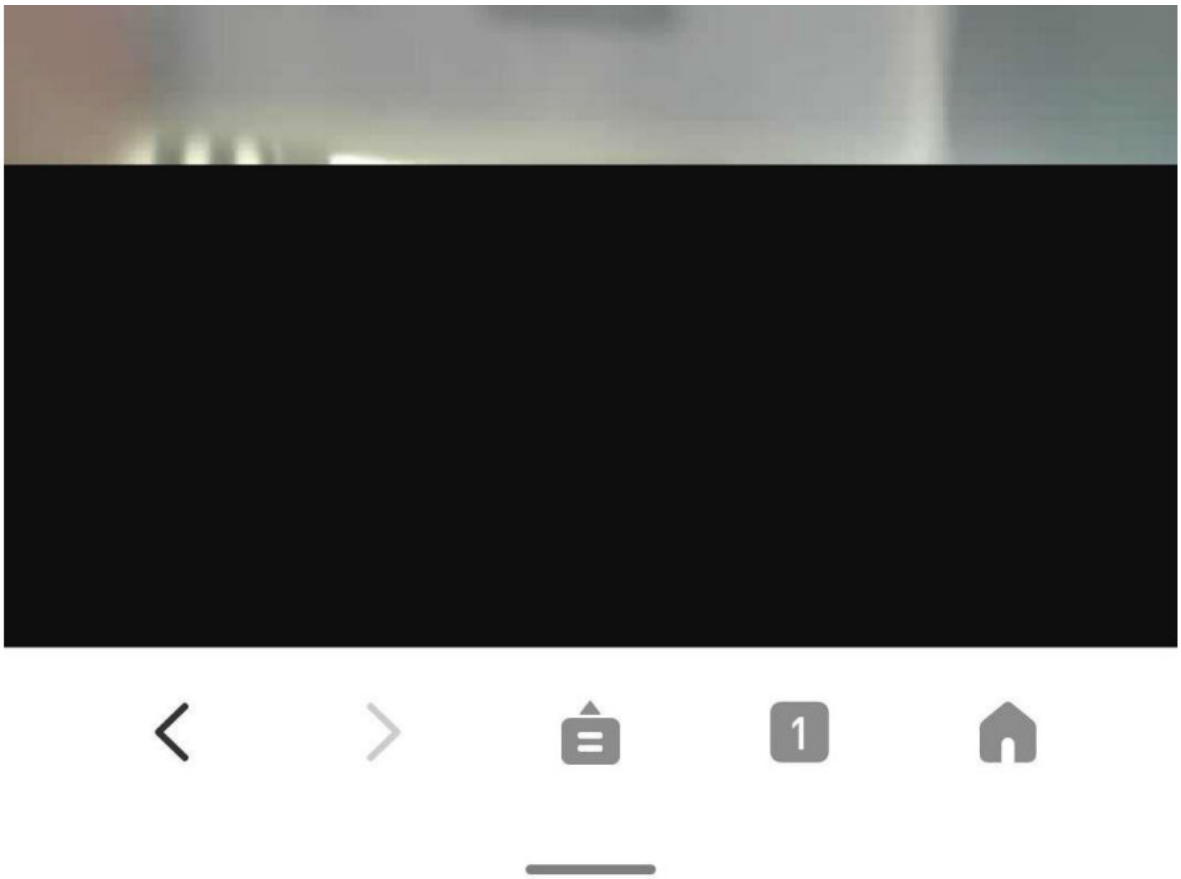
1. Power on the cable into ESP32TimerCam/TimerCameraF/TimerCameraX by USB cable. Baud rate 921600.



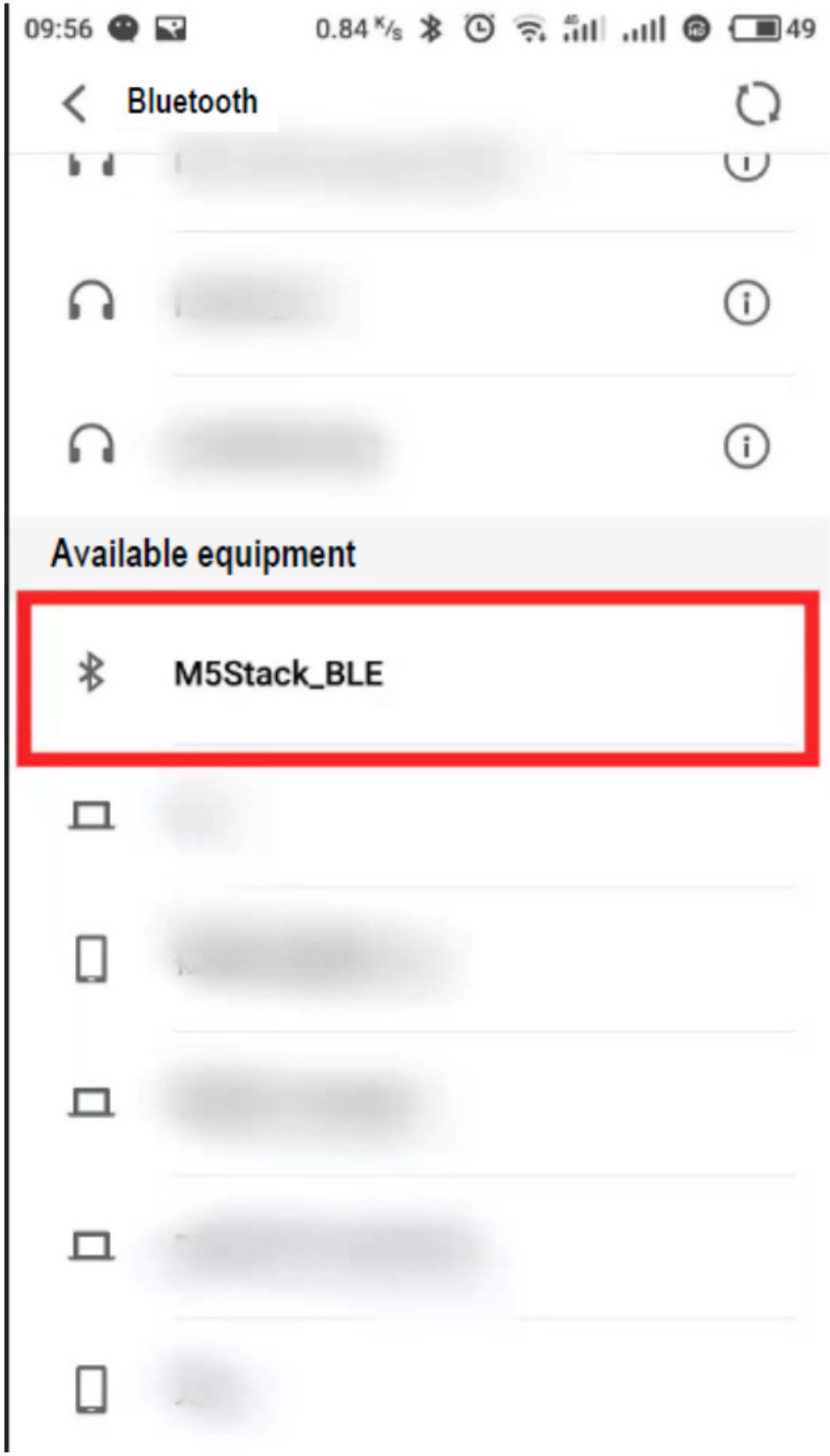
2. After waiting for a few seconds, Wi-Fi scan an AP named “TimerCam” with your computer(or mobile phone), and connects it.

3. Open up the browser on the computer(or mobile phone), and visit the URL **http://192.168.4.1:81.** At the moment, you can see the real-time transmission of video by ESP32TimerCam/TimerCameraF/TimerCameraX on the browser.





A Bluetooth name “m5stack” is found on the mobile phone_ BLE”



Documents / Resources

COREINK M5STACK	**M5STACK 19777 Core Ink Development Kit** [pdf] User Manual M5COREINK, 2AN3WM5COREINK, 19777 Core Ink Development Kit, 19777, Core Ink Development Kit