TURBO MAINBOARD
4.77/10MHZ
USER'S MANUAL

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CHAPTER 1 THE SYSTEM BOARD

1-1 Introduction

The 10MHz – TURBO system board fits horizontally in the base of the system unit and is approximately 8½ x 12 inches. It is a double-sided PCB using DC power. A signal from the power supply enters the board through two six-pin connectors. Other connectors on the board are for attaching the keyboard and speaker. Eight 62-pin card edge sockets are also mounted on the board. The I/O channel is bussed across these eight I/O slots.

A "Dual-in-Line Package (DIP) switch (SW1) (one eight switch pack) is mounted on the board and can be read under program control. The DIP switch provides the system software with information about the installed options.

The system board has five functions: the processor subsystem and its support elements, the Read Only Memory (ROM) subsystem the Read/Write (R/W) Memory subsystem, integrated I/O adapters, and I/O channel.

The heart of the 10MHz Turbo system board is the Intel 8088-1 or qualified 8088-2 microprocessor. This processor is an 8-bit external bus version of Intel's 16 bit 8086 processor, and is software compatible with the 8086. Thus, the 8088 supports 16 bit operations, including multiply and divide and supports 20 bits of addressable memory (1 megabyte of storage).

It also operates in a maximum mode, so a co-processor can be added as a feature. The processor operates in two modes which can be switched, namely the Normal mode and the Turbo mode. When the processor is operating at 4.77MHz in the Normal mode, the frequency, which is derived from a 14.318MHz crystal, is divided by 3 for the processor clock, and by 4 to obtain the 3.58 MHz color burts signal required for color television. When the processor is operating in the 10 MHz Turbo mode, the frequency is derived from 30 MHz.

– DMA –

Three of the four DMA channels are available on the I/O bus and support high speed data transfers between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic memory. This is done by programming a channel of the timer counter device to request periodically a dummy DMA transfer. This action creates a memory read cycle, which is available to refresh dynamic storage, both on the system board and in the system expansion slots. All DMA data transfers, except the refresh channel, take five processor clocks of 210 ns, or 1.05 μs if the processor ready line is not deactivated. Refreshing DMA cycles takes four clocks or 840 ns.

– TIMER –

The three programmable timer/counters are used by the system as follows: Channel 0 is used as a general purpose timer, providing a constant time base for implementing a time-of-day clock; Channel 1 is used to time and request refresh cycles from the DMA channel; and Channel 2 is used to support the tone generation for the audio speaker. Each channel has a minimum timing resolution of 1.05 μs.

– INTERRUPT –

Of the eight pricritized levels of interrupt, six are bussed to the system expansion slots for use by feature cards. Two levels are used on the system board. Level 0, the highest priority, is attached to Channel 0 of the timer/counter and provides a periodic interrupt for the time-of-day clock. Level 1 is attached to the keyboard adapter circuits and receives an interrupt for each scan code sent by the keyboard. The Non-Maskable Interrupt (NMI) of the 8088 is used to report memory parity errors.

– MEMORY –

The system board supports both ROM/EPROM and R/W memory. It has space for 32KB x 1 and 8 KB x 1 of ROM or EPROM. This ROM contains a power-on self-test, I/O drivers, dot patterns for 128 characters in graphics mode, and a diskette.

The system board also has from 256KB to 640KB of R/W memory. A minimum system has 256KB of memory.

– KEYBOARD –

The system board contains the adapter circuits for attaching the serial interface from the keyboard. These circuits generate an interrupt to the processor, when a complete scan code is received. The interface can request execution of a diagnostic test in the keyboard.

The keyboard interface is a 5-pin DIN connector on the system board that extends through the rear panel of the system unit.

– SPEAKER –

The system unit has a 2¼-inch audio speaker. The speaker's control circuits and driver are on the system board. The speaker connects through a 2-wire interface that attaches to a 3-pin connector on the system board.

The speaker drive circuit is capable of providing approximately ½ watt of power. The control circuits allow the speaker to be driven three different ways: 1) a direct program control register bit may be toggled to generate a pulse train; 2) the output from Channel 2 of the timer counter may be programmed to generate a waveform to the speaker; 3) the clock input to the timer counter can be modulated with a program controlled by the I/O register bit. All three methods may be performed simultaneously.

1-2 Expansion I/O Channel

The I/O channel is an extension of the 8088 microprocessor bus. It is, however, demultiplexed, repowered, and enhanced by the addition of interrupts and Direct Memory Access (DMA) functions.

The I/O channel contains an 8 bit, bidirectional data bus, with 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines, a channel check line, and power and a ground for the adapters. Four voltage levels are provided for I/O cards: +5Vdc, –5Vdc, +12Vdc, and –12dc. These functions are provided in a 62-pin connector with 100-mil card tab spacing.

A "ready" line is available on the I/O channel to allow operation with slow I/O or memory devices. If the channel's ready line is not activated by an addressed device, all processor-generated memory read and write cycles take four 210-ns/clock or 840-ns/byte. All processor-generated I/O read and write cycles require five clocks for a cycle time of 1.05 μs/byte. Refresh cycles occur once every 72 clocks (approximately 15 μs) and require four clocks or approximately 7% of the bus bandwidth.

I/O devices are addressed using I/O mapped address space. The channel is designed so that 768 I/O devices addressed are available to the I/O channel cards.

A channel check line exists for reporting error conditions to the processor. Activating this line results in a Non-Maskable Interrupt (NMI) to the 8088 processor. Memory expansion options use this line to report parity errors.

The I/O channel is repowered to provide sufficient drive, to power all eight (J1 through J8, expansion slots assuming two Low-Power Schorttky (LS) loads per slot. The I/O adapters typically use only one load.

1-3 I/O Channel Description

The following is a description of the PC/XT I/O Channel. All lines are TTL-compatible.

I/O Signal Description

OSC, Oscillator:

High speed clock with a 70-ns period (14.31818 MHz). It has a 50% duty cycle.

CLK, System Clock:

It operates at one-third the frequency of the oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.

RESET:

This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of the clock and is active high.

A0-A19, Address Bits 0 to 19:

These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the Least Significant Bit (LSB) and A19 is the Most Significant Bit (MSB). These lines are generated by either the processor or the DMA controller. They are active high.

D0-D7, I/O Data Bits 0 to 7:

These lines provide data bus bits 0 to 7 for the processor

memory, and I/O devices. D0 is the Least Significant Bit (LSB) and D7 is the Most Significant Bit (MSB). These lines are active high.

ALE, Address Latch Enable:

This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the falling edge of ALE.

I/O CH CK, I/O Channel Check:

This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.

I/O CH RDY, I/O Channel Ready:

This line, normally high (ready), can be pulled low (not ready) by a memory or an I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles.

IRQ2-IRQ7, Interrupt Request 2 to 7:

These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is gener-

ated by raising an IRQ line (low to high) and holding it high, until it is acknowledged by the processor (interrupt service routine).

IOR, I/O Read Command:

This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

IOW, I/O Write Command:

This command line instructs an I/O device, to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMR, Memory Read Command:

This command line instructs the memory to drive its data into the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMW, Memory Write Command:

This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

DRQ1-DRQ3, DMA Request 1 to 3:

These lines are for asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK

line goes active.

DACK 0– 3 – DAM Acknowledge 0 to 3:

These lines are DACK3 used to acknowledge DMA requests (DRQ1 DRQ3) and to refresh system dynamic memory (DACK 0) They are active low

AEN, Address Enable:

This line is used to negate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control over the address bus, the data bus, the read command lines (memory and I/O), and the write command lines (memory and I/O).

I/C, Terminal Count:

This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

CARD SLCTD, Card Selected:

This line is activated by cards in expansion slot J8. It signals the system board that the card has been selected and that appropriate drivers on the system board should be disabled either to read from, or write to, expansion slot J2. Connections J1 through J8 are tied together at this pin, but the system board should be driven by an open collector device.

The following voltages are available on the system board I/O channel:

+5 Vdc ± 5%, located on 2 connector pins
−5 Vdc ± 10%, located on 1 connector pin
+ 12 Vdc ± 5%, located on 1 connector pin
− 12 Vdc ± 10%, located on 1 connector pin
GND (Ground), located on 3 connector pins

1.4 Speaker Interface

The sound system has a small, permanent magnet, 2¼ inch speaker. The speaker can be driven from one or two sources:

- An 8255A-5 PPI output bit. The address and bit are defined in the "I/O Address Map"

- A timer clock channel, the output of which is programmable within the functions of the 8253-5 timer when using a 1.19-MHz clock input. The timer gate also is controlled by an 8255A-5 PPI outputport bit. Address and bit assignment are in the "I/O Address Map"

The speaker connection is a 2-pin 90°-degree connector, See "System Board Component Diagram", earlier in this section, for speaker connection or placement.

CHAPTER 2
NORMAL/TURBO MODE OPERATION

2-1 ADVANTAGES OF THE 10 MHz TURBO

The difference between the PIM-TB10-Z and other mainboards is the approximate 110% increase in speed of program execution made possible with the 8088-1 or the qualified 8088-2 CPU, both of which operate at the faster frequency of 10 MHz. Ordinary mainboards operate at a slower clock speed of 4.77 MHz.

This Board runs on a dual clock system: in Normal mode the clock speed is 4.77 MHz, while in Turbo mode, the speed is increased to 10 MHz.

NOTE: Do not use RAM memory on the interface card because its original design may not be compatible with the 10 MHz CPU at access time. Use memory on the mainboard and use 4164 and 41256 and 4464 access time within 120 ns.

FOR EXAMPLE:

	4164	41256	4454
NEC	D4164C	D41256C	D4464C
HITACHI	HM4846	HM50256	HM50464
MITSUBISHI	M5K4164	M5M4256P	M5M4464P
PANASONIC	MN4164	MN41256	MN4464

NOTE: Use the NEC 70108-10 to enable speed up to 380% faster than an ordinary XT

2-2 TO OBTAIN TURBO MODE AT 10 MHz

The system board supports both a software switch and a hardware switch to allow transferring from Normal mode to Turbo mode. The switches may be used interchangeably.

A) SOFTWARE SWITCH

The software switch is available when using Turbo BIOS only.

1) To turn on Turbo mode

Press and hold down the "Ctrl" (control) and "alt" (alternative) keys and then press the "–" (minus) key. The cursor will then appear on the screen as a "■" (box). The Turbo LED will light up, indicating that the computer is in Turbo mode.

2) To return to Normal mode

Press and hold down the "Ctrl" (control) and "Alt" (alternative) keys and then press the "–" (minus) key. The cursor will then appear on the screen as a "–" (dash) and the Turbo LED will turn off.

3) Software Switch Jump Set.

JP7

JP8

B) HARDWARE SWITCH JUMPER SETTING

1) To turn on Turbo mode

Push the Turbo switch into the "OFF" position to turn on Turbo mode at 10 MHz. The Turbo LED will come on to indicate that the computer is in Turbo mode.

2) To return to Normal mode

Push the Turbo switch into the "ON" position to return to Normal mode at 4.77 MHz. The Turbo LED will turn off to indicate that the computer is in Normal mode.

2) Hardware Switch Jump Set.

JP7 JP8

NOTE: 1. The pushbutton leads to JP6 on the mainboard. When the button is pushed in, JP6 is in a closed circuit.

2. In the 10 MHz Turbo mode, the computer can run Lotus 1-2-3, CP/M 86, DBASE II and many other well-known IBM package programs. However, Normal mode (4.77 MHz) should be used to run Copywrite.

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B) HARDWARE SWITCH JUMPER SETTING

1) To turn on Turbo mode

Push the Turbo switch into the "OFF" position to turn on Turbo mode at 10 MHz. The Turbo LED will come on to indicate that the computer is in Turbo mode.

2) To return to Normal mode

Push the Turbo switch into the "ON" position to return to Normal mode at 4.77 MHz. The Turbo LED will turn off to indicate that the computer is in Normal mode.

3) Hardware Switch Jump Set.

4) Software & Hardware Switch Jump Set.

NOTE: 1. The pushbutton leads to JP6 on the mainboard. When the button is pushed in, JP6 is in a closed circuit.

2. In the 10 MHz Turbo mode, the computer can run Lotus 1-2-3, CP/M 86, DBASE II and many other well known IBM package programs. However, Normal mode (4.77 MHz) should be used to run Copyware.

CHAPTER 3
CONNECTORS AND SWITCH SETTING

3-1 Connectors

The system board has the following connectors:

Two power-supply connectors (P1 and P2)

- Speaker connector (JP1)
- Keyboard connector (JP2)
- Keylock connector (JP3)
- Reset connector (JP4)
- Power LED and Turbo LED connector (JP5)

A) Power Supply Connectors (P1 and P2)

Pin	Assignments	Connector
1	Power good	P1
2	Not used	
3	+ 12 Vdc	
4	– 12 Vdc	
5	Ground	
6	Ground	
1	Ground	P2
2	Ground	
3	– 5 Vdc	
4	+ 5 Vdc	
5	+ 5 Vdc	
6	+ 5 Vdc	

B) Speaker Connector (JP1)

The pin assignments for the 2-pin, Berg scrip are as follows

Pin	Function
1	Data out
2	+ 5 Vec

C) Keyboard Connector (JP2)

The keyboard connector is a 5-pin, DIN connector. The pin assignments are Shown below

Pin	Assignments
1	Keyboard clock
2	Keyboard data
3	Keyboard reset
4	Ground
5	+ 5 Vdc

D) Keylock Connector (JP3)

The keylock connector is a 2-pin, Berg strip. When this connector (JP3) is open, the keyboard is locked. When this connector (JP3) is shorted, the keyboard is unlocked.

E) Reset Connector (JP4)

The reset connector is a 2-pin, keyed, Berg strip. When this connector (JP4) is open, the system is in regular operation. When this connector (JP4) is shorted for a while, the system restarts.

F) Power LED and Turbo LED Connector (JP5)

The power LED and LED connector is a 4-pin Berg strip. Its pin assignments are as following:

Pin	Assignments
1	+ TURBO LED
2	– TURBO LED
3	Power LED
4	Ground

Pin 1 and , pin 2 to Turbo LED. Pin 3 and pin 4 to power LED.

3-2 THE SYSTEM BOARD SWITCH SETTING

The DIP Switch (SW1) is used to set the system configuration and specify the amount of memory installed on the system board.

Position	Function
1	Normal operation off
2	Use for 8087-2 co-processor
3-4	Not use
5-6	Type of display adapter
7-8	Number of 5¼ inch diskette drives

Switch (SW1)

1 = OFF	(NORMAL OPERATION)
2 = ON	W/O 8087-2 co-processor
2 = OFF	W/ 8087-2 co-processor

Display Adapter Switch Settings:

5 = ON	6 = ON	ENHANCED GRAPHICS ADAPTER
5 = OFF	6 = ON	COLOR/GRAPHICS (40x20 Mode)
5 = ON	6 = OFF	COLOR/GRAPHICS (80x25 Mode)
5 = OFF	6 = OFF	MONOCHROME DISPLAY ADAPTER OR BOTH

Display Dirve Switch Setting:

7 = ON	8 = ON	1 DRIVE INSTALLED
7 = OFF	8 = ON	2 DRIVES INSTALLED
7 = ON	8 = OFF	3 DRIVES INSTALLED
7 = OFF	8 = OFF	4 DRIVES INSTALLED

CHAPTER 4
MEMORY RAM CHIP INSTALLATION

4-1 RAM Chip Installation

The 10MHz Turbo mainboard provides 4 banks of memory.

BANK 0 is made up of 9 pieces of 41256 in U90 through U57.

BANK 1 is made up of 9 pieces of 41256 in U89 through U56.

BANK 2 is made up of 2 pieces of 4464 in U63, U59 and 1 piece of 4164 in U55.

BANK 3 is made up of 2 pieces of 4464 in U72, U67 and 1 piece of 4164 in U76.

- 4164 in BANK 2 and BANK 3 is used for parity checking.

4 portions of memory configuration can be installed on board. Follow the instructions below for proper installation.

Option	RAM chips on Bank 0	RAM chips on Bank 1	RAM chips on Bank 2	RAM chips on Bank 3
256K RAM	41256 x9	No chip	No chip	No chip
512k RAM	41256x9	41256x9	No chip	No chip
576K RAM	41256x9	41256x9	4464x2 +4164x1	No chip
640K RAM	41256x9	41256x9	4464x2 +4164x1	4464x2 +4164x1

4-2 INSTALLATION OF ROM CHIPS

The 10MHz Turbo Mainboard provides space for system.

U38 must be installed 2764 for ROM BIOS.
U49 must be installed 27256 for ROM BASIC.

HARDWARE RESET
KEYBOARD CONNECTOR
DIP SW
POWER CONNECTOR
KEY LOCK
LED INDICATOR
TURBO SW
BANK 3
BANK 2
EXPENSION BIOS ROM
SPEAKER