Setting CSV parameters

TRAVEO™ T2G family

About this document

Scope and purpose

The Clock Supervision (CSV) feature in TRAVEO™ T2G family enables you to check the frequency of the monitored clock to ensure that it is within the allowed frequency window. To understand the functionality described and terminology used in this guide, see the “Clocking System” chapter in the **architecture technical reference manual (TRM)**.

This guide describes how to calculate and set the CSV parameters using the CSV calculator.

Intended audience

This document is intended for anyone using the TRAVEO™ T2G family to determine the CSV parameters.

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1 Overview

Figure 1 shows the signal example of the CSV.

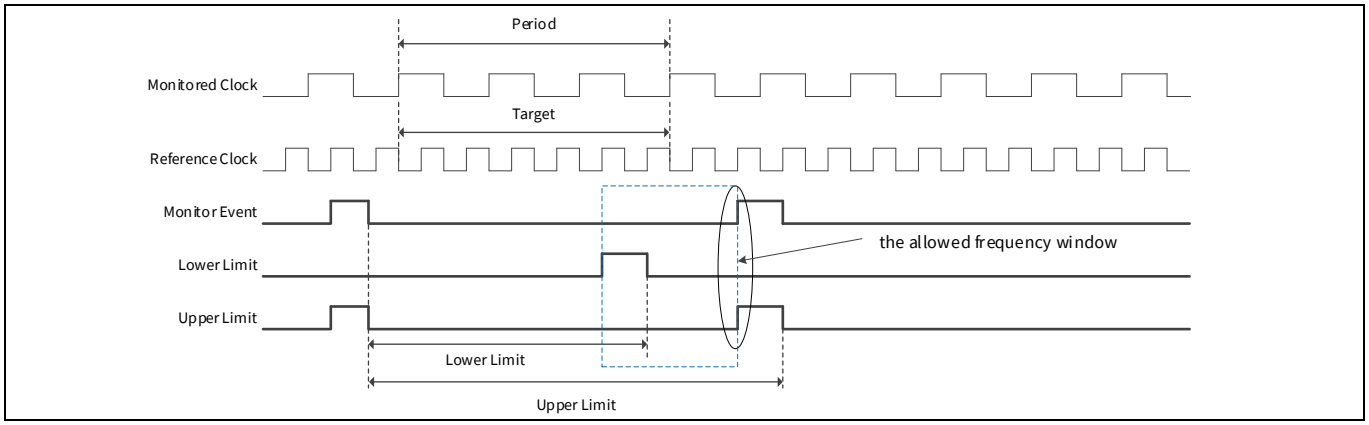

Figure 1 CSV operation signal example

The basic operation principle of the CSV circuit is as follows:

- Period is the monitored clock count while 'Target' is the reference clock count. In an ideal case, these two are the same.
- The monitored clock generates a Monitor event (Period), and the reference clock generates Lower and Upper limits.
- The Monitor event is compared against the Lower and Upper limits.
- An error is reported if the Monitor event ≤ Lower limit, or Monitor event > Upper limit.

2 Parameters related to CSV

Check the parameters related to CSV by the following steps.

2.1 Check the clock specifications

Check the following clock specifications:

- Reference clock frequency and tolerance (integer %)
- Monitored clock frequency and required tolerance (integer %)
  The required monitored clock tolerance should be equal to or larger than the reference clock tolerance.
  - In case of the monitored clock is FLL, PLL200 or PLL400
    - Set the nominal frequency (Fc) of configured VCO or PLL400 output for fractional mode or SSCG in down spread mode to the monitor clock frequency. See the “Root and intermediate clocks” table in the **TRAVEO™ T2G cluster device datasheet** or SID341/SID341A(4)/SID341B(4)/SID351 in the **TRAVEO™ T2G body device datasheet** for the maximum frequency.

Note: The maximum frequency is reduced in PLL400 with SSCG/fractional mode.

  - In case of the monitored clock is PLL200 or PLL400 without SSCG/fractional mode
    - Set ‘3 or more’ in the consideration of the PLL jitter to the monitored clock tolerance.
  - In case of the monitored clock is PLL400 with SSCG/fractional mode
    - Set ‘5 or more’ in the consideration of the PLL jitter shown in **Figure 2** to the monitored clock tolerance.
  - In case of the monitored clock is PLL400 with SSCG mode
    - Set the modulation depth corresponding to your configuration.

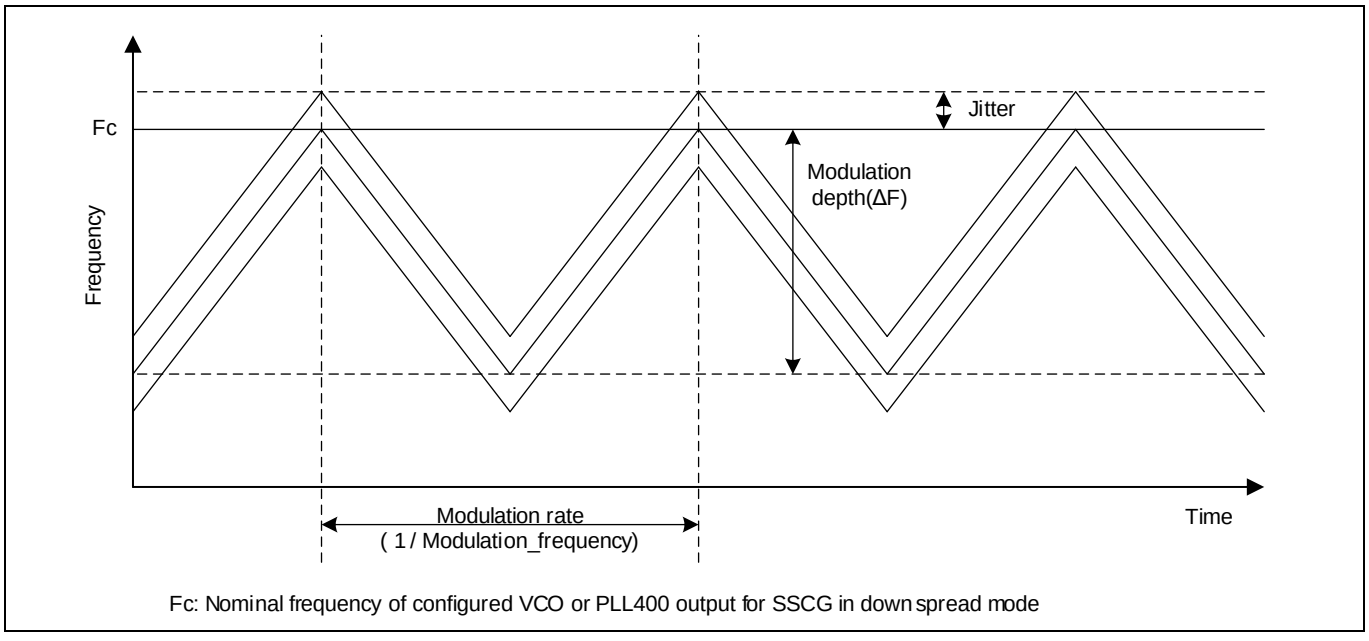

Figure 2 PLL clock frequency tolerance

- Maximum startup time for the monitored clock except for WCO.
  In the case of WCO, the startup time is unused (0). CSV should be enabled after WCO is started (BACKUP_STATUS.WCO_OK = 1).

Enter the above values in the cells, highlighted in orange, of the CSV calculator. If the monitored clock tolerance is smaller than reference clock tolerance, the 'Value' cell of monitored clock tolerance will be highlighted in red.

Table 1 Clock specification parameters

Parameters	Value	Unit	Remarks
Reference clock frequency	8000000	Hz	Nominal source clock frequency ILO: 32768 (SID320) IMO: 8000000 (SID310)
Reference clock tolerance	1	%	ILO: SID320 IMO: SID310
Monitored clock frequency	50000000	Hz	Nominal frequency, see "Root and Intermediate Clocks " table in TRAVEO™ T2G cluster device datasheet or SID341/SID341A(4)/SID341B(4)/SID351 in the TRAVEO™ T2G body device datasheet
Monitored clock tolerance	3	%	≥ Reference clock tolerance (SID310/SID320) Minimum: 3 (When the monitored clock is PLL200/400 without SSCG/fractional mode) Minimum: 5 (When the monitored clock is PLL400 with SSCG/fractional mode)
Monitored clock tolerance (Modulation depth)	0	%	Maximum: 3 (only for PLL400 with SSCG mode) 0 (others)
Maximum startup time for monitored clock	35	μ s	ILO: 12 (SID321) IMO: 7.5 (SID311) PLL200: 35 (SID340) PLL400: 50 (SID340A) FLL: 5 (SID350) WCO: 0 (Unused)

2.2 Determine the target

Check the minimum Target with **Equation 1** using the CSV calculator.

For example, for a tolerance of one percent, the Target must be at least 200. Increasing the Target increases the CSV accuracy; it also increases the latency.

Equation 1

$$Min\ Target = \frac{200}{Reference\ clock\ tolerance}$$

Determine and enter the Target highlighted in orange of the CSV calculator referring the calculated minimum Target. The Target should be equal to or greater than the minimum Target. If the Target is smaller than the minimum Target, the 'Value' cell of the Target will be highlighted in red.

Table 2 Target parameters

Parameters	Value	Unit	Remarks
Minimum Target (Calculated reference clock count)	200	Cycles	
Target (Reference clock count for user definition)	200	Cycles	≥ Minimum Target

2.3 Calculate the lower and upper limit

Calculate the Lower limit with **Equation 2** using the CSV calculator.

Equation 2

$$Lower\ limit = Period \times \frac{\text{Reference clock frequency} \times \left(1 - \frac{Reference\ clock\ tolerance}{100}\right)}{\text{Monitored clock frequency} \times \left(1 + \frac{Monitored\ clock\ tolerance}{100}\right)}$$

Calculate the Upper limit with **Equation 3** using the CSV calculator.

Equation 3

$$Upper\ limit = Period \times \frac{\text{Reference clock frequency} \times \left(1 + \frac{Reference\ clock\ tolerance}{100}\right)}{\text{Monitored clock frequency} \times \left(1 - \frac{Monitored\ clock\ tolerance}{100}\right)}$$

Only for PLL400 SSCG mode:

$$Upper\ limit = Period \times \frac{\text{Reference clock frequency} \times \left(1 + \frac{Reference\ clock\ tolerance}{100}\right)}{\text{Monitored clock frequency} \times \left(1 - \frac{Monitored\ clock\ tolerance + Modulation\ depth}{100}\right)}$$

2.4 Calculate the period

Calculate the Period with **Equation 4** using the CSV calculator. If the Period value is less than one, increase the Target value. To avoid the round off error of the Period value, the value should be as close to an integral value as possible and not a decimal value. This can be achieved by adjusting Target value.

Equation 4

$$Period = \text{Target} \times \frac{Monitored\ clock\ frequency}{Reference\ clock\ frequency}$$

2.5 Calculate the startup delay

Calculate the Startup Delay with **Equation 5** using the CSV calculator. In the case of WCO, the startup time is unused (0). CSV should be enabled after WCO is started (BACKUP_STATUS.WCO_OK = 1).

Equation 5

$$Startup\ Delay = Maximum\ startup\ time\ for\ monitored\ clock \times \text{Reference clock frequency} \times \left(1 + \frac{Reference\ clock\ tolerance}{100}\right)$$

2.6 Check the values for CSV register settings

You should set the values obtained by subtracting 1 from the above calculated values in the CSV register. The CSV calculator calculates these CSV register values based on the above parameters and automatically displays the values in cells highlighted in green. If the Value is larger than 65535, the cell will be highlighted in red.

When determining the final CSV parameters, evaluate the CSV function sufficiently in the user system environment.

Table 3 Parameters for CSV registers

Parameters	Value	Unit	Remarks
Upper limit value for UPPER register	204	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Lower limit value for LOWER register	195	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Period value for PERIOD register	1249	Cycles	Minimum: 0 Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Startup delay value for STARTUP register	282	Cycles	Maximum: 255 (Only for CSV_ILO/LF in the TRAVEO™ T2G body devices) Maximum: 511 (Only for CSV_ILO/LF/BAK in the TRAVEO™ T2G cluster devices) Maximum: 65535 (Others)

3 CSV calculator example

3.1 PLL200 example

This section shows the CSV calculator example of PLL200 with the following parameters:

- Reference clock frequency: 8 MHz (ECO)
- Reference clock tolerance: 1 % (ECO)
- Target: 200 (use the same value as the calculated minimum Target)
- Monitored clock frequency: 50 MHz (CSV_HF0/PLL200)
- Monitored clock tolerance: 3 % (CSV_HF0/PLL200)
- Monitored clock tolerance (Modulation depth): 0% (CSV_HF0/PLL200)
- Startup time for Monitored clock: 35 μs (PLL200)

Enter the above parameters in the cells, highlighted in orange, of the CSV calculator.

Table 4 Input parameters

Parameters	Value	Unit	Remarks
Reference clock frequency	8000000	Hz	Nominal source clock frequency ILO: 32768 (SID320) IMO: 8000000 (SID310)
Reference clock tolerance	1	%	ILO: SID320 IMO: SID310
Minimum Target (Calculated reference clock count)	200	Cycles	
Target (Reference clock count for user definition)	200	Cycles	≥ Minimum Target
Monitored clock frequency	50000000	Hz	Nominal frequency, see "Root and Intermediate Clocks " table in the TRAVEO™ T2G cluster device datasheet or SID341/SID341A(4)/SID341B(4) /SID351 in the TRAVEO™ T2G body device datasheet.
Monitored clock tolerance	3	%	≥ Reference clock tolerance (SID310/SID320) Minimum: 3 (When the monitored clock is PLL200/400 without SSCG/fractional mode) Minimum: 5 (When the monitored clock is PLL400 with SSCG/fractional mode)
Monitored clock tolerance (Modulation depth)	0	%	Maximum: 3 (only for PLL400 with SSCG mode) 0 (others)

Parameters	Value	Unit	Remarks
Maximum startup time for monitored clock	35	µs	ILO: 12 (SID321) IMO: 7.5 (SID311) PLL200: 35 (SID340) PLL400: 50 (SID340A) FLL: 5 (SID350) WCO: 0 (Unused)

The CSV Calculator calculates the CSV register values based on the entered parameters and automatically displays the values in cells highlighted in green.

Table 5 Output parameters

Parameters	Value	Unit	Remarks
Upper limit value for UPPER register	208	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Lower limit value for LOWER register	191	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Period value for PERIOD register	1249	Cycles	Minimum: 0 Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Startup delay value for STARTUP register	282	Cycles	Maximum: 255 (Only for CSV_ILO/LF in the TRAVEO™ T2G body devices) Maximum: 511 (Only for CSV_ILO/LF/BAK in the TRAVEO™ T2G cluster devices) Maximum: 65535 (Others)

3.2 PLL400 example

This section shows the CSV calculator example of PLL400 with the following parameters:

- Reference clock frequency: 8 MHz (ECO)
- Reference clock tolerance: 1 % (ECO)
- Target: 400 (use the twice value of the calculated minimum Target)
- Monitored clock frequency: 200 MHz (CSV_HF1/PLL400 with SSCG)
- Monitored clock tolerance: 5 % (CSV_HF1/PLL400 with SSCG)
- Monitored clock tolerance (Modulation depth): 3 %
- Startup time for Monitored clock: 50 μs (PLL400)

Enter the above parameters in the cells, highlighted in orange, of the CSV calculator.

Table 6 Input parameters

Parameters	Value	Unit	Remarks
Reference clock frequency	8000000	Hz	Nominal source clock frequency ILO: 32768 (SID320) IMO: 8000000 (SID310)

Parameters	Value	Unit	Remarks
Reference clock tolerance	1	%	ILO: SID320 IMO: SID310
Minimum Target (Calculated reference clock count)	200	Cycles	
Target (Reference clock count for user definition)	400	Cycles	≥ Minimum Target
Monitored clock frequency	200000000	Hz	Nominal frequency, see "Root and Intermediate Clocks " table in the TRAVEO™ T2G cluster device datasheet or SID341/SID341A(4)/SID341B(4)/SID351 in the TRAVEO™ T2G body device datasheet.
Monitored clock tolerance	5	%	≥ Reference clock tolerance (SID310/SID320) Minimum: 3 (When the monitored clock is PLL200/400 without SSCG/fractional mode) Minimum: 5 (When the monitored clock is PLL400 with SSCG/fractional mode)
Monitored clock tolerance (Modulation depth)	3	%	Maximum: 3 (only for PLL400 SSCG mode) 0 (others)
Maximum startup time for monitored clock	50	µs	ILO: 12 (SID321) IMO: 7.5 (SID311) PLL200: 35 (SID340) PLL400: 50 (SID340A) FLL: 5 (SID350) WCO: 0 (Unused)

The CSV calculator calculates the CSV register values based on the entered parameters and automatically displays the values in cells highlighted in green.

Table 7 Output parameters

Parameters	Value	Unit	Remarks
Upper limit value for UPPER register	439	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Lower limit value for LOWER register	376	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Period value for PERIOD register	9999	Cycles	Minimum: 0 Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)

Parameters	Value	Unit	Remarks
Startup delay value for STARTUP register	403	Cycles	Maximum: 255 (Only for CSV_ILO/LF in the TRAVEO™ T2G body devices) Maximum: 511 (Only for CSV_ILO/LF/BAK in the TRAVEO™ T2G cluster devices) Maximum: 65535 (Others)

3.3 FLL example

This section shows the CSV calculator example of FLL with the following parameters:

- Reference clock frequency: 8 MHz (IMO)
- Reference clock tolerance: 4 % (IMO)
- Target: 50 (use the same value as the calculated minimum Target)
- Monitored clock frequency: 100 MHz (CSV_HF0/FLL)
- Monitored clock tolerance: 5 % (Reference clock tolerance + SID352)
- Monitored clock tolerance (Modulation depth): 0 % (CSV_HF0/FLL)
- Startup time for Monitored clock: 5 μs (FLL)

Enter the above parameters in the cells, highlighted in orange, of the CSV calculator.

Table 8 Input parameters

Parameters	Value	Unit	Remarks
Reference clock frequency	8000000	Hz	Nominal source clock frequency ILO: 32768 (SID320) IMO: 8000000 (SID310)
Reference clock tolerance	4	%	ILO: SID320 IMO: SID310
Minimum Target (Calculated reference clock count)	50	Cycles	
Target (Reference clock count for user definition)	50	Cycles	≥ Minimum Target
Monitored clock frequency	100000000	Hz	Nominal frequency, see "Root and Intermediate Clocks " table in the TRAVEO™ T2G cluster device datasheet or SID341/SID341A(4)/SID341B(4)/SID351 in the TRAVEO™ T2G body device datasheet.
Monitored clock tolerance	4	%	≥ Reference clock tolerance (SID310/SID320) Minimum: 3 (When the monitored clock is PLL200/400 without SSCG/fractional mode)

Parameters	Value	Unit	Remarks
			Minimum: 5 (When the monitored clock is PLL400 with SSCG/fractional mode)
Monitored clock tolerance (Modulation depth)	0	%	Maximum: 3 (only for PLL400 SSCG mode) 0 (others)
Maximum startup time for monitored clock	5	µs	ILO: 12 (SID321) IMO: 7.5 (SID311) PLL200: 35 (SID340) PLL400: 50 (SID340A) FLL: 5 (SID350) WCO: 0 (Unused)

The CSV calculator calculates the CSV register values based on the entered parameters and automatically displays the values in cells highlighted in green.

Table 9 Output parameters

Parameters	Value	Unit	Remarks
Upper limit value for UPPER register	54	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Lower limit value for LOWER register	45	Cycles	Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Period value for PERIOD register	624	Cycles	Minimum: 0 Maximum: 255 (Only for CSV_ILO/LF/BAK) Maximum: 65535 (Others)
Startup delay value for STARTUP register	41	Cycles	Maximum: 255 (Only for CSV_ILO/LF in the TRAVEO™ T2G body devices) Maximum: 511 (Only for CSV_ILO/LF/BAK in the TRAVEO™ T2G cluster devices) Maximum: 65535 (Others)

References

The following are the TRAVEO™ T2G family series datasheets and technical reference manuals. Contact **Technical Support** to obtain these documents.

[1] Device datasheets

- **CYT2B6 datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family**
- **CYT2B7 datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family**
- **CYT2B9 datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family**
- **CYT4BF datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family**
- **CYT3BB/4BB datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family**
- CYT4DN datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family (Doc No. 002-24601)
- CYT3DL datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family (Doc No. 002-27763)
- CYT2CL datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family (Doc No. 002-32508)

[2] Body controller entry family TRMs

- **TRAVEO™ T2G automotive body controller entry family architecture technical reference manual (TRM)**
- **TRAVEO™ T2G automotive body controller entry registers technical reference manual (TRM) for CYT2B7**
- **TRAVEO™ T2G automotive body controller entry registers technical reference manual (TRM) for CYT2B9**

[3] Body controller high family TRMs

- **TRAVEO™ T2G automotive body controller high family architecture technical reference manual (TRM)**
- **TRAVEO™ T2G automotive body controller high registers technical reference manual (TRM) for CYT4BF**
- **TRAVEO™ T2G automotive body controller high registers technical reference manual (TRM) for CYT3BB/4BB**

[4] Cluster 2D family TRMs

- TRAVEO™ T2G automotive cluster 2D family architecture technical reference manual (TRM) (Doc No. 002-25800)
- TRAVEO™ T2G automotive cluster 2D registers technical reference manual (TRM) for CYT4DN (Doc No. 002-25923)
- TRAVEO™ T2G automotive cluster 2D registers technical reference manual (TRM) for CYT3DL (Doc No. 002-29854)

[5] Cluster entry family TRMs

- TRAVEO™ T2G automotive cluster entry family architecture technical reference manual (TRM) (Doc No. 002-33175)
- TRAVEO™ T2G automotive cluster entry registers technical reference manual (TRM) for CYT4DN (Doc No. 002-33404)

Revision history

Revision	Issue date	Description of change
**	2021-02-10	Initial release
*A	2021-04-22	Updated the description in 2.4 and the remarks in Table 3 and Table 5.
*B	2021-11-04	Added the description of monitored clock frequency tolerance and modulation depth parameter and PLL400/FLL example. Added the **References** section.

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