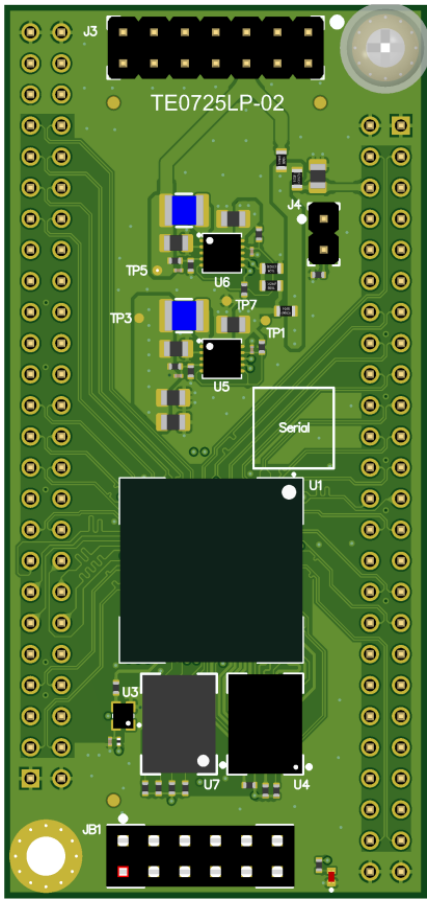

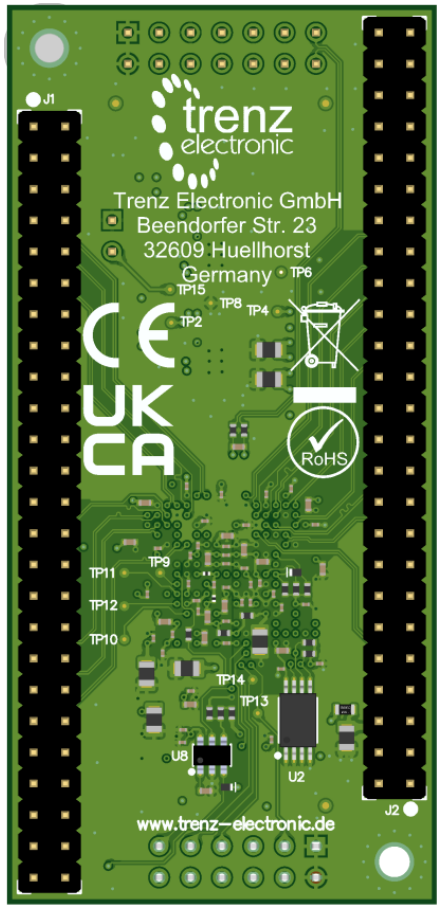

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Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: Legal Notices Modules		
	A4	Number: TE0725LP 72C-AU	Rev. 04
	Date: 2023-07-14	Copyright: Trenz Electronic GmbH	Page 1 of 12
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02	1. L1 , L2 , L6 ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000. 2. Added J4 and R30 (JTAG only Enable). 3. Added Diode D1 for INIT reset. 4. Added Diode D3 for U8 input protection. 5. Added a pull-up resistor R29 on U7B RESET, pin A4. 6. Added a pull-up resistor R31 on SPI_DQ2, pin C4. 7. Added capacitor C22 to avoid false resetting. 8. Resistors R13 , R72 , R29 , R18 , R20 , R31 , R21 , R3 , R9 value 5.6kOhms changed to 2.2kOhms. 9. Resistor R7 10 kOhms replaced with 2.2 kOhms to optimise the voltage divider values. 10. Resistors R4 , R15 value 2kOhms changed to 330Ohms according to AMD specification (UG470). 11. Added a 2.4 kOhm resistor R32 . 12. Capacitor C21 value 47 uF changed to 100 uF, added additional decoupling capacitors C33 , C34 , C35 according to AMD specification (UG 483). 13. Added C24 to improve noise immunity. 14. AVCC power rail filter is improved. C1 connected to 1.8V. 15. Added pages Legal notices, power diagram. 16. Added System Overview. 17. Added testpoints TP1 - TP15 .	VG (05.08.2024)

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Title: TE0725LP - Changes list		
A4	Number: TE0725LP 72C-AU	Rev. 02
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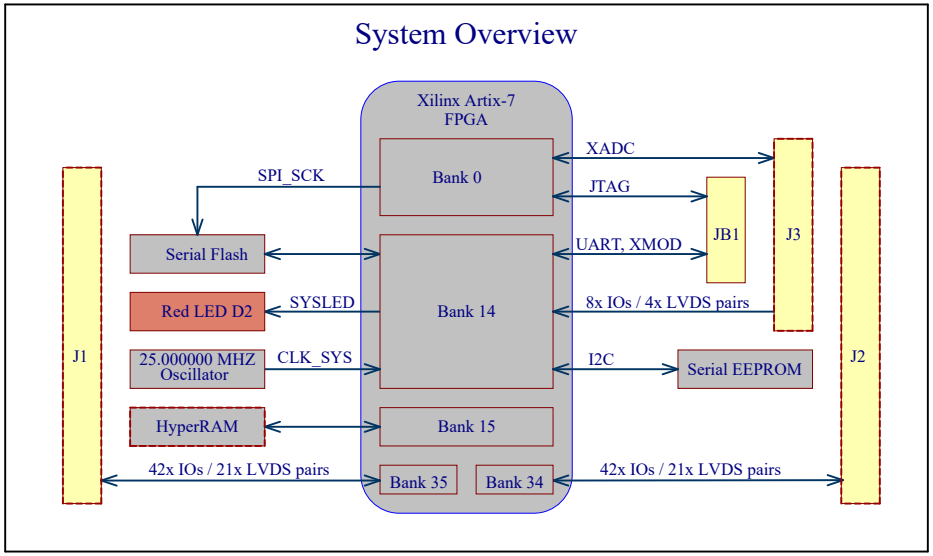
Filename: Revision_Changes.SchDoc		

U_FPGA_PWR_MISC
FPGA_PWR_MISC.SchDoc

Power_Diagram
Power_Diagram.SchDoc

U_PowerSupply
POWER.SchDoc



GND
Mount.Hole 3.2mm

PM1 PM2
PM4 PM5
PM6 PM3

Serial
Serial
Serialnumber 6,3 x 6.3mm

RoHS1
RoHS Logo on Top Overlay
RoHS-TOPOVERLAY

UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY

MECH1
TE Address Overlay
LOGO ADDRESS

LOGO1
TE Logo PRINT Layer
LOGO PRINT

CE
CE Logo on Top Overlay
CE-TOPOVERLAY

Drawn by	VG
Checked by	MT
Assembly variant	72C-AU
Created by	
Modified by	
Modified at	

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Title:	TE0725LP - Overview		
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Date: 2023-07-14	Copyright: Trenz Electronic GmbH		Page3 of 12
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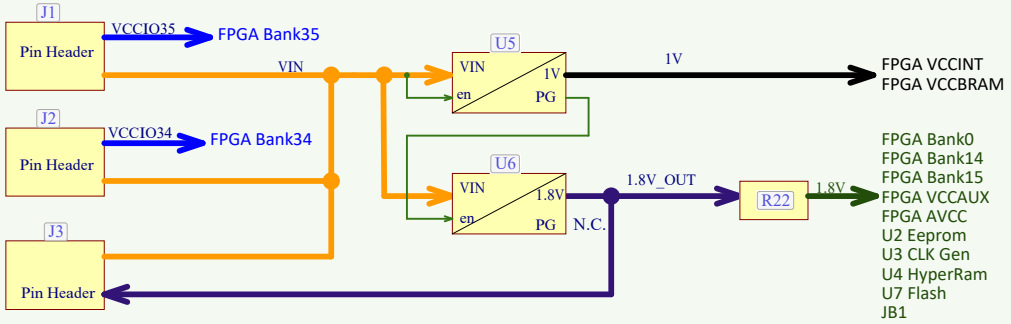
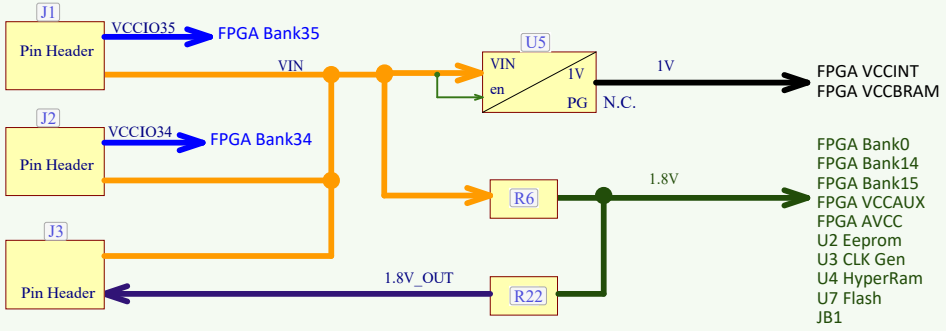
Power-on sequencing: VIN = 3.3V



Depends on assembly option

Power-on sequencing: VIN = 1.8V

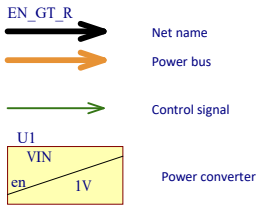


Depends on assembly option

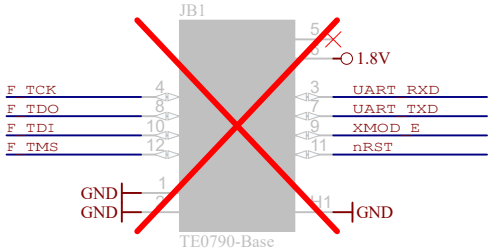
Supported Voltage Ranges:

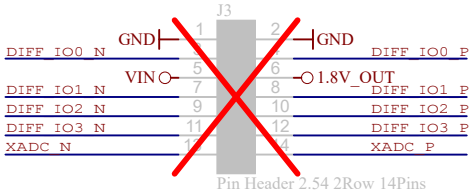
Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3V / 1.8V	+/-3%	Micromodule Power	J1, J2, J3
1.8V_OUT	OUT	1.8V	+/-3%	Power supply for external use	J3
VCCIO35	IN	1.8V ... 3.3V	+/-3%	Power of Bank 35	J1
VCCIO34	IN	1.8V ... 3.3V	+/-3%	Power of Bank 34	J2

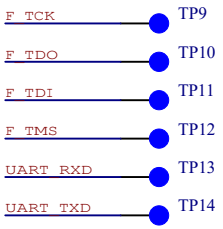
Programmable Logic, supplied by power rail
Low-Power Domain, supplied by power rail

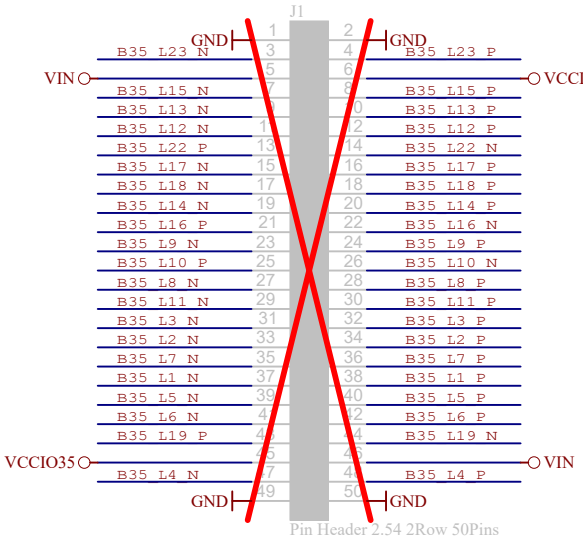


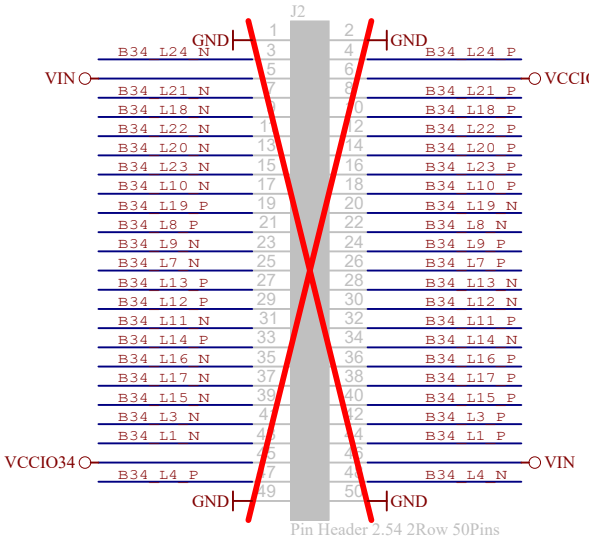
trenz electronic	Title: Power Diagram		
A4	Number: TE0725LP 72C-AU		Rev. 02
Date: 2023-07-14	Copyright: Trenz Electronic GmbH		Page4 of 12
Filename: Power_Diagram.SchDoc			

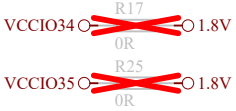












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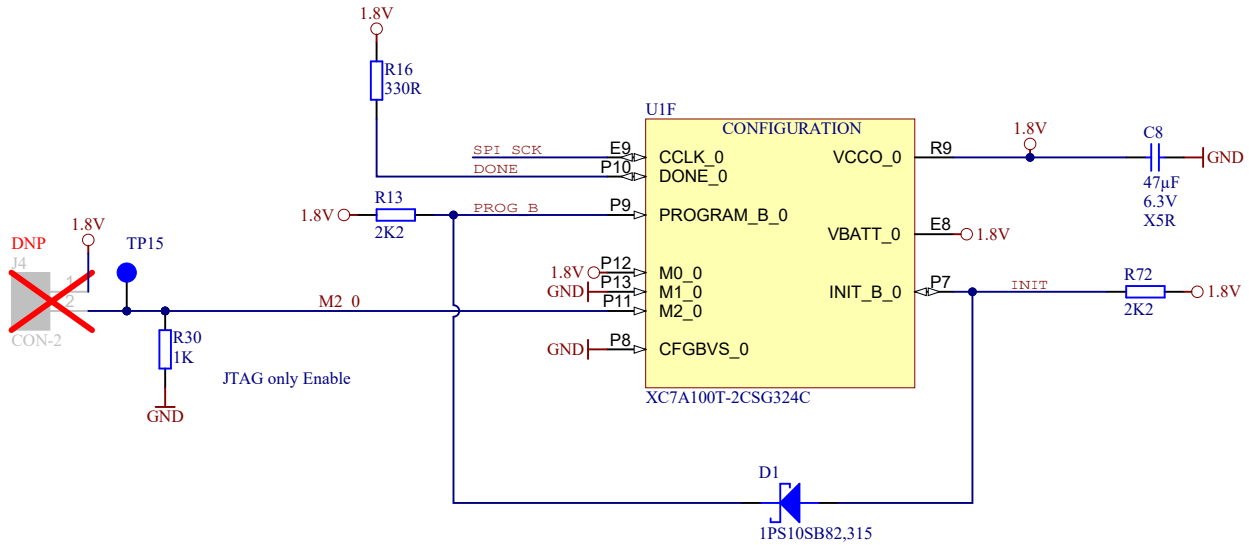
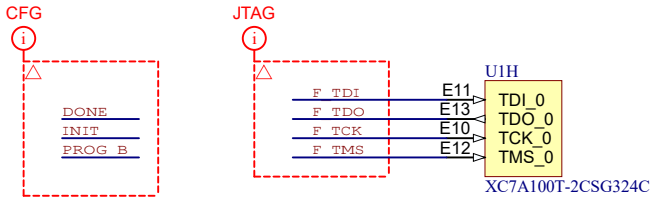
Title: TE0725LP - B2B Connectors			
A4	Number: TE0725LP 72C-AU		Rev. 02
Date: 2023-07-14	Copyright: Trenz Electronic GmbH / TT		Page5 of 12
Filename: B2B_Connector.SchDoc			





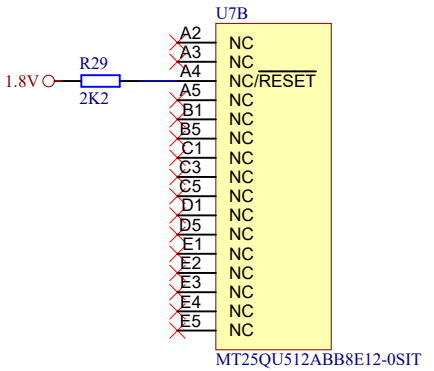
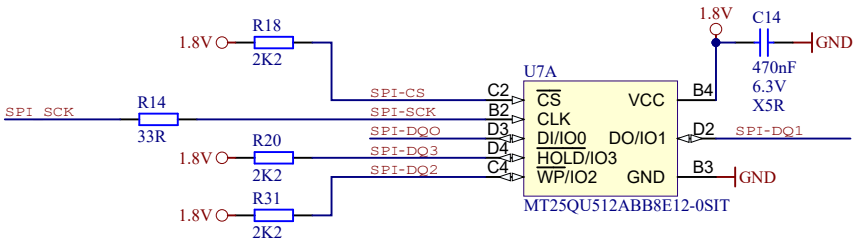
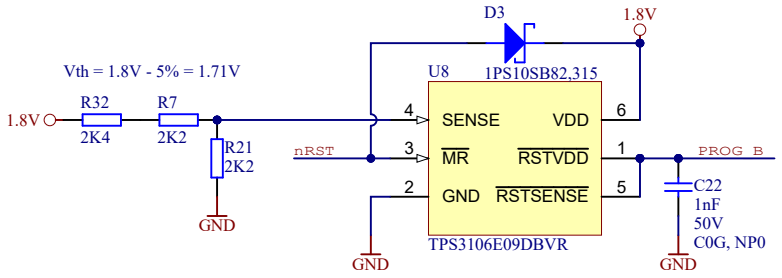


Table 2-1: **7 Series FPGA Configuration Modes (UG470)**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32(1)	Input
Slave Serial(2)	111	x1	Input





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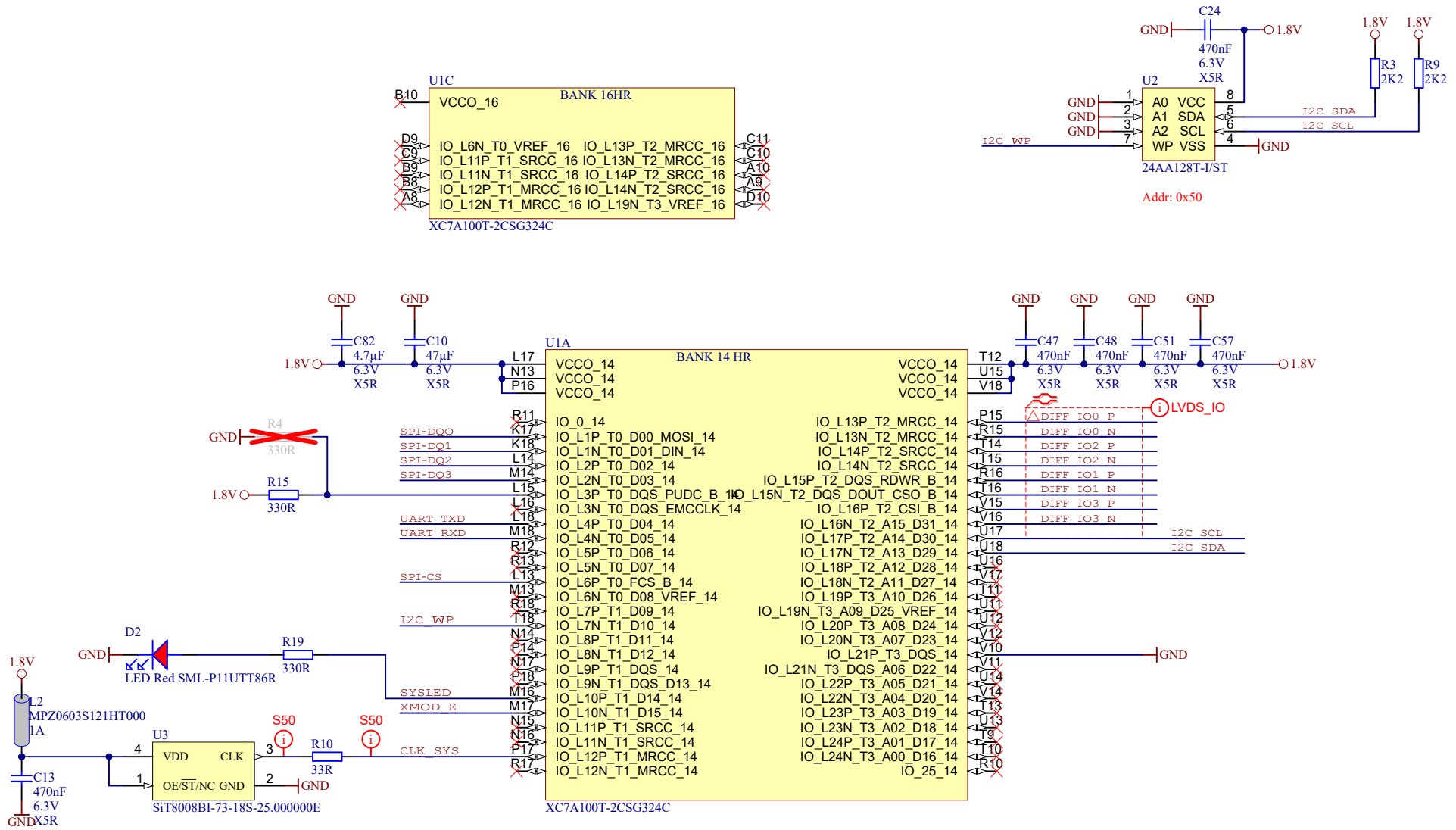
Title: TE0725LP - FPGA CFG		
A4	Number: TE0725LP 72C-AU	Rev. 02
Date: 2023-07-14	Copyright: Trenz Electronic GmbH / TT	Page6 of 12
Filename: FPGA_CFG.SchDoc		



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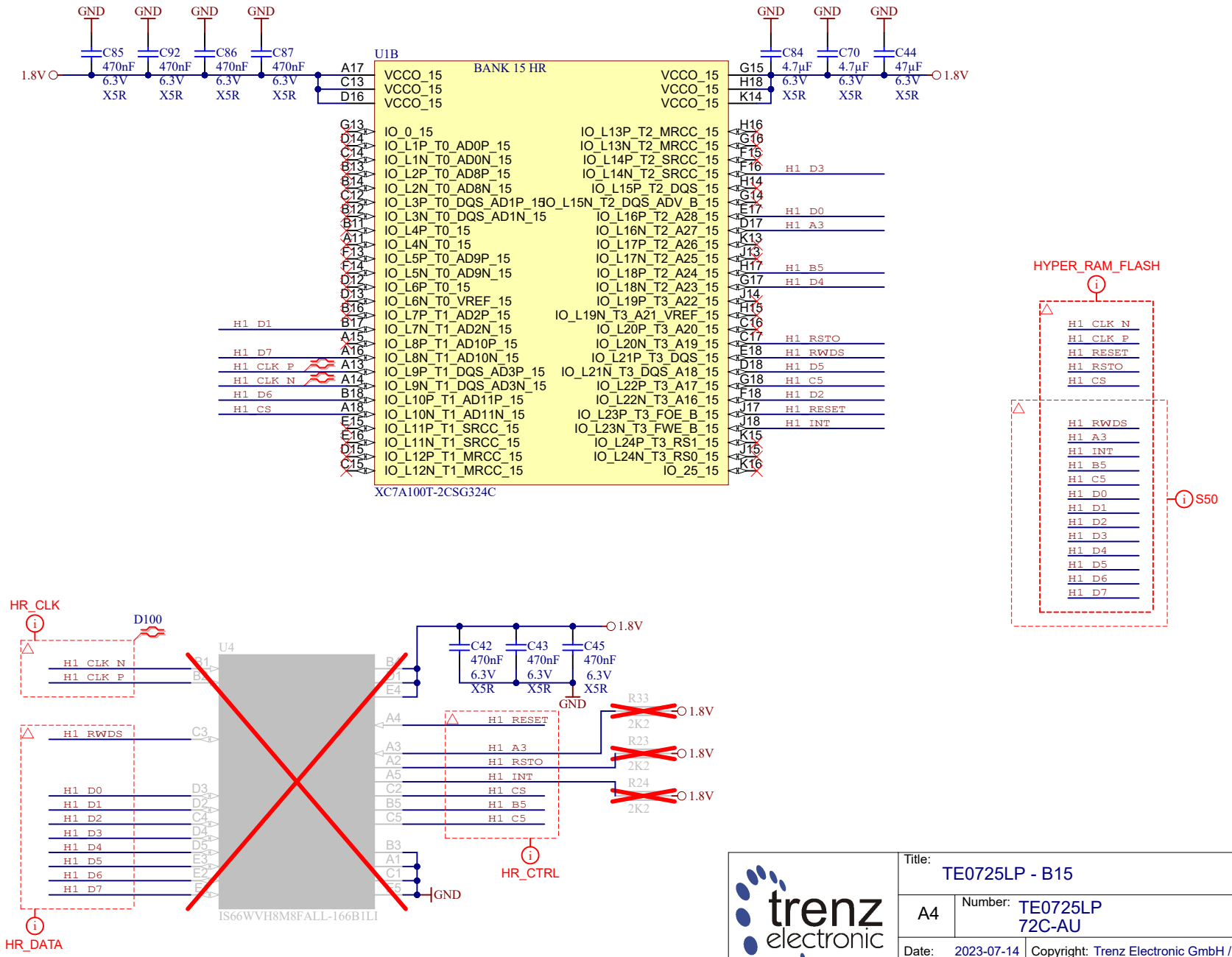
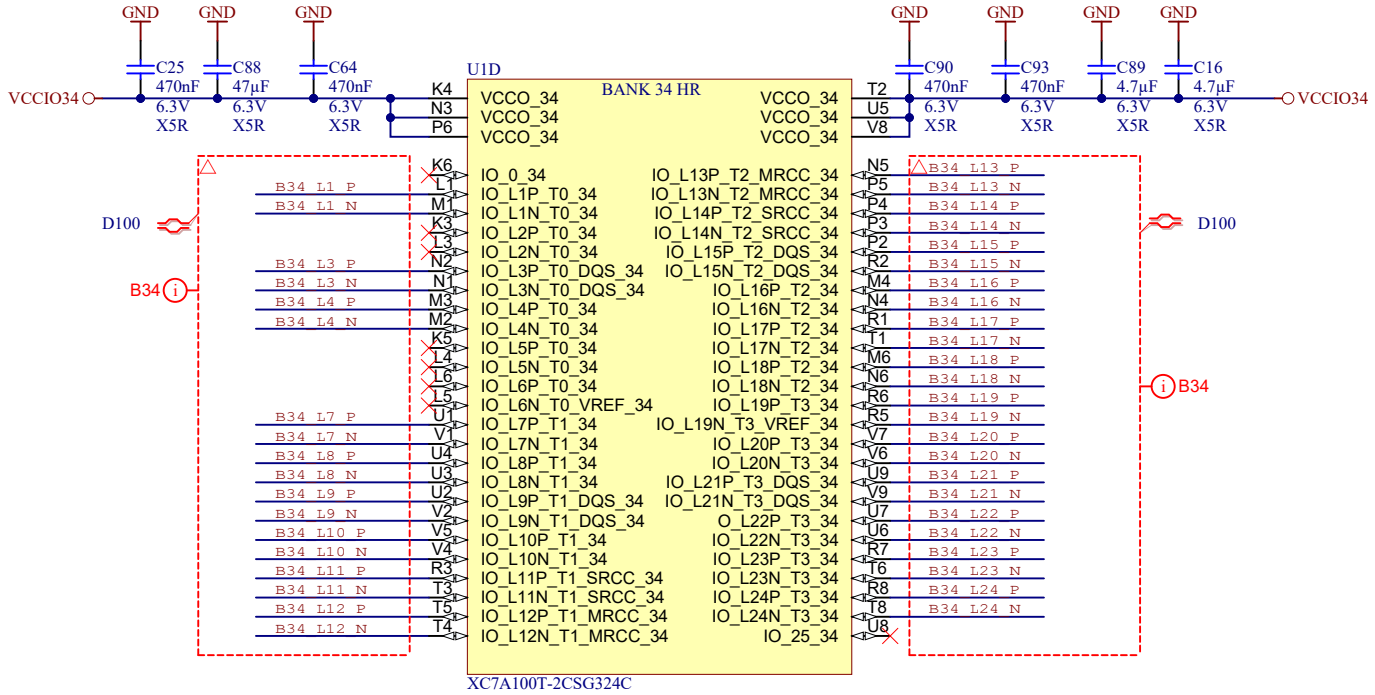
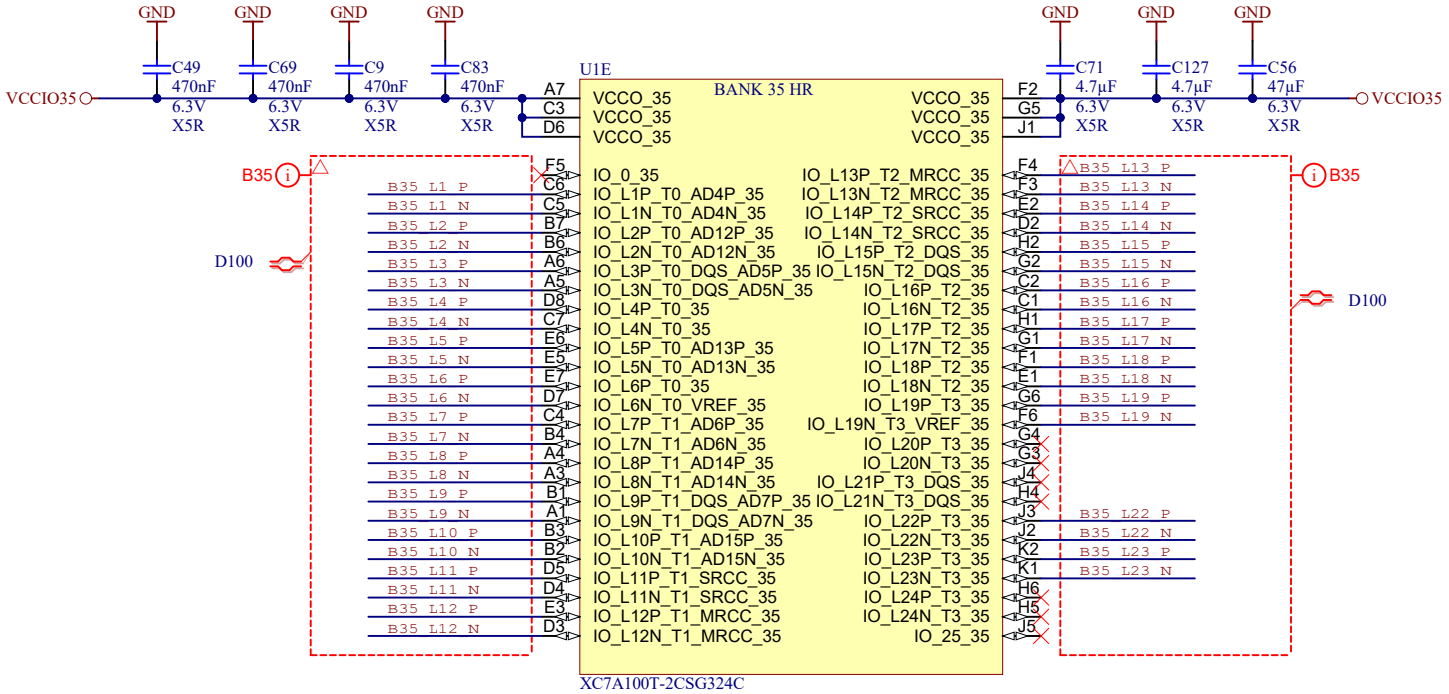
	A4	Number: TE0725LP 72C-AU	Rev. 02
	Date: 2023-07-14	Copyright: Trenz Electronic GmbH / TT	Page7 of 12
	Filename: B14_B16.SchDoc		



Title:	TE0725LP - B15		
A4	Number: TE0725LP 72C-AU		Rev. 02
Date: 2023-07-14	Copyright: Trenz Electronic GmbH / TT		Page8 of 12
Filename:	B15.SchDoc		



trenz electronic	Title: TE0725LP - B34		
	A4	Number: TE0725LP 72C-AU	Rev. 02
	Date: 2023-07-14	Copyright: Trenz Electronic GmbH / TT	Page9 of 12
	Filename: B34.SchDoc		



trenz electronic	Title: TE0725LP - B35		
	A4	Number: TE0725LP 72C-AU	Rev. 02
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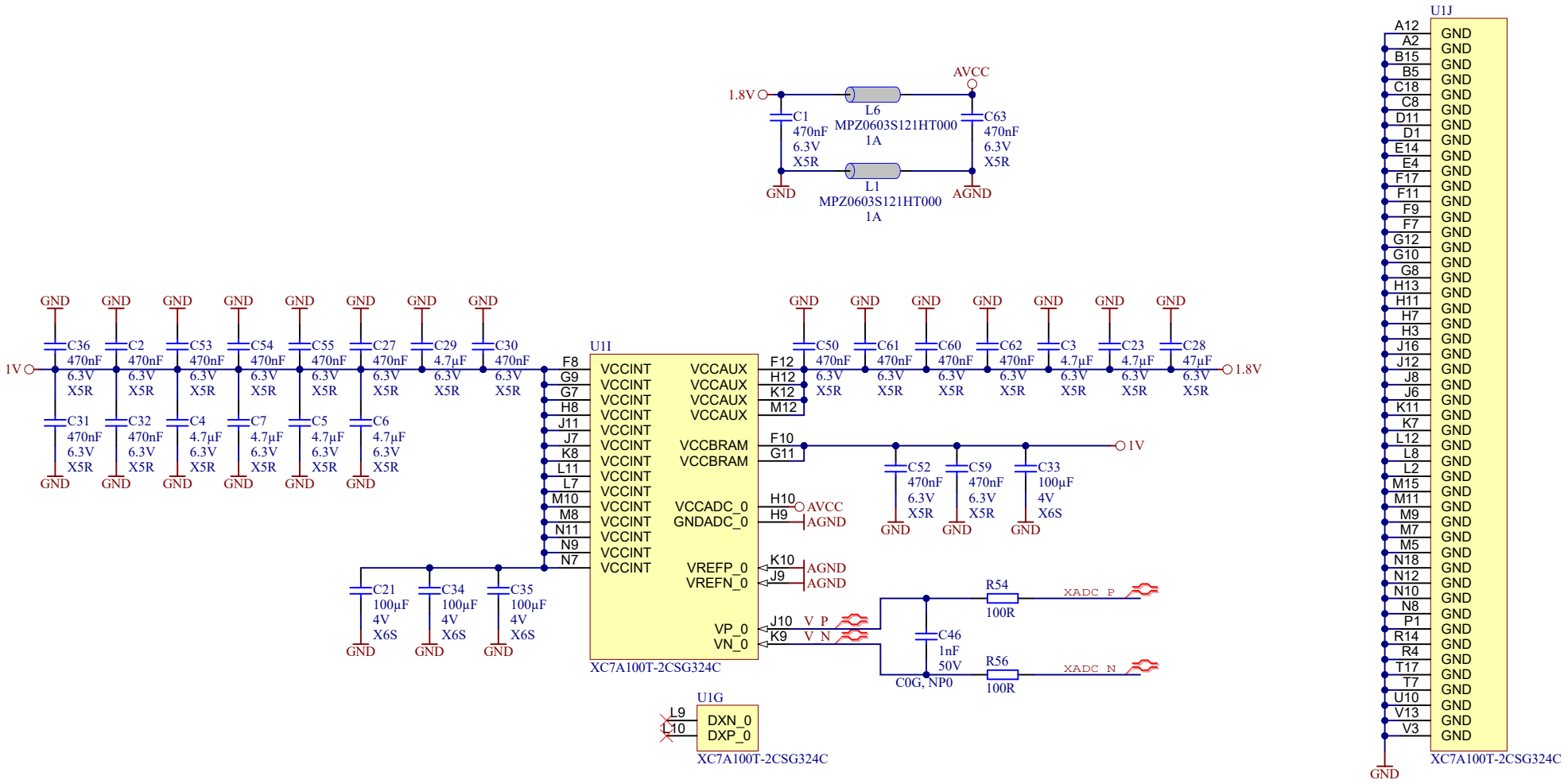
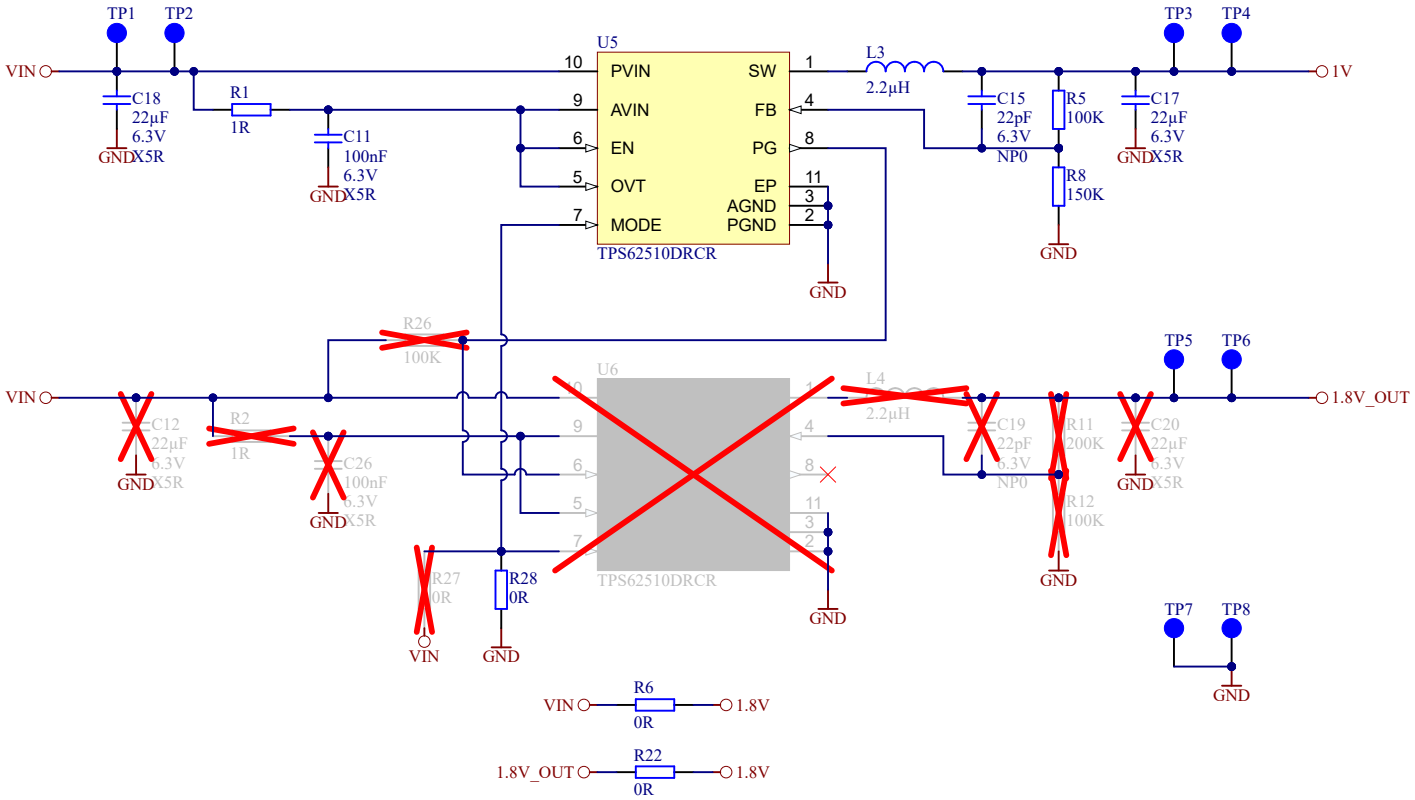
	Filename: B35.SchDoc		



trenz electronic	Title: TE0725LP - FPGA PWR MISC		
	A4	Number: TE0725LP 72C-AU	Rev. 02
	Date: 2023-07-14	Copyright: Trenz Electronic GmbH / TT	Page11 of 12
	Filename: FPGA_PWR_MISC.SchDoc		



Title: TE0725LP - POWER			
A4	Number: TE0725LP 72C-AU		Rev. 02
Date: 2023-07-14	Copyright: Trenz Electronic GmbH		Page 12 of 12
Filename: POWER.SchDoc			