

XMC7000中如何定时完成多组ADC采样

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2025 8 23



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问题背景

- 客户在实际项目中需要用到多路ADC进行定时采样。由于是首次使用XMC7000系列产品，客户对于该产品外设以及开发工具都不熟悉。而现有demo工程中也没有可供参考的例子，所以不知道如何实现该功能。为此，我实现了满足该功能的例程，本文档是对该例程实现进行详细说明。

- 软件开发环境：

- ModusToolbox V3.2.0.16028

- 硬件验证环境：

- KIT XMC72 EVK

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使用的外设资源以及参考资料

– 本例程用到的MCU 外设资源如下:

➤ 四路TCPWM:

- PWM: TCPWM[1] Group[1] Counter0, 定时触发ADC0采样
- PWM1: TCPWM[1] Group[1] Counter1, 定时触发ADC1采样
- PWM2: TCPWM[1] Group[1] Counter2, 定时触发ADC2采样
- PWM_S: TCPWM[0] Group[0] Counter0, 触发另外三路PWM,PWM1,PWM2同步启动
- TCPWM周期: 100us

➤ 三组ADC:

- ADC0的6个channel: P6.0,P6.1,P6.2,P6.3,P6.4,P6.5
- ADC1的6个channel: P12.0,P12.1,P12.2,P12.3,P12.4,P12.5
- ADC2的6个channel: P18.0,P18.1,P18.2,P18.3,P18.4,P18.5

– 例程实现参考官网的以下Appnote:

- [AN234119 - Timer, Counter, and PWM _TCPWM_ usage in XMC7000 family](#)
- [AN234282 - Using a SAR ADC in XMC7000 Family](#)

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ADC0 配置



C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

Name(s)

Persona

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0

SAR

SAR2-1.

☒ 12-bit SAR ADC 1

SAR1

SAR2-1.

☒ 12-bit SAR ADC 2

SAR2

SAR2-1.

☐ epassaref

pass 0 aref 0

▼ Communication

▶ Controller Area Network FD (CAN FD) 0

▶ Controller Area Network FD (CAN FD) 1

☐ Ethernet 0

eth 0

☐ Ethernet 1

eth 1

☐ Inter-IC Sound Bus (I2S) 0

audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1

audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2

audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0

smif 0

☐ SD Host Controller (SDHC) 0

sdhc 0

☐ Serial Communication Block (SCB) 0

scb 0

☐ Serial Communication Block (SCB) 1

scb 1

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name

Value

▼ Overview

Configuration Help

Open SAR2 Documentation

▼ General

Enable SAR Block

☒

Enable The SAR MUX

☒

Enable The SAR ADC

☒

Precondition Time

3

Power Up Time

0

Power Down If Idle

☐

MSB Cycles

Use 1 clock cycles per conversion

Half LSB

☐

Number Of Channels

6

▼ Connections

Clock

24.5 bit Divider 0 clk [SHARED]

Clock Frequency

8.333333 MHz

▼ Channel 0

Channel Name

channel_0

Enabled

☒

HW Trigger

TCPWM

Code Preview

12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

ADC0 channel 0 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0 SAR SAR2-1.

☒ 12-bit SAR ADC 1 SAR1 SAR2-1.

☒ 12-bit SAR ADC 2 SAR2 SAR2-1.

☐ epassaref pass 0 aref 0

▼ Communication

> Controller Area Network FD (CAN FD) 0

> Controller Area Network FD (CAN FD) 1

☐ Ethernet 0 eth 0

☐ Ethernet 1 eth 1

☐ Inter-IC Sound Bus (I2S) 0 audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1 audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2 audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0 smif 0

☐ SD Host Controller (SDHC) 0 sdhc 0

☐ Serial Communication Block (SCB) 0 scb 0

☐ Serial Communication Block (SCB) 1 scb 1

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
▼ Channel 0	
Channel Name	channel_0
Enabled	☒
HW Trigger	TCPWM
Trigger Input	TCPWM[1] Group[1] 16-bit Counter 0 out 0 (PWM) [USED]
Trigger Output	<unassigned>
Trigger Chaner Input	TCPWM[1] Group[1] 16-bit Counter 0 out 1 (PWM) [USED]
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	P6[0] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

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ADC0 channel 0 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	P6[0] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location

Ready

ADC0 channel 1 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0 SAR SAR2-1.

☒ 12-bit SAR ADC 1 SAR1 SAR2-1.

☒ 12-bit SAR ADC 2 SAR2 SAR2-1.

☐ epassaref pass 0 aref 0

▼ Communication

> Controller Area Network FD (CAN FD) 0

> Controller Area Network FD (CAN FD) 1

☐ Ethernet 0 eth 0

☐ Ethernet 1 eth 1

☐ Inter-IC Sound Bus (I2S) 0 audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1 audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2 audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0 smif 0

☐ SD Host Controller (SDHC) 0 sdhc 0

☐ Serial Communication Block (SCB) 0 scb 0

☐ Serial Communication Block (SCB) 1 scb 1

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name

Value

▼ Channel 1

Channel Name channel_1

Enabled ☒

HW Trigger Disabled

Trigger Input <unassigned>

Trigger Output <unassigned>

Trigger Chanel Input <unassigned>

Voltage Range Trigger Output <unassigned>

Channel Done Trigger Output <unassigned>

Debug Freeze Input <unassigned>

Priority 0

Preemption Type Abort ongoing acquisition, do not return

Group End ☐

Output Trigger Type Pulse

Input ☒ P6[1] analog [USED]

Enable External Analog Mux ☐

Precondition Mode Discharge to VREFL

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

只有channel0需要设置HW Trigger为TCPWM，后面5路均不需要再次设置

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ADC0 channel 1 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P6[1] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC0 channel 2 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
Channel 2	
Channel Name	channel_2
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	P6[2] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC0 channel 2 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P6[2] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
-----	-------------	----------

Ready

ADC0 channel 3 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0 SAR SAR2-1.

☒ 12-bit SAR ADC 1 SAR1 SAR2-1.

☒ 12-bit SAR ADC 2 SAR2 SAR2-1.

☐ epassaref pass 0 aref 0

▼ Communication

▶ Controller Area Network FD (CAN FD) 0

▶ Controller Area Network FD (CAN FD) 1

☐ Ethernet 0 eth 0

☐ Ethernet 1 eth 1

☐ Inter-IC Sound Bus (I2S) 0 audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1 audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2 audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0 smif 0

☐ SD Host Controller (SDHC) 0 sdhc 0

☐ Serial Communication Block (SCB) 0 scb 0

☐ Serial Communication Block (SCB) 1 scb 1

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
▼ Channel 3	
Channel Name	channel_3
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	P6[3] analog (CYBSP_QSPI_SCK) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

▼ Fix

Description

Location

Ready

ADC0 channel 3 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P6[3] analog (CYBSP_QSPI_SCK) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

ADC0 channel 4 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0 SAR SAR2-1.

☒ 12-bit SAR ADC 1 SAR1 SAR2-1.

☒ 12-bit SAR ADC 2 SAR2 SAR2-1.

☐ epassaref pass 0 aref 0

▼ Communication

▶ Controller Area Network FD (CAN FD) 0

▶ Controller Area Network FD (CAN FD) 1

☐ Ethernet 0 eth 0

☐ Ethernet 1 eth 1

☐ Inter-IC Sound Bus (I2S) 0 audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1 audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2 audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0 smif 0

☐ SD Host Controller (SDHC) 0 sdhc 0

☐ Serial Communication Block (SCB) 0 scb 0

☐ Serial Communication Block (SCB) 1 scb 1

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
▼ Channel 4	
Channel Name	channel_4
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	P6[4] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

▼ Fix

Description

Location

Ready

ADC0 channel 4 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	P6[4] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location

Ready

ADC0 channel 5 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
Channel 5	
Channel Name	channel_5
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☒
Output Trigger Type	Pulse
Input	P6[5] analog (CYBSP_QSPI_SS, CYBSP_QSPI_FLASH_SSEL) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC0 channel 5 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 0 (SAR) - Parameters

Enter filter text...

Name	Value
Input	P6[5] analog (CYBSP_QSPI_SS, CYBSP_QSPI_FLASH_SSEL) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535
Advanced	
Store Config in Flash	☒

Code Preview 12-bit SAR ADC 0 (SAR) - Parameters

Notice List

0 Errors

0 Warnings

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1 Info

Fix

Description

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ADC1 配置



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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open SAR2 Documentation
General	
Enable SAR Block	☒
Enable The SAR MUX	☒
Enable The SAR ADC	☒
Precondition Time	3
Power Up Time	0
Power Down If Idle	☐
MSB Cycles	Use 1 clock cycles per conversion
Half LSB	☐
Number Of Channels	6
Connections	
Clock	24.5 bit Divider 0 clk [SHARED]
Clock Frequency	8.333333 MHz
Channel 0	
Channel Name	channel_0
Enabled	☒
HW Trigger	TCPWM

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC1 channel 0 配置

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0 SAR SAR2-1.

☒ 12-bit SAR ADC 1 SAR1 SAR2-1.

☒ 12-bit SAR ADC 2 SAR2 SAR2-1.

☐ epassaref pass 0 aref 0

▼ Communication

> Controller Area Network FD (CAN FD) 0

> Controller Area Network FD (CAN FD) 1

☐ Ethernet 0 eth 0

☐ Ethernet 1 eth 1

☐ Inter-IC Sound Bus (I2S) 0 audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1 audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2 audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0 smif 0

☐ SD Host Controller (SDHC) 0 sdhc 0

☐ Serial Communication Block (SCB) 0 scb 0

☐ Serial Communication Block (SCB) 1 scb 1

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name

Value

▼ Channel 0

Channel Name channel_0

Enabled ☒

HW Trigger TCPWM

Trigger Input TCPWM[1] Group[1] 16-bit Counter 1 out 0 (PWM1) [USED]

Trigger Output <unassigned>

Trigger Chaner Input TCPWM[1] Group[1] 16-bit Counter 1 out 1 (PWM1) [USED]

Voltage Range Trigger Output <unassigned>

Channel Done Trigger Output <unassigned>

Debug Freeze Input <unassigned>

Priority 0

Preemption Type Abort ongoing acquisition, do not return

Group End ☐

Output Trigger Type Pulse

Input P12[0] analog (CYBSP_A8) [USED]

Enable External Analog Mux ☐

Precondition Mode Discharge to VREFL

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

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0 Tasks

1 Info

▼ Fix Description

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ADC1 channel 0 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	● P12[0] analog (CYBSP_A8) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

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0 Tasks

1 Info

Fix	Description	Location

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ADC1 channel 1 配置

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XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0

SAR

SAR2-1.

☒ 12-bit SAR ADC 1

SAR1

SAR2-1.

☒ 12-bit SAR ADC 2

SAR2

SAR2-1.

☐ epassaref

pass 0 aref 0

▼ Communication

> Controller Area Network FD (CAN FD) 0

> Controller Area Network FD (CAN FD) 1

☐ Ethernet 0

eth 0

☐ Ethernet 1

eth 1

☐ Inter-IC Sound Bus (I2S) 0

audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1

audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2

audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0

smif 0

☐ SD Host Controller (SDHC) 0

sdhc 0

☐ Serial Communication Block (SCB) 0

scb 0

☐ Serial Communication Block (SCB) 1

scb 1

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name

Value

▼ Channel 1

☐ Channel Name

channel_1

☐ Enabled

☒

☐ HW Trigger

Disabled

☐ Trigger Input

<unassigned>

☐ Trigger Output

<unassigned>

☐ Trigger Chanel Input

<unassigned>

☐ Voltage Range Trigger Output

<unassigned>

☐ Channel Done Trigger Output

<unassigned>

☐ Debug Freeze Input

<unassigned>

☐ Priority

0

☐ Preemption Type

Abort ongoing acquisition, do not return

☐ Group End

☐

☐ Output Trigger Type

Pulse

☐ Input

☒

 P12[1] analog (CYBSP_A9) [USED]

☐ Enable External Analog Mux

☐

☒ Precondition Mode

Discharge to VREFL

Code Preview

12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

☒ 0 Errors

☐ 0 Warnings

☐ 0 Tasks

☐ 1 Info

Fix

Description

Location

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ADC1 channel 1 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	P12[1] analog (CYBSP_A9) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC1 channel 2 配置

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File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Channel 2	
Channel Name	channel_2
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	P12[2] analog (CYBSP_A10) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC1 channel 2 配置

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File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P12[2] analog (CYBSP_A10) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC1 channel 3 配置

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File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog 12-bit SAR ADC 0 SAR SAR2-1. 12-bit SAR ADC 1 SAR1 SAR2-1. 12-bit SAR ADC 2 SAR2 SAR2-1. epassaref pass 0 aref 0 Communication Controller Area Network FD (CAN FD) 0 Controller Area Network FD (CAN FD) 1 Ethernet 0 eth 0 Ethernet 1 eth 1 Inter-IC Sound Bus (I2S) 0 audioss 0 i2s 0 Inter-IC Sound Bus (I2S) 1 audioss 1 i2s 0 Inter-IC Sound Bus (I2S) 2 audioss 2 i2s 0 Quad Serial Memory Interface (QSPI) 0 smif 0 SD Host Controller (SDHC) 0 sdhc 0 Serial Communication Block (SCB) 0 scb 0 Serial Communication Block (SCB) 1 scb 1		

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Channel 3	
Channel Name	channel_3
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	P12[3] analog (CYBSP_A11) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC1 channel 3 配置

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File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P12[3] analog (CYBSP_A11) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC1 channel 4 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Channel 4	
Channel Name	channel_4
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	P12[4] analog (CYBSP_A12) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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ADC1 channel 4 配置

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	P12[4] analog (CYBSP_A12) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location

Ready

ADC1 channel 5 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0

SAR

SAR2-1.

☒ 12-bit SAR ADC 1

SAR1

SAR2-1.

☒ 12-bit SAR ADC 2

SAR2

SAR2-1.

☐ epassaref

pass 0 aref 0

▼ Communication

▶ Controller Area Network FD (CAN FD) 0

▶ Controller Area Network FD (CAN FD) 1

☐ Ethernet 0

eth 0

☐ Ethernet 1

eth 1

☐ Inter-IC Sound Bus (I2S) 0

audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1

audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2

audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0

smif 0

☐ SD Host Controller (SDHC) 0

sdhc 0

☐ Serial Communication Block (SCB) 0

scb 0

☐ Serial Communication Block (SCB) 1

scb 1

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name

Value

▼ Channel 5

Channel Name

channel_5

☒ Enabled

HW Trigger

Disabled

Trigger Input

<unassigned>

Trigger Output

<unassigned>

Trigger Chanel Input

<unassigned>

Voltage Range Trigger Output

<unassigned>

Channel Done Trigger Output

<unassigned>

Debug Freeze Input

<unassigned>

Priority

0

Preemption Type

Abort ongoing acquisition, do not return

☒ Group End

Output Trigger Type

Pulse

Input

☒ P12[5] analog (CYBSP_A13) [USED]

☐ Enable External Analog Mux

Precondition Mode

Discharge to VREFL

Overlap Diagnostic Mode

No Overlap or SARMUX Diagnostic

Code Preview

12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

☒ 0 Errors

☐ 0 Warnings

☐ 0 Tasks

☐ 1 Info

▼ Fix

Description

Location

Ready

ADC1 channel 5 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 1 (SAR1) - Parameters

Enter filter text...

Name	Value
Input	P12[5] analog (CYBSP_A13) [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535
Advanced	
Store Config in Flash	☒

Code Preview 12-bit SAR ADC 1 (SAR1) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

ADC2 配置



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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
▼ Analog		
▼ Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
▼ Communication		
> Controller Area Network FD (CAN FD) 0		
> Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
▼ Overview	
Configuration Help	Open SAR2 Documentation
▼ General	
Enable SAR Block	☒
Enable The SAR MUX	☒
Enable The SAR ADC	☒
Precondition Time	3
Power Up Time	0
Power Down If Idle	☐
MSB Cycles	Use 1 clock cycles per conversion
Half LSB	☐
Number Of Channels	6
▼ Connections	
Clock	24.5 bit Divider 0 clk [SHARED]
Clock Frequency	8.333333 MHz
▼ Channel 0	
Channel Name	channel_0
Enabled	☒
HW Trigger	TCPWM

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

ADC2 channel 0 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0 SAR SAR2-1.

☒ 12-bit SAR ADC 1 SAR1 SAR2-1.

☒ 12-bit SAR ADC 2 SAR2 SAR2-1.

☐ epassaref pass 0 aref 0

▼ Communication

> Controller Area Network FD (CAN FD) 0

> Controller Area Network FD (CAN FD) 1

☐ Ethernet 0 eth 0

☐ Ethernet 1 eth 1

☐ Inter-IC Sound Bus (I2S) 0 audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1 audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2 audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0 smif 0

☐ SD Host Controller (SDHC) 0 sdhc 0

☐ Serial Communication Block (SCB) 0 scb 0

☐ Serial Communication Block (SCB) 1 scb 1

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name

Value

▼ Channel 0

Channel Name channel_0

Enabled ☒

HW Trigger TCPWM

Trigger Input TCPWM[1] Group[1] 16-bit Counter 2 out 0 (PWM2) [USED]

Trigger Output <unassigned>

Trigger Chanel Input TCPWM[1] Group[1] 16-bit Counter 2 out 1 (PWM2) [USED]

Voltage Range Trigger Output <unassigned>

Channel Done Trigger Output <unassigned>

Debug Freeze Input <unassigned>

Priority 0

Preemption Type Abort ongoing acquisition, do not return

Group End ☐

Output Trigger Type Pulse

Input P18[0] analog [USED]

Enable External Analog Mux ☐

Precondition Mode Discharge to VREFL

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

2025-08-23

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ADC2 channel 0 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P18[0] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC2 channel 1 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Channel 1	
Channel Name	channel_1
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	☒ P18[1] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

ADC2 channel 1 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P18[1] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC2 channel 2 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0

☒ 12-bit SAR ADC 1

☒ 12-bit SAR ADC 2

☐ epassaref

▼ Communication

> Controller Area Network FD (CAN FD) 0

> Controller Area Network FD (CAN FD) 1

☐ Ethernet 0

☐ Ethernet 1

☐ Inter-IC Sound Bus (I2S) 0

☐ Inter-IC Sound Bus (I2S) 1

☐ Inter-IC Sound Bus (I2S) 2

☐ Quad Serial Memory Interface (QSPI) 0

☐ SD Host Controller (SDHC) 0

☐ Serial Communication Block (SCB) 0

☐ Serial Communication Block (SCB) 1

Name(s)

Persona

SAR

SAR1

SAR2

pass 0 aref 0

SAR2-1.

SAR2-1.

SAR2-1.

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name

Value

▼ Channel 2

Channel Name

channel_2

Enabled

☒

HW Trigger

Disabled

Trigger Input

<unassigned>

Trigger Output

<unassigned>

Trigger Chanel Input

<unassigned>

Voltage Range Trigger Output

<unassigned>

Channel Done Trigger Output

<unassigned>

Debug Freeze Input

<unassigned>

Priority

0

Preemption Type

Abort ongoing acquisition, do not return

Group End

☐

Output Trigger Type

Pulse

Input

P18[2] analog [USED]

Enable External Analog Mux

☐

Precondition Mode

Discharge to VREFL

Overlap Diagnostic Mode

No Overlap or SARMUX Diagnostic

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

ADC2 channel 2 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	P18[2] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location

Ready

ADC2 channel 3 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

▼ Analog

▼ Programmable Analog

☒ 12-bit SAR ADC 0

SAR

SAR2-1.

☒ 12-bit SAR ADC 1

SAR1

SAR2-1.

☒ 12-bit SAR ADC 2

SAR2

SAR2-1.

☐ epassaref

pass 0 aref 0

▼ Communication

▶ Controller Area Network FD (CAN FD) 0

▶ Controller Area Network FD (CAN FD) 1

☐ Ethernet 0

eth 0

☐ Ethernet 1

eth 1

☐ Inter-IC Sound Bus (I2S) 0

audioss 0 i2s 0

☐ Inter-IC Sound Bus (I2S) 1

audioss 1 i2s 0

☐ Inter-IC Sound Bus (I2S) 2

audioss 2 i2s 0

☐ Quad Serial Memory Interface (QSPI) 0

smif 0

☐ SD Host Controller (SDHC) 0

sdhc 0

☐ Serial Communication Block (SCB) 0

scb 0

☐ Serial Communication Block (SCB) 1

scb 1

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name

Value

▼ Channel 3

Channel Name

channel_3

☒ Enabled

HW Trigger

Disabled

Trigger Input

<unassigned>

Trigger Output

<unassigned>

Trigger Chanel Input

<unassigned>

Voltage Range Trigger Output

<unassigned>

Channel Done Trigger Output

<unassigned>

Debug Freeze Input

<unassigned>

Priority

0

Preemption Type

Abort ongoing acquisition, do not return

☐ Group End

Output Trigger Type

Pulse

Input

☒ P18[3] analog [USED]

☐ Enable External Analog Mux

Precondition Mode

Discharge to VREFL

Overlap Diagnostic Mode

No Overlap or SARMUX Diagnostic

Code Preview

12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

☒ 0 Errors

☐ 0 Warnings

☐ 0 Tasks

☐ 1 Info

▼ Fix

Description

Location

Ready

ADC2 channel 3 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P18[3] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
-----	-------------	----------

Ready

ADC2 channel 4 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Channel 4	
Channel Name	channel_4
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☐
Output Trigger Type	Pulse
Input	P18[4] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
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Ready

ADC2 channel 4 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bps/TARGET_APP_KIT_XMC72_EVK/config/design.modus - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Group End	☐
Output Trigger Type	Pulse
Input	☒ P18[4] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
-----	-------------	----------

Ready

ADC2 channel 5 配置

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File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
Controller Area Network FD (CAN FD) 0		
Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Channel 5	
Channel Name	channel_5
Enabled	☒
HW Trigger	Disabled
Trigger Input	<unassigned>
Trigger Output	<unassigned>
Trigger Chanel Input	<unassigned>
Voltage Range Trigger Output	<unassigned>
Channel Done Trigger Output	<unassigned>
Debug Freeze Input	<unassigned>
Priority	0
Preemption Type	Abort ongoing acquisition, do not return
Group End	☒
Output Trigger Type	Pulse
Input	P18[5] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostic

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix	Description	Location
-----	-------------	----------

Ready

ADC2 channel 5 配置

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File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
Analog		
Programmable Analog		
☒ 12-bit SAR ADC 0	SAR	SAR2-1.
☒ 12-bit SAR ADC 1	SAR1	SAR2-1.
☒ 12-bit SAR ADC 2	SAR2	SAR2-1.
☐ epassaref	pass 0 aref 0	
Communication		
> Controller Area Network FD (CAN FD) 0		
> Controller Area Network FD (CAN FD) 1		
☐ Ethernet 0	eth 0	
☐ Ethernet 1	eth 1	
☐ Inter-IC Sound Bus (I2S) 0	audioss 0 i2s 0	
☐ Inter-IC Sound Bus (I2S) 1	audioss 1 i2s 0	
☐ Inter-IC Sound Bus (I2S) 2	audioss 2 i2s 0	
☐ Quad Serial Memory Interface (QSPI) 0	smif 0	
☐ SD Host Controller (SDHC) 0	sdhc 0	
☐ Serial Communication Block (SCB) 0	scb 0	
☐ Serial Communication Block (SCB) 1	scb 1	

12-bit SAR ADC 2 (SAR2) - Parameters

Enter filter text...

Name	Value
Input	P18[5] analog [USED]
Enable External Analog Mux	☐
Precondition Mode	Discharge to VREFL
Overlap Diagnostic Mode	No Overlap or SARMUX Diagnostics
Sample Time (Aperture)	6
Selection Of Calibration Values	Regular
Result Data Alignment	The data is right aligned in Result[11:0]
Sign Extension	Unsigned
Post Processing Mode	No Post Processing
Averaging Count	1
Shift Right	0
Positive Reload	0
Negative Reload	0
Range Detection Mode	Below Low Threshold (Result < Low)
Range Detect Low Threshold	0
Range Detect High Threshold	65535
Advanced	
Store Config in Flash	☒

Code Preview 12-bit SAR ADC 2 (SAR2) - Parameters

Notice List

0 Errors

0 Warnings

0 Tasks

1 Info

Fix

Description

Location

Ready

ADC时钟配置



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File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Personality
☐ 16 bit Divider 14	peri_0_group_1_div_16_14	
☐ 16 bit Divider 15	peri_0_group_1_div_16_15	
☐ 16 bit Divider 16	peri_0_group_1_div_16_16	
☐ 16 bit Divider 17	peri_0_group_1_div_16_17	
☐ 16 bit Divider 18	peri_0_group_1_div_16_18	
☐ 16 bit Divider 19	peri_0_group_1_div_16_19	
▼ 24.5 bit		
☒ 24.5 bit Divider 0	peri_0_group_1_div_24_5_0	Peripheral Clock-1.0 ▼
☐ 24.5 bit Divider 1	peri_0_group_1_div_24_5_1	
☐ 24.5 bit Divider 2	peri_0_group_1_div_24_5_2	
☐ 24.5 bit Divider 3	peri_0_group_1_div_24_5_3	
☐ 24.5 bit Divider 4	peri_0_group_1_div_24_5_4	
☐ 24.5 bit Divider 5	peri_0_group_1_div_24_5_5	
☐ 24.5 bit Divider 6	peri_0_group_1_div_24_5_6	
☐ 24.5 bit Divider 7	peri_0_group_1_div_24_5_7	
☐ 24.5 bit Divider 8	peri_0_group_1_div_24_5_8	
☐ 24.5 bit Divider 9	peri_0_group_1_div_24_5_9	
☐ 24.5 bit Divider 10	peri_0_group_1_div_24_5_10	

24.5 bit Divider 0 - Parameters

Enter filter text...

Name	Value
▼ Overview	
Configuration Help	Open Peripherals Clock Dividers Documentation
▼ General	
Source Clock	CLK_HF2 (100 MHz ± 0.002%)
Integer Divider	12
Fractional Divider	0
Frequency	8.333333 MHz ± 0.002%
Start on Reset	☒
Peripherals	12-bit SAR ADC 0 clock_sar (SAR) [USED] 12-bit SAR ADC 1 clock_sar (SAR1) [USED] 12-bit SAR ADC 2 clock_sar (SAR2) [USED]

Notice List

0 Errors 0 Warnings 0 Tasks 1 Info

Fix	Description	Location
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Ready

TCPWM[1] Group[1] Counter0配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bsps/TARGET_APP_KIT_XMC72_EVK/config/design.modus* - Device Configurator 4.20

File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 80 tcpwm_1_group_0_cnt_80	
☐	TCPWM[1] Group[0] 16-bit Counter 81 tcpwm_1_group_0_cnt_81	
☐	TCPWM[1] Group[0] 16-bit Counter 82 tcpwm_1_group_0_cnt_82	
☐	TCPWM[1] Group[0] 16-bit Counter 83 tcpwm_1_group_0_cnt_83	
✓	TCPWM[1] Group 1	
✓	TCPWM[1] Group[1] 16-bit Counter 0 PWM	PWM-1.
✓	TCPWM[1] Group[1] 16-bit Counter 1 PWM1	PWM-1.
✓	TCPWM[1] Group[1] 16-bit Counter 2 PWM2	PWM-1.
☐	TCPWM[1] Group[1] 16-bit Counter 3 tcpwm 1 group 1 cnt 3	
☐	TCPWM[1] Group[1] 16-bit Counter 4 tcpwm 1 group 1 cnt 4	
☐	TCPWM[1] Group[1] 16-bit Counter 5 tcpwm 1 group 1 cnt 5	
☐	TCPWM[1] Group[1] 16-bit Counter 6 tcpwm 1 group 1 cnt 6	
☐	TCPWM[1] Group[1] 16-bit Counter 7 tcpwm 1 group 1 cnt 7	
☐	TCPWM[1] Group[1] 16-bit Counter 8 tcpwm 1 group 1 cnt 8	
☐	TCPWM[1] Group[1] 16-bit Counter 9 tcpwm 1 group 1 cnt 9	
☐	TCPWM[1] Group[1] 16-bit Counter 10 tcpwm 1 group 1 cnt 10	
☐	TCPWM[1] Group[1] 16-bit Counter 11 tcpwm 1 group 1 cnt 11	

TCPWM[1] Group[1] 16-bit Counter 0 (PWM) - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open PWM (TCPWM) Documentation
General	
PWM Mode	PWM
Clock Prescaler	Divide by 1
PWM Resolution	16-bits
PWM Alignment	Left Aligned
Run Mode	Continuous
Period	
Enable Period Swap	☐
Period	10000
Compare	
Enable Compare 0 Swap	☐
Compare 0	5000
Enable Compare 1 Swap	☐
Compare 1	5000
Stepper Motor Control	
Enable Line Sel Swap	☐
Line Out Source Signal	PWM Signal

Code Preview TCPWM[1] Group[1] 16-bit Counter 0 (PWM) - Parameters

Notice List

0 Errors 0 Warnings 0 Tasks 1 Info

Fix	Description	Location
-----	-------------	----------

Ready

TCPWM[1] Group[1] Counter0配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bsps/TARGET_APP_KIT_XMC72_EVK/config/design.modus* - Device Configurator 4.20

File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 80 tcpwm_1_group_0_cnt_80	
☐	TCPWM[1] Group[0] 16-bit Counter 81 tcpwm_1_group_0_cnt_81	
☐	TCPWM[1] Group[0] 16-bit Counter 82 tcpwm_1_group_0_cnt_82	
☐	TCPWM[1] Group[0] 16-bit Counter 83 tcpwm_1_group_0_cnt_83	
✓	TCPWM[1] Group 1	
✓	TCPWM[1] Group[1] 16-bit Counter 0 PWM	PWM-1.
✓	TCPWM[1] Group[1] 16-bit Counter 1 PWM1	PWM-1.
✓	TCPWM[1] Group[1] 16-bit Counter 2 PWM2	PWM-1.
☐	TCPWM[1] Group[1] 16-bit Counter 3 tcpwm 1 group 1 cnt 3	
☐	TCPWM[1] Group[1] 16-bit Counter 4 tcpwm 1 group 1 cnt 4	
☐	TCPWM[1] Group[1] 16-bit Counter 5 tcpwm 1 group 1 cnt 5	
☐	TCPWM[1] Group[1] 16-bit Counter 6 tcpwm 1 group 1 cnt 6	
☐	TCPWM[1] Group[1] 16-bit Counter 7 tcpwm 1 group 1 cnt 7	
☐	TCPWM[1] Group[1] 16-bit Counter 8 tcpwm 1 group 1 cnt 8	
☐	TCPWM[1] Group[1] 16-bit Counter 9 tcpwm 1 group 1 cnt 9	
☐	TCPWM[1] Group[1] 16-bit Counter 10 tcpwm 1 group 1 cnt 10	
☐	TCPWM[1] Group[1] 16-bit Counter 11 tcpwm 1 group 1 cnt 11	

TCPWM[1] Group[1] 16-bit Counter 0 (PWM) - Parameters

Enter filter text...

Name	Value
✓ Stepper Motor Control	
? Enable Line Sel Swap	☐
? Line Out Source Signal	PWM Signal
? Line Compl Out Source Signal	Inverted PWM Signal
? Buf Line Out Source Signal	PWM Signal
? Buff Line Compl Out Source Signal	Inverted PWM Signal
✓ Interrupt Source	
? Overflow & Underflow	☐
? Compare 0	☒
? Compare 1	☐
✓ Kill Mode	
? PWM Stop on Kill	☒
? PWM Sync Kill	☐
? PWM Immediate Kill	☐
? PWM Terminal Count Sync Kill DT	☐
? PWM Sync Kill DT	☐
✓ Inputs	
? Clock Signal	☒ 8 bit Divider 0 clk [SHARED]
? Count Input	Disabled

Code Preview TCPWM[1] Group[1] 16-bit Counter 0 (PWM) - Parameters

Notice List

✖ 0 Errors ⚠ 0 Warnings 📋 0 Tasks ⓘ 1 Info

Fix	Description	Location
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Ready

TCPWM[1] Group[1] Counter0配置

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File Edit Settings View Help

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 75	tcpwm_1_group_0_cnt_75
☐	TCPWM[1] Group[0] 16-bit Counter 76	tcpwm_1_group_0_cnt_76
☐	TCPWM[1] Group[0] 16-bit Counter 77	tcpwm_1_group_0_cnt_77
☐	TCPWM[1] Group[0] 16-bit Counter 78	tcpwm_1_group_0_cnt_78
☐	TCPWM[1] Group[0] 16-bit Counter 79	tcpwm_1_group_0_cnt_79
☐	TCPWM[1] Group[0] 16-bit Counter 80	tcpwm_1_group_0_cnt_80
☐	TCPWM[1] Group[0] 16-bit Counter 81	tcpwm_1_group_0_cnt_81
☐	TCPWM[1] Group[0] 16-bit Counter 82	tcpwm_1_group_0_cnt_82
☐	TCPWM[1] Group[0] 16-bit Counter 83	tcpwm_1_group_0_cnt_83
▼ TCPWM[1] Group 1		
☒	TCPWM[1] Group[1] 16-bit Counter 0	PWM
☒	TCPWM[1] Group[1] 16-bit Counter 1	PWM1
☒	TCPWM[1] Group[1] 16-bit Counter 2	PWM2
☐	TCPWM[1] Group[1] 16-bit Counter 3	tcpwm_1_group_1_cnt_3
☐	TCPWM[1] Group[1] 16-bit Counter 4	tcpwm_1_group_1_cnt_4
☐	TCPWM[1] Group[1] 16-bit Counter 5	tcpwm_1_group_1_cnt_5
☐	TCPWM[1] Group[1] 16-bit Counter 6	tcpwm_1_group_1_cnt_6
☐	TCPWM[1] Group[1] 16-bit Counter 7	tcpwm_1_group_1_cnt_7
☐	TCPWM[1] Group[1] 16-bit Counter 8	tcpwm_1_group_1_cnt_8
☐	TCPWM[1] Group[1] 16-bit Counter 9	tcpwm_1_group_1_cnt_9
☐	TCPWM[1] Group[1] 16-bit Counter 10	tcpwm_1_group_1_cnt_10
☐	TCPWM[1] Group[1] 16-bit Counter 11	tcpwm_1_group_1_cnt_11
> TCPWM[1] Group 2		
> System		

Ready

TCPWM[1] Group[1] 16-bit Counter 0 (PWM) - Parameters

Enter filter text...

Name	Value
▼ Inputs	
⌵ Clock Signal	8 bit Divider 0 clk [SHARED]
⌵ Count Input	Disabled
⌵ Kill 0 Input	Disabled
⌵ Reload Input	Rising Edge
⌵ Reload Signal	TCPWM[0] Group[0] 16-bit Counter 0 out 0 (PWM S) [SHARED]
⌵ Start Input	Disabled
⌵ Swap Input	Disabled
⌵ Kill 1 Input	Disabled
▼ PWM Output Polarity	
⌵ Invert PWM Output	☐
⌵ Invert PWM_n Output	☐
▼ PWM Disabled Output	
⌵ PWM Disabled Output	High Impedance
▼ Outputs	
⌵ PWM (line)	P3[5] digital_out [USED]
⌵ PWM_n (line_compl)	<unassigned>
▼ Trigger Outputs	
⌵ Trigger 0 Event	Compare 0 Match
⌵ Trigger 0 Signal	12-bit SAR ADC 0 tr_sar_gen_in[0] (SAR) [USED]
⌵ Trigger 1 Event	Compare 0 Match
⌵ Trigger 1 Signal	12-bit SAR ADC 0 tr_sar_ch_in[0] (SAR) [USED]
▼ Advanced	
⌵ Store Config in Flash	☒

Code Preview TCPWM[1] Group[1] 16-bit Counter 0 (PWM) - Parameters

TCPWM[1] Group[1] Counter1 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bsps/TARGET_APP_KIT_XMC72_EVK/config/design.modus* - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 75 tcpwm_1_group_0_cnt_75	
☐	TCPWM[1] Group[0] 16-bit Counter 76 tcpwm_1_group_0_cnt_76	
☐	TCPWM[1] Group[0] 16-bit Counter 77 tcpwm_1_group_0_cnt_77	
☐	TCPWM[1] Group[0] 16-bit Counter 78 tcpwm_1_group_0_cnt_78	
☐	TCPWM[1] Group[0] 16-bit Counter 79 tcpwm_1_group_0_cnt_79	
☐	TCPWM[1] Group[0] 16-bit Counter 80 tcpwm_1_group_0_cnt_80	
☐	TCPWM[1] Group[0] 16-bit Counter 81 tcpwm_1_group_0_cnt_81	
☐	TCPWM[1] Group[0] 16-bit Counter 82 tcpwm_1_group_0_cnt_82	
☐	TCPWM[1] Group[0] 16-bit Counter 83 tcpwm_1_group_0_cnt_83	
▼	TCPWM[1] Group 1	
☒	TCPWM[1] Group[1] 16-bit Counter 0 PWM	PWM-1.
☒	TCPWM[1] Group[1] 16-bit Counter 1 PWM1	PWM-1.
☒	TCPWM[1] Group[1] 16-bit Counter 2 PWM2	PWM-1.
☐	TCPWM[1] Group[1] 16-bit Counter 3 tcpwm_1_group_1_cnt_3	
☐	TCPWM[1] Group[1] 16-bit Counter 4 tcpwm_1_group_1_cnt_4	
☐	TCPWM[1] Group[1] 16-bit Counter 5 tcpwm_1_group_1_cnt_5	
☐	TCPWM[1] Group[1] 16-bit Counter 6 tcpwm_1_group_1_cnt_6	
☐	TCPWM[1] Group[1] 16-bit Counter 7 tcpwm_1_group_1_cnt_7	
☐	TCPWM[1] Group[1] 16-bit Counter 8 tcpwm_1_group_1_cnt_8	
☐	TCPWM[1] Group[1] 16-bit Counter 9 tcpwm_1_group_1_cnt_9	
☐	TCPWM[1] Group[1] 16-bit Counter 10 tcpwm_1_group_1_cnt_10	
☐	TCPWM[1] Group[1] 16-bit Counter 11 tcpwm_1_group_1_cnt_11	
>	TCPWM[1] Group 2	
>	System	

Ready

TCPWM[1] Group[1] 16-bit Counter 1 (PWM1) - Parameters

Enter filter text...

Name	Value
▼ Overview	
Configuration Help	Open PWM (TCPWM) Documentation
▼ General	
PWM Mode	PWM
Clock Prescaler	Divide by 1
PWM Resolution	16-bits
PWM Alignment	Left Aligned
Run Mode	Continuous
▼ Period	
Enable Period Swap	☐
Period	10000
▼ Compare	
Enable Compare 0 Swap	☐
Compare 0	5000
Enable Compare 1 Swap	☐
Compare 1	5000
▼ Stepper Motor Control	
Enable Line Sel Swap	☐
Line Out Source Signal	PWM Signal
Line Compl Out Source Signal	Inverted PWM Signal
Buf Line Out Source Signal	PWM Signal
Buf Line Compl Out Source Signal	Inverted PWM Signal
▼ Interrupt Source	
Overflow & Underflow	☐
Compare 0	☒

Code Preview TCPWM[1] Group[1] 16-bit Counter 1 (PWM1) - Parameters

TCPWM[1] Group[1] Counter1 配置

C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bsps/TARGET_APP_KIT_XMC72_EVK/config/design.modus* - Device Configurator 4.20

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 75 tcpwm_1_group_0_cnt_75	
☐	TCPWM[1] Group[0] 16-bit Counter 76 tcpwm_1_group_0_cnt_76	
☐	TCPWM[1] Group[0] 16-bit Counter 77 tcpwm_1_group_0_cnt_77	
☐	TCPWM[1] Group[0] 16-bit Counter 78 tcpwm_1_group_0_cnt_78	
☐	TCPWM[1] Group[0] 16-bit Counter 79 tcpwm_1_group_0_cnt_79	
☐	TCPWM[1] Group[0] 16-bit Counter 80 tcpwm_1_group_0_cnt_80	
☐	TCPWM[1] Group[0] 16-bit Counter 81 tcpwm_1_group_0_cnt_81	
☐	TCPWM[1] Group[0] 16-bit Counter 82 tcpwm_1_group_0_cnt_82	
☐	TCPWM[1] Group[0] 16-bit Counter 83 tcpwm_1_group_0_cnt_83	
▼ TCPWM[1] Group 1		
☒	TCPWM[1] Group[1] 16-bit Counter 0 PWM	PWM-1.
☒	TCPWM[1] Group[1] 16-bit Counter 1 PWM1	PWM-1.
☒	TCPWM[1] Group[1] 16-bit Counter 2 PWM2	PWM-1.
☐	TCPWM[1] Group[1] 16-bit Counter 3 tcpwm_1_group_1_cnt_3	
☐	TCPWM[1] Group[1] 16-bit Counter 4 tcpwm_1_group_1_cnt_4	
☐	TCPWM[1] Group[1] 16-bit Counter 5 tcpwm_1_group_1_cnt_5	
☐	TCPWM[1] Group[1] 16-bit Counter 6 tcpwm_1_group_1_cnt_6	
☐	TCPWM[1] Group[1] 16-bit Counter 7 tcpwm_1_group_1_cnt_7	
☐	TCPWM[1] Group[1] 16-bit Counter 8 tcpwm_1_group_1_cnt_8	
☐	TCPWM[1] Group[1] 16-bit Counter 9 tcpwm_1_group_1_cnt_9	
☐	TCPWM[1] Group[1] 16-bit Counter 10 tcpwm_1_group_1_cnt_10	
☐	TCPWM[1] Group[1] 16-bit Counter 11 tcpwm_1_group_1_cnt_11	
> TCPWM[1] Group 2		
> System		

Ready

TCPWM[1] Group[1] 16-bit Counter 1 (PWM1) - Parameters

Enter filter text...

Name	Value
▼ Interrupt Source	
Overflow & Underflow	☐
Compare 0	☒
Compare 1	☐
▼ Kill Mode	
PWM Stop on Kill	☒
PWM Sync Kill	☐
PWM Immediate Kill	☐
PWM Terminal Count Sync Kill DT	☐
PWM Sync Kill DT	☐
▼ Inputs	
Clock Signal	☒ 8 bit Divider 0 clk [SHARED]
Count Input	Disabled
Kill 0 Input	Disabled
Reload Input	Rising Edge
Reload Signal	☒ TCPWM[0] Group[0] 16-bit Counter 0 out 0 (PWM S) [SHARED]
Start Input	Disabled
Swap Input	Disabled
Kill 1 Input	Disabled
▼ PWM Output Polarity	
Invert PWM Output	☐
Invert PWM_n Output	☐
▼ PWM Disabled Output	
PWM Disabled Output	High Impedance
▼ Outputs	

Code Preview TCPWM[1] Group[1] 16-bit Counter 1 (PWM1) - Parameters

TCPWM[1] Group[1] Counter1 配置

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XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 75	tcpwm_1_group_0_cnt_75
☐	TCPWM[1] Group[0] 16-bit Counter 76	tcpwm_1_group_0_cnt_76
☐	TCPWM[1] Group[0] 16-bit Counter 77	tcpwm_1_group_0_cnt_77
☐	TCPWM[1] Group[0] 16-bit Counter 78	tcpwm_1_group_0_cnt_78
☐	TCPWM[1] Group[0] 16-bit Counter 79	tcpwm_1_group_0_cnt_79
☐	TCPWM[1] Group[0] 16-bit Counter 80	tcpwm_1_group_0_cnt_80
☐	TCPWM[1] Group[0] 16-bit Counter 81	tcpwm_1_group_0_cnt_81
☐	TCPWM[1] Group[0] 16-bit Counter 82	tcpwm_1_group_0_cnt_82
☐	TCPWM[1] Group[0] 16-bit Counter 83	tcpwm_1_group_0_cnt_83
▼ TCPWM[1] Group 1		
☒	TCPWM[1] Group[1] 16-bit Counter 0	PWM
☒	TCPWM[1] Group[1] 16-bit Counter 1	PWM1
☒	TCPWM[1] Group[1] 16-bit Counter 2	PWM2
☐	TCPWM[1] Group[1] 16-bit Counter 3	tcpwm_1_group_1_cnt_3
☐	TCPWM[1] Group[1] 16-bit Counter 4	tcpwm_1_group_1_cnt_4
☐	TCPWM[1] Group[1] 16-bit Counter 5	tcpwm_1_group_1_cnt_5
☐	TCPWM[1] Group[1] 16-bit Counter 6	tcpwm_1_group_1_cnt_6
☐	TCPWM[1] Group[1] 16-bit Counter 7	tcpwm_1_group_1_cnt_7
☐	TCPWM[1] Group[1] 16-bit Counter 8	tcpwm_1_group_1_cnt_8
☐	TCPWM[1] Group[1] 16-bit Counter 9	tcpwm_1_group_1_cnt_9
☐	TCPWM[1] Group[1] 16-bit Counter 10	tcpwm_1_group_1_cnt_10
☐	TCPWM[1] Group[1] 16-bit Counter 11	tcpwm_1_group_1_cnt_11
> TCPWM[1] Group 2		
> System		

Ready

TCPWM[1] Group[1] 16-bit Counter 1 (PWM1) - Parameters

Enter filter text...

Name	Value
ⓘ Clock Signal	8 bit Divider 0 clk [SHARED]
ⓘ Count Input	Disabled
ⓘ Kill 0 Input	Disabled
ⓘ Reload Input	Rising Edge
ⓘ Reload Signal	TCPWM[0] Group[0] 16-bit Counter 0 out 0 (PWM S) [SHARED]
ⓘ Start Input	Disabled
ⓘ Swap Input	Disabled
ⓘ Kill 1 Input	Disabled
▼ PWM Output Polarity	
ⓘ Invert PWM Output	☐
ⓘ Invert PWM_n Output	☐
▼ PWM Disabled Output	
ⓘ PWM Disabled Output	High Impedance
▼ Outputs	
ⓘ PWM (line)	<unassigned>
ⓘ PWM_n (line_compl)	<unassigned>
▼ Trigger Outputs	
ⓘ Trigger 0 Event	Compare 0 Match
ⓘ Trigger 0 Signal	12-bit SAR ADC 1 tr_sar_gen_in[0] (SAR1) [USED]
ⓘ Trigger 1 Event	Compare 0 Match
ⓘ Trigger 1 Signal	12-bit SAR ADC 1 tr_sar_ch_in[0] (SAR1) [USED]
▼ Advanced	
ⓘ Store Config in Flash	☒

Code Preview TCPWM[1] Group[1] 16-bit Counter 1 (PWM1) - Parameters

TCPWM[1] Group[1] Counter2 配置

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 75 tcpwm_1_group_0_cnt_75	
☐	TCPWM[1] Group[0] 16-bit Counter 76 tcpwm_1_group_0_cnt_76	
☐	TCPWM[1] Group[0] 16-bit Counter 77 tcpwm_1_group_0_cnt_77	
☐	TCPWM[1] Group[0] 16-bit Counter 78 tcpwm_1_group_0_cnt_78	
☐	TCPWM[1] Group[0] 16-bit Counter 79 tcpwm_1_group_0_cnt_79	
☐	TCPWM[1] Group[0] 16-bit Counter 80 tcpwm_1_group_0_cnt_80	
☐	TCPWM[1] Group[0] 16-bit Counter 81 tcpwm_1_group_0_cnt_81	
☐	TCPWM[1] Group[0] 16-bit Counter 82 tcpwm_1_group_0_cnt_82	
☐	TCPWM[1] Group[0] 16-bit Counter 83 tcpwm_1_group_0_cnt_83	
▼ TCPWM[1] Group 1		
☒	TCPWM[1] Group[1] 16-bit Counter 0 PWM	PWM-1.
☒	TCPWM[1] Group[1] 16-bit Counter 1 PWM1	PWM-1.
☒	TCPWM[1] Group[1] 16-bit Counter 2 PWM2	PWM-1.
☐	TCPWM[1] Group[1] 16-bit Counter 3 tcpwm_1_group_1_cnt_3	
☐	TCPWM[1] Group[1] 16-bit Counter 4 tcpwm_1_group_1_cnt_4	
☐	TCPWM[1] Group[1] 16-bit Counter 5 tcpwm_1_group_1_cnt_5	
☐	TCPWM[1] Group[1] 16-bit Counter 6 tcpwm_1_group_1_cnt_6	
☐	TCPWM[1] Group[1] 16-bit Counter 7 tcpwm_1_group_1_cnt_7	
☐	TCPWM[1] Group[1] 16-bit Counter 8 tcpwm_1_group_1_cnt_8	
☐	TCPWM[1] Group[1] 16-bit Counter 9 tcpwm_1_group_1_cnt_9	
☐	TCPWM[1] Group[1] 16-bit Counter 10 tcpwm_1_group_1_cnt_10	
☐	TCPWM[1] Group[1] 16-bit Counter 11 tcpwm_1_group_1_cnt_11	
> TCPWM[1] Group 2		
> System		

Ready

TCPWM[1] Group[1] 16-bit Counter 2 (PWM2) - Parameters

Enter filter text...

Name	Value
▼ Overview	
Configuration Help	Open PWM (TCPWM) Documentation
▼ General	
PWM Mode	PWM
Clock Prescaler	Divide by 1
PWM Resolution	16-bits
PWM Alignment	Left Aligned
Run Mode	Continuous
▼ Period	
Enable Period Swap	☐
Period	10000
▼ Compare	
Enable Compare 0 Swap	☐
Compare 0	5000
Enable Compare 1 Swap	☐
Compare 1	5000
▼ Stepper Motor Control	
Enable Line Sel Swap	☐
Line Out Source Signal	PWM Signal
Line Compl Out Source Signal	Inverted PWM Signal
Buf Line Out Source Signal	PWM Signal
Buf Line Compl Out Source Signal	Inverted PWM Signal
▼ Interrupt Source	
Overflow & Underflow	☐
Compare 0	☒

Code Preview TCPWM[1] Group[1] 16-bit Counter 2 (PWM2) - Parameters

TCPWM[1] Group[1] Counter2 配置

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 75 tcpwm_1_group_0_cnt_75	
☐	TCPWM[1] Group[0] 16-bit Counter 76 tcpwm_1_group_0_cnt_76	
☐	TCPWM[1] Group[0] 16-bit Counter 77 tcpwm_1_group_0_cnt_77	
☐	TCPWM[1] Group[0] 16-bit Counter 78 tcpwm_1_group_0_cnt_78	
☐	TCPWM[1] Group[0] 16-bit Counter 79 tcpwm_1_group_0_cnt_79	
☐	TCPWM[1] Group[0] 16-bit Counter 80 tcpwm_1_group_0_cnt_80	
☐	TCPWM[1] Group[0] 16-bit Counter 81 tcpwm_1_group_0_cnt_81	
☐	TCPWM[1] Group[0] 16-bit Counter 82 tcpwm_1_group_0_cnt_82	
☐	TCPWM[1] Group[0] 16-bit Counter 83 tcpwm_1_group_0_cnt_83	
▼ TCPWM[1] Group 1		
☒	TCPWM[1] Group[1] 16-bit Counter 0 PWM	PWM-1.
☒	TCPWM[1] Group[1] 16-bit Counter 1 PWM1	PWM-1.
☒	TCPWM[1] Group[1] 16-bit Counter 2 PWM2	PWM-1.
☐	TCPWM[1] Group[1] 16-bit Counter 3 tcpwm_1_group_1_cnt_3	
☐	TCPWM[1] Group[1] 16-bit Counter 4 tcpwm_1_group_1_cnt_4	
☐	TCPWM[1] Group[1] 16-bit Counter 5 tcpwm_1_group_1_cnt_5	
☐	TCPWM[1] Group[1] 16-bit Counter 6 tcpwm_1_group_1_cnt_6	
☐	TCPWM[1] Group[1] 16-bit Counter 7 tcpwm_1_group_1_cnt_7	
☐	TCPWM[1] Group[1] 16-bit Counter 8 tcpwm_1_group_1_cnt_8	
☐	TCPWM[1] Group[1] 16-bit Counter 9 tcpwm_1_group_1_cnt_9	
☐	TCPWM[1] Group[1] 16-bit Counter 10 tcpwm_1_group_1_cnt_10	
☐	TCPWM[1] Group[1] 16-bit Counter 11 tcpwm_1_group_1_cnt_11	
> TCPWM[1] Group 2		
> System		

Ready

TCPWM[1] Group[1] 16-bit Counter 2 (PWM2) - Parameters

Enter filter text...

Name	Value
▼ Interrupt Source	
Overflow & Underflow	☐
Compare 0	☒
Compare 1	☐
▼ Kill Mode	
PWM Stop on Kill	☒
PWM Sync Kill	☐
PWM Immediate Kill	☐
PWM Terminal Count Sync Kill DT	☐
PWM Sync Kill DT	☐
▼ Inputs	
Clock Signal	☒ 8 bit Divider 0 clk [SHARED]
Count Input	Disabled
Kill 0 Input	Disabled
Reload Input	Rising Edge
Reload Signal	☒ TCPWM[0] Group[0] 16-bit Counter 0 out 0 (PWM S) [SHARED]
Start Input	Disabled
Swap Input	Disabled
Kill 1 Input	Disabled
▼ PWM Output Polarity	
Invert PWM Output	☐
Invert PWM_n Output	☐
▼ PWM Disabled Output	
PWM Disabled Output	High Impedance
▼ Outputs	

Code Preview TCPWM[1] Group[1] 16-bit Counter 2 (PWM2) - Parameters

TCPWM[1] Group[1] Counter2 配置

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐	TCPWM[1] Group[0] 16-bit Counter 75	tcpwm_1_group_0_cnt_75
☐	TCPWM[1] Group[0] 16-bit Counter 76	tcpwm_1_group_0_cnt_76
☐	TCPWM[1] Group[0] 16-bit Counter 77	tcpwm_1_group_0_cnt_77
☐	TCPWM[1] Group[0] 16-bit Counter 78	tcpwm_1_group_0_cnt_78
☐	TCPWM[1] Group[0] 16-bit Counter 79	tcpwm_1_group_0_cnt_79
☐	TCPWM[1] Group[0] 16-bit Counter 80	tcpwm_1_group_0_cnt_80
☐	TCPWM[1] Group[0] 16-bit Counter 81	tcpwm_1_group_0_cnt_81
☐	TCPWM[1] Group[0] 16-bit Counter 82	tcpwm_1_group_0_cnt_82
☐	TCPWM[1] Group[0] 16-bit Counter 83	tcpwm_1_group_0_cnt_83
▼ TCPWM[1] Group 1		
☒	TCPWM[1] Group[1] 16-bit Counter 0	PWM
☒	TCPWM[1] Group[1] 16-bit Counter 1	PWM1
☒	TCPWM[1] Group[1] 16-bit Counter 2	PWM2
☐	TCPWM[1] Group[1] 16-bit Counter 3	tcpwm_1_group_1_cnt_3
☐	TCPWM[1] Group[1] 16-bit Counter 4	tcpwm_1_group_1_cnt_4
☐	TCPWM[1] Group[1] 16-bit Counter 5	tcpwm_1_group_1_cnt_5
☐	TCPWM[1] Group[1] 16-bit Counter 6	tcpwm_1_group_1_cnt_6
☐	TCPWM[1] Group[1] 16-bit Counter 7	tcpwm_1_group_1_cnt_7
☐	TCPWM[1] Group[1] 16-bit Counter 8	tcpwm_1_group_1_cnt_8
☐	TCPWM[1] Group[1] 16-bit Counter 9	tcpwm_1_group_1_cnt_9
☐	TCPWM[1] Group[1] 16-bit Counter 10	tcpwm_1_group_1_cnt_10
☐	TCPWM[1] Group[1] 16-bit Counter 11	tcpwm_1_group_1_cnt_11
> TCPWM[1] Group 2		
> System		

Ready

TCPWM[1] Group[1] 16-bit Counter 2 (PWM2) - Parameters

Enter filter text...

Name	Value
ⓘ Clock Signal	8 bit Divider 0 clk [SHARED]
ⓘ Count Input	Disabled
ⓘ Kill 0 Input	Disabled
ⓘ Reload Input	Rising Edge
ⓘ Reload Signal	TCPWM[0] Group[0] 16-bit Counter 0 out 0 (PWM S) [SHARED]
ⓘ Start Input	Disabled
ⓘ Swap Input	Disabled
ⓘ Kill 1 Input	Disabled
▼ PWM Output Polarity	
ⓘ Invert PWM Output	☐
ⓘ Invert PWM_n Output	☐
▼ PWM Disabled Output	
ⓘ PWM Disabled Output	High Impedance
▼ Outputs	
ⓘ PWM (line)	<unassigned>
ⓘ PWM_n (line_compl)	<unassigned>
▼ Trigger Outputs	
ⓘ Trigger 0 Event	Compare 0 Match
ⓘ Trigger 0 Signal	12-bit SAR ADC 2 tr_sar_gen_in[0] (SAR2) [USED]
ⓘ Trigger 1 Event	Compare 0 Match
ⓘ Trigger 1 Signal	12-bit SAR ADC 2 tr_sar_ch_in[0] (SAR2) [USED]
▼ Advanced	
ⓘ Store Config in Flash	☒

Code Preview TCPWM[1] Group[1] 16-bit Counter 2 (PWM2) - Parameters

TCPWM[0] Group[0] Counter0 配置

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐ Serial Communication Block (SCB) 1	scb_1	
☐ Serial Communication Block (SCB) 2	scb_2	
☐ Serial Communication Block (SCB) 3	scb_3	
☐ Serial Communication Block (SCB) 4	scb_4	
☐ Serial Communication Block (SCB) 5	scb_5	
☐ Serial Communication Block (SCB) 6	scb_6	
☐ Serial Communication Block (SCB) 7	scb_7	
☐ Serial Communication Block (SCB) 8	scb_8	
☐ Serial Communication Block (SCB) 9	scb_9	
☐ Serial Communication Block (SCB) 10	scb_10	
▼ Digital		
▼ Timer, Counter, and PWM (TCPWM) 0		
▼ TCPWM[0] Group 0		
☒ TCPWM[0] Group[0] 16-bit Counter 0	PWM_S	PWM-1.
☐ TCPWM[0] Group[0] 16-bit Counter 1	tcpwm 0 group 0 cnt 1	
☐ TCPWM[0] Group[0] 16-bit Counter 2	tcpwm 0 group 0 cnt 2	
▼ TCPWM[0] Group 1		
☐ TCPWM[0] Group[1] 16-bit Counter 0	tcpwm 0 group 1 cnt 0	
☐ TCPWM[0] Group[1] 16-bit Counter 1	tcpwm 0 group 1 cnt 1	
☐ TCPWM[0] Group[1] 16-bit Counter 2	tcpwm 0 group 1 cnt 2	
▼ TCPWM[0] Group 2		
☐ TCPWM[0] Group[2] 32-bit Counter 0	tcpwm 0 group 2 cnt 0	
☐ TCPWM[0] Group[2] 32-bit Counter 1	tcpwm 0 group 2 cnt 1	
☐ TCPWM[0] Group[2] 32-bit Counter 2	tcpwm 0 group 2 cnt 2	
▼ Timer, Counter, and PWM (TCPWM) 1		

Ready

TCPWM[0] Group[0] 16-bit Counter 0 (PWM_S) - Parameters

Enter filter text...

Name	Value
▼ Overview	
Configuration Help	Open PWM (TCPWM) Documentation
▼ General	
PWM Mode	PWM
Clock Prescaler	Divide by 1
PWM Resolution	16-bits
PWM Alignment	Left Aligned
Run Mode	One Shot
▼ Period	
Enable Period Swap	☐
Period	10000
▼ Compare	
Enable Compare 0 Swap	☐
Compare 0	5000
Enable Compare 1 Swap	☐
Compare 1	5000
▼ Interrupt Source	
Overflow & Underflow	☐
Compare 0	☐
Compare 1	☐
▼ Kill Mode	
PWM Stop on Kill	☒
PWM Sync Kill	☐
PWM Immediate Kill	☐
PWM Terminal Count Sync Kill DT	☐
PWM Sync Kill DT	☐

Code Preview TCPWM[0] Group[0] 16-bit Counter 0 (PWM_S) - Parameters

该TCPWM只是为
了同时触发另外三
路PWM, 所以这
里设置为One
Shot模式即可

TCPWM[0] Group[0] Counter0 配置

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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Persona
☐ Serial Communication Block (SCB) 1	scb_1	
☐ Serial Communication Block (SCB) 2	scb_2	
☐ Serial Communication Block (SCB) 3	scb_3	
☐ Serial Communication Block (SCB) 4	scb_4	
☐ Serial Communication Block (SCB) 5	scb_5	
☐ Serial Communication Block (SCB) 6	scb_6	
☐ Serial Communication Block (SCB) 7	scb_7	
☐ Serial Communication Block (SCB) 8	scb_8	
☐ Serial Communication Block (SCB) 9	scb_9	
☐ Serial Communication Block (SCB) 10	scb_10	
▼ Digital		
▼ Timer, Counter, and PWM (TCPWM) 0		
▼ TCPWM[0] Group 0		
☒ TCPWM[0] Group[0] 16-bit Counter 0	PWM_S	PWM-1.
☐ TCPWM[0] Group[0] 16-bit Counter 1	tcpwm 0 group 0 cnt 1	
☐ TCPWM[0] Group[0] 16-bit Counter 2	tcpwm 0 group 0 cnt 2	
▼ TCPWM[0] Group 1		
☐ TCPWM[0] Group[1] 16-bit Counter 0	tcpwm 0 group 1 cnt 0	
☐ TCPWM[0] Group[1] 16-bit Counter 1	tcpwm 0 group 1 cnt 1	
☐ TCPWM[0] Group[1] 16-bit Counter 2	tcpwm 0 group 1 cnt 2	
▼ TCPWM[0] Group 2		
☐ TCPWM[0] Group[2] 32-bit Counter 0	tcpwm 0 group 2 cnt 0	
☐ TCPWM[0] Group[2] 32-bit Counter 1	tcpwm 0 group 2 cnt 1	
☐ TCPWM[0] Group[2] 32-bit Counter 2	tcpwm 0 group 2 cnt 2	
▼ Timer, Counter, and PWM (TCPWM) 1		

Ready

TCPWM[0] Group[0] 16-bit Counter 0 (PWM_S) - Parameters

Enter filter text...

Name	Value
▼ Inputs	
⌚ Clock Signal	8 bit Divider 0 clk [USED]
⌚ Count Input	Disabled
⌚ Kill 0 Input	Disabled
⌚ Reload Input	Disabled
⌚ Start Input	Disabled
⌚ Swap Input	Disabled
⌚ Kill 1 Input	Disabled
▼ PWM Output Polarity	
⌚ Invert PWM Output	☐
⌚ Invert PWM_n Output	☐
▼ PWM Disabled Output	
⌚ PWM Disabled Output	High Impedance
▼ Outputs	
⌚ PWM (line)	<unassigned>
⌚ PWM_n (line_compl)	<unassigned>
▼ Trigger Outputs	
⌚ Trigger 0 Event	Compare 0 Match
⌚ Trigger 0 Signal	☒ TCPWM[1] Group[1] 16-bit Counter 0 reload (PWM) [USED] ☒ TCPWM[1] Group[1] 16-bit Counter 1 reload (PWM1) [USED] ☒ TCPWM[1] Group[1] 16-bit Counter 2 reload (PWM2) [USED]
⌚ Trigger 1 Event	Disabled
▼ Advanced	
⌚ Store Config in Flash	☒

Code Preview TCPWM[0] Group[0] 16-bit Counter 0 (PWM_S) - Parameters

TCPWM时钟配置



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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Personality
▼ Peri Clock Group 0		
▼ 8 bit		
☒ 8 bit Divider 0	peri_0_group_0_div_8_0	Peripheral Clock-1.0 ▼
☐ 8 bit Divider 1	peri_0_group_0_div_8_1	
☐ 8 bit Divider 2	peri_0_group_0_div_8_2	
☒ 8 bit Divider 3	CYBSP_TRACE_CLK_DIV	Peripheral Clock-1.0 ▼
▼ 16 bit		
☐ 16 bit Divider 0	peri_0_group_0_div_16_0	
☐ 16 bit Divider 1	peri_0_group_0_div_16_1	
☐ 16 bit Divider 2	peri_0_group_0_div_16_2	
▼ 24.5 bit		
☐ 24.5 bit Divider 0	peri_0_group_0_div_24_5_0	
▼ Peri Clock Group 1		
▼ 8 bit		
☒ 8 bit Divider 0	peri_0_group_1_div_8_0	Peripheral Clock-1.0 ▼
☐ 8 bit Divider 1	peri_0_group_1_div_8_1	
☐ 8 bit Divider 2	peri_0_group_1_div_8_2	
☐ 8 bit Divider 3	peri_0_group_1_div_8_3	
☐ 8 bit Divider 4	peri_0_group_1_div_8_4	
☐ 8 bit Divider 5	peri_0_group_1_div_8_5	
☐ 8 bit Divider 6	peri_0_group_1_div_8_6	
☐ 8 bit Divider 7	peri_0_group_1_div_8_7	
☐ 8 bit Divider 8	peri_0_group_1_div_8_8	
☐ 8 bit Divider 9	peri_0_group_1_div_8_9	
☐ 8 bit Divider 10	peri_0_group_1_div_8_10	

8 bit Divider 0 - Parameters

Enter filter text...

Name	Value
▼ Overview	
Configuration Help Open Peripherals Clock Dividers Documentation	
▼ General	
Source Clock	CLK_HF2 (100 MHz ± 0.002%)
Divider	1
Frequency	100 MHz ± 0.002%
Start on Reset	☒
Peripherals	TCPWM[1] Group[1] 16-bit Counter 0 clock (PWM) [USED] TCPWM[1] Group[1] 16-bit Counter 1 clock (PWM1) [USED] TCPWM[1] Group[1] 16-bit Counter 2 clock (PWM2) [USED]

Code Preview 8 bit Divider 0 - Parameters

Ready

TCPWM时钟配置



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Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource	Name(s)	Personality
Peri Clock Group 0		
8 bit		
☒ 8 bit Divider 0	peri_0_group_0_div_8_0	Peripheral Clock-1.0
☐ 8 bit Divider 1	peri_0_group_0_div_8_1	
☐ 8 bit Divider 2	peri_0_group_0_div_8_2	
☒ 8 bit Divider 3	CYBSP_TRACE_CLK_DIV	Peripheral Clock-1.0
16 bit		
☐ 16 bit Divider 0	peri_0_group_0_div_16_0	
☐ 16 bit Divider 1	peri_0_group_0_div_16_1	
☐ 16 bit Divider 2	peri_0_group_0_div_16_2	
24.5 bit		
☐ 24.5 bit Divider 0	peri_0_group_0_div_24_5_0	
Peri Clock Group 1		
8 bit		
☒ 8 bit Divider 0	peri_0_group_1_div_8_0	Peripheral Clock-1.0
☐ 8 bit Divider 1	peri_0_group_1_div_8_1	
☐ 8 bit Divider 2	peri_0_group_1_div_8_2	
☐ 8 bit Divider 3	peri_0_group_1_div_8_3	
☐ 8 bit Divider 4	peri_0_group_1_div_8_4	
☐ 8 bit Divider 5	peri_0_group_1_div_8_5	
☐ 8 bit Divider 6	peri_0_group_1_div_8_6	
☐ 8 bit Divider 7	peri_0_group_1_div_8_7	
☐ 8 bit Divider 8	peri_0_group_1_div_8_8	
☐ 8 bit Divider 9	peri_0_group_1_div_8_9	
☐ 8 bit Divider 10	peri_0_group_1_div_8_10	

8 bit Divider 0 - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open Peripherals Clock Dividers Documentation
General	
Source Clock	CLK_PERI (100 MHz ± 0.002%)
Divider	1
Frequency	100 MHz ± 0.002%
Start on Reset	☒
Peripherals	☒ TCPWM[0] Group[0] 16-bit Counter 0 clock (PWM_S) [USED]

Code Preview 8 bit Divider 0 - Parameters

Ready

采样通道PIN脚配置



C:/Users/duanraym/mtw/ADC_MULTI_MTB3.2/bsps/TARGET_APP_KIT_XMC72_EVK/config/design.modus* - Device Configurator 4.20

File Edit Settings View Help

XMC7200D-E272K8384

Peripherals Pins System Peripheral-Clocks DMA

Enter filter text...

Resource

Name(s)

> Port 0

> Port 1

> Port 2

> Port 3

☐ P3[0] ioss_0_port_3_pin_0

☐ P3[1] ioss_0_port_3_pin_1

☐ P3[2] ioss_0_port_3_pin_2

☐ P3[3] ioss_0_port_3_pin_3

☒ P3[4] ioss_0_port_3_pin_4

☒ P3[5] ioss_0 port 3 pin 5

☒ P3[6] CYBSP_TEST_PIN

☐ P3[7] ioss 0 port 3 pin 7

> Port 4

> Port 5

> Port 6

☒ P6[0] ioss 0 port 6 pin 0

☒ P6[1] ioss_0_port_6_pin_1

☒ P6[2] ioss 0 port 6 pin 2

☒ P6[3] CYBSP_QSPI_SCK

☒ P6[4] ioss 0 port 6 pin 4

☒ P6[5] CYBSP_QSPI_SS, CYBSP_QSPI_FLASH_SSE

☐ P6[6] CYBSP_POT

☐ P6[7] ioss 0 port 6 pin 7

> Port 7

P6[0] - Parameters

Enter filter text...

Name

Value

> Overview

Configuration Help

Open GPIO Documentation

> General

Drive Mode

Analog High-Z. Input buffer off

Initial Drive State

High (1)

> Input

Threshold

CMOS

Interrupt Trigger Type

None

> Output

Slew Rate

Fast

Drive Strength

1 / 2

> Internal Connection

Analog

12-bit SAR ADC 0 vin[0] (SAR) [USED]

Digital Input

<unassigned>

Digital Output

<unassigned>

Digital InOut

<unassigned>

> Advanced

Store Config in Flash

☒

Code Preview

P6[0] - Parameters

Ready

确保当前采样通道PIN脚，其
Drive mode为Analog
High-Z,Input buffer off,而
非其他模式

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ADC0中断设置以及中断函数实现

```

69  /* SAR0 interrupt configuration structure */
70  const cy_stc_sysint_t SAR_IRQ_cfg = {
71      .intrSrc = ((NvicMux2_IRQn << 16) | SAR_CH5_IRQ),
72      .intrPriority = 7u
73  };
89  static void sar0_interrupt_handler(void)
90  {
91      /* Check if End-Of-Scan trigger has occurred. If yes, set sar0_isr_set flag to true */
92      uint32_t intrSource =
93          Cy_SAR2_Channel_GetInterruptStatusMasked(SAR_HW, 5);
94
95      //if (Cy_SAR2_Channel_GetInterruptStatus(SAR_HW, 0u) == CY_SAR2_INT_GRP_DONE)
96      if(CY_SAR2_INT_GRP_DONE == (intrSource & CY_SAR2_INT_GRP_DONE))
97      {
98          //Cy_GPIO_Inv(CYBSP_TEST_PIN_PORT, CYBSP_TEST_PIN_NUM);
99          sar0_isr_set = true;
100      }
101      /* Clear the interrupts */
102      Cy_SAR2_Channel_ClearInterrupt(SAR_HW, 5u ,CY_SAR2_INT_GRP_DONE);
103
104  }

201  /*Configure and register SAR0 channel interrupts*/
202  Cy_SysInt_Init(&SAR_IRQ_cfg, sar0_interrupt_handler);
203  NVIC_ClearPendingIRQ(NvicMux2_IRQn);
204  NVIC_EnableIRQ((IRQn_Type) NvicMux2_IRQn);

```

ADC0中断配置参数

ADC0中断函数实现

ADC0中断使能

ADC1中断设置以及中断函数实现

```

75 const cy_stc_sysint_t SAR1_IRQ_cfg = {
76     .intrSrc = (NvicMux3_IRQn << 16) | SAR1_CH5_IRQ),
77     .intrPriority = 7u
78 };
106 static void sar1_interrupt_handler(void)
107 {
108     /* Check if End-Of-Scan trigger has occurred. If yes, set sar0_isr_set flag to true */
109     uint32_t intrSource =
110         Cy_SAR2_Channel_GetInterruptStatusMasked(SAR1_HW, 5);
111
112     //if (Cy_SAR2_Channel_GetInterruptStatus(SAR_HW, 0u) == CY_SAR2_INT_GRP_DONE)
113     if (CY_SAR2_INT_GRP_DONE == (intrSource & CY_SAR2_INT_GRP_DONE))
114     {
115         //Cy_GPIO_Inv(CYBSP_TEST_PIN_PORT, CYBSP_TEST_PIN_NUM);
116         sar1_isr_set = true;
117     }
118     /* Clear the interrupts */
119     Cy_SAR2_Channel_ClearInterrupt(SAR1_HW, 5u, CY_SAR2_INT_GRP_DONE);
120
121 }

206 /*Configure and register SAR1 channel interrupts*/
207 Cy_SysInt_Init(&SAR1_IRQ_cfg, sar1_interrupt_handler);
208 NVIC_ClearPendingIRQ(NvicMux3_IRQn);
209 NVIC_EnableIRQ((IRQn_Type) NvicMux3_IRQn);

```

ADC1中断配置参数

ADC1中断函数实现

ADC1中断使能

ADC2中断设置以及中断函数实现

```

80  const cy_stc_sysint_t SAR2_IRQ_cfg = {
81      .intrSrc = ((NvicMux4_IRQn << 16) | SAR2_CH5_IRQ),
82      .intrPriority = 7u
83  };
123 static void sar2_interrupt_handler(void)
124 {
125     /* Check if End-Of-Scan trigger has occurred. If yes, set sar0_isr_set flag to true */
126     uint32_t intrSource =
127         Cy_SAR2_Channel_GetInterruptStatusMasked(SAR2_HW, 5);
128
129     //if (Cy_SAR2_Channel_GetInterruptStatus(SAR_HW, 0u) == CY_SAR2_INT_GRP_DONE)
130     if (CY_SAR2_INT_GRP_DONE == (intrSource & CY_SAR2_INT_GRP_DONE))
131     {
132         //Cy_GPIO_Inv(CYBSP_TEST_PIN_PORT, CYBSP_TEST_PIN_NUM);
133         sar2_isr_set = true;
134     }
135     /* Clear the interrupts */
136     Cy_SAR2_Channel_ClearInterrupt(SAR2_HW, 5u, CY_SAR2_INT_GRP_DONE);
137
138 }
211 /*Configure and register SAR2 channel interrupts*/
212 Cy_SysInt_Init(&SAR2_IRQ_cfg, sar2_interrupt_handler);
213 NVIC_ClearPendingIRQ(NvicMux4_IRQn);
214 NVIC_EnableIRQ((IRQn_Type) NvicMux4_IRQn);

```

ADC2中断配置参数

ADC2中断函数实现

ADC2中断使能

ADC0初始化

```

144  /* Initialize SAR0 */
145  status = Cy_SAR2_Init(SAR_HW, &SAR_config);
146  if (CY_SAR2_SUCCESS != status)
147  {
148  CY_ASSERT(0);
149  }
165  /* Set ePASS MMIO reference buffer mode for bangap voltage */
166  Cy_SAR2_SetReferenceBufferMode(PASS0_EPASS_MMIO, CY_SAR2_REF_BUF_MODE_OFF);
167
168  /*Initialize SAR0 channel 0~5*/
169  Cy_SAR2_Channel_Init(SAR_HW, 0u, &SAR_channel_0_config);
170  Cy_SAR2_Channel_Init(SAR_HW, 1u, &SAR_channel_1_config);
171  Cy_SAR2_Channel_Init(SAR_HW, 2u, &SAR_channel_2_config);
172  Cy_SAR2_Channel_Init(SAR_HW, 3u, &SAR_channel_3_config);
173  Cy_SAR2_Channel_Init(SAR_HW, 4u, &SAR_channel_4_config);
174  Cy_SAR2_Channel_Init(SAR_HW, 5u, &SAR_channel_5_config);
192  /*Set SAR0 channel 5 interrupt mask*/
193  Cy_SAR2_Channel_SetInterruptMask(SAR_HW, 5u, CY_SAR2_INT_GRP_DONE);
...
```

ADC1初始化

```

151  /* Initialize SAR1 */
152  status = Cy_SAR2_Init(SAR1_HW, &SAR1_config);
153  if (CY_SAR2_SUCCESS != status)
154  {
155  CY_ASSERT(0);
156  }
176  /*Initialize SAR1 channel 0~5*/
177  Cy_SAR2_Channel_Init(SAR1_HW, 0u, &SAR1_channel_0_config);
178  Cy_SAR2_Channel_Init(SAR1_HW, 1u, &SAR1_channel_1_config);
179  Cy_SAR2_Channel_Init(SAR1_HW, 2u, &SAR1_channel_2_config);
180  Cy_SAR2_Channel_Init(SAR1_HW, 3u, &SAR1_channel_3_config);
181  Cy_SAR2_Channel_Init(SAR1_HW, 4u, &SAR1_channel_4_config);
182  Cy_SAR2_Channel_Init(SAR1_HW, 5u, &SAR1_channel_5_config);
195  /*Set SAR1 channel 5 interrupt mask*/
196  Cy_SAR2_Channel_SetInterruptMask(SAR1_HW, 5u, CY_SAR2_INT_GRP_DONE);

```

ADC2初始化

```

158     /* Initialize SAR2 */
159     status = Cy_SAR2_Init(SAR2_HW, &SAR2_config);
160     if (CY_SAR2_SUCCESS != status)
161     {
162         CY_ASSERT(0);
163     }
164     /*Initialize SAR2 channel 0~5*/
165     Cy_SAR2_Channel_Init(SAR2_HW, 0u, &SAR2_channel_0_config);
166     Cy_SAR2_Channel_Init(SAR2_HW, 1u, &SAR2_channel_1_config);
167     Cy_SAR2_Channel_Init(SAR2_HW, 2u, &SAR2_channel_2_config);
168     Cy_SAR2_Channel_Init(SAR2_HW, 3u, &SAR2_channel_3_config);
169     Cy_SAR2_Channel_Init(SAR2_HW, 4u, &SAR2_channel_4_config);
170     Cy_SAR2_Channel_Init(SAR2_HW, 5u, &SAR2_channel_5_config);
171     /*Set SAR2 channel 5 interrupt mask*/
172     Cy_SAR2_Channel_SetInterruptMask(SAR2_HW, 5u, CY_SAR2_INT_GRP_DONE);

```

PWM, PWM1,PWM2初始化

```

293  /* Initialize PWM using the config structure generated using device configurator*/
294  if (CY_TCPWM_SUCCESS != Cy_TCPWM_PWM_Init(PWM_HW, PWM_NUM, &PWM_config))
295  {
296      CY_ASSERT(0);
297  }
298  /* Enable the initialized PWM */
299  Cy_TCPWM_PWM_Enable(PWM_HW, PWM_NUM);
303  /* Initialize PWM1 using the config structure generated using device configurator*/
304  if (CY_TCPWM_SUCCESS != Cy_TCPWM_PWM_Init(PWM1_HW, PWM1_NUM, &PWM1_config))
305  {
306      CY_ASSERT(0);
307  }
308  /* Enable the initialized PWM */
309  Cy_TCPWM_PWM_Enable(PWM1_HW, PWM1_NUM);
313  /* Initialize PWM2 using the config structure generated using device configurator*/
314  if (CY_TCPWM_SUCCESS != Cy_TCPWM_PWM_Init(PWM2_HW, PWM2_NUM, &PWM2_config))
315  {
316      CY_ASSERT(0);
317  }
318  /* Enable the initialized PWM */
319  Cy_TCPWM_PWM_Enable(PWM2_HW, PWM2_NUM);

```

PWM_S初始化

```

324  /* Initialize PWM1 using the config structure generated using device configurator */
325  if (CY_TCPWM_SUCCESS != Cy_TCPWM_PWM_Init(PWM_S_HW, PWM_S_NUM, &PWM_S_config))
326  {
327      CY_ASSERT(0);
328  }
329  /* Enable the initialized PWM */
330  Cy_TCPWM_PWM_Enable(PWM_S_HW, PWM_S_NUM);
331  /* Then start the TCPWM_S to synchronous PWM_U, PWM_V and PWM_W */
332  Cy_TCPWM_TriggerReloadOrIndex_Single(PWM_S_HW, PWM_S_NUM);

```

ADC0 6通道采样数据读取

```

337     if(sar0_isr_set)
338     {
339         sar0Result0 = Cy_SAR2_Channel_GetResult(SAR_HW, 0u, NULL);
340         printf("sar0Result0 = %d \r\n",sar0Result0 );
341         sar0Result1 = Cy_SAR2_Channel_GetResult(SAR_HW, 1u, NULL);
342         printf("sar0Result1 = %d \r\n",sar0Result1 );
343         sar0Result2 = Cy_SAR2_Channel_GetResult(SAR_HW, 2u, NULL);
344         printf("sar0Result2 = %d \r\n",sar0Result2 );
345         sar0Result3 = Cy_SAR2_Channel_GetResult(SAR_HW, 3u, NULL);
346         printf("sar0Result3 = %d \r\n",sar0Result3 );
347         sar0Result4 = Cy_SAR2_Channel_GetResult(SAR_HW, 4u, NULL);
348         printf("sar0Result4 = %d \r\n",sar0Result4 );
349         sar0Result5 = Cy_SAR2_Channel_GetResult(SAR_HW, 5u, NULL);
350         printf("sar0Result5 = %d \r\n",sar0Result5 );
351         sar0_isr_set = false;
352     }

```

ADC1 6通道采样数据读取

```

354     if(sar1_isr_set)
355     {
356         sar1Result0 = Cy_SAR2_Channel_GetResult(SAR1_HW, 0u, NULL);
357         printf("sar1Result0 = %d \r\n",sar1Result0 );
358         sar1Result1 = Cy_SAR2_Channel_GetResult(SAR1_HW, 1u, NULL);
359         printf("sar1Result1 = %d \r\n",sar1Result1 );
360         sar1Result2 = Cy_SAR2_Channel_GetResult(SAR1_HW, 2u, NULL);
361         printf("sar1Result2 = %d \r\n",sar1Result2 );
362         sar1Result3 = Cy_SAR2_Channel_GetResult(SAR1_HW, 3u, NULL);
363         printf("sar1Result3 = %d \r\n",sar1Result3 );
364         sar1Result4 = Cy_SAR2_Channel_GetResult(SAR1_HW, 4u, NULL);
365         printf("sar1Result4 = %d \r\n",sar1Result4 );
366         sar1Result5 = Cy_SAR2_Channel_GetResult(SAR1_HW, 5u, NULL);
367         printf("sar1Result5 = %d \r\n",sar1Result5 );
368         sar1_isr_set = false;
369     }

```

ADC2 6通道采样数据读取

```

371     if(sar2_isr_set)
372     {
373         sar2Result0 = Cy_SAR2_Channel_GetResult(SAR2_HW, 0u, NULL);
374         printf("sar2Result0 = %d \r\n",sar2Result0 );
375         sar2Result1 = Cy_SAR2_Channel_GetResult(SAR2_HW, 1u, NULL);
376         printf("sar2Result1 = %d \r\n",sar2Result1 );
377         sar2Result2 = Cy_SAR2_Channel_GetResult(SAR2_HW, 2u, NULL);
378         printf("sar2Result2 = %d \r\n",sar2Result2 );
379         sar2Result3 = Cy_SAR2_Channel_GetResult(SAR2_HW, 3u, NULL);
380         printf("sar2Result3 = %d \r\n",sar2Result3 );
381         sar2Result4 = Cy_SAR2_Channel_GetResult(SAR2_HW, 4u, NULL);
382         printf("sar2Result4 = %d \r\n",sar2Result4 );
383         sar2Result5 = Cy_SAR2_Channel_GetResult(SAR2_HW, 5u, NULL);
384         printf("sar2Result5 = %d \r\n",sar2Result5 );
385         sar2_isr_set = false;
386     }

```

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问题总结

- 三组SAR ADC unit需要分别用对应的TCPWM来进行定时触发：
 - TCPWM[1] Group[1] Counter0用来触发ADC SAR0
 - TCPWM[1] Group[1] Counter2用来触发ADC SAR1
 - TCPWM[1] Group[1] Counter2用来触发ADC SAR2

- 在采样过程中，为了避免同一采样通道上模拟信号的变化(比如从3.3V突然变成0V)，而造成采样结果的突变（由于ADC内部采样电容的存在，会导致当前采样到的数值不会马上变为0，而是持续一段时间后才归零），这时可以调整SAR中的precondition Time，并Precondition mode为Discharge to VREFL。这样作的目的是，在下次采样前，会先对ADC内部电容进行放电处理，从而避免了采样数据偏差的问题。

- 若每个ADC unit存在多个通道的使用，在设置完最后一个通道后，需要在Device configuration上勾选“Group End”

- 在对应的TCPWM中，通过设置Trigger Outputs来完成TCPWM信号与ADC SAR间的信号关联，以及触发条件。

- 若需要实现多路TCPWM同时启动，可以使用TCPWM中的reload事件，通过设置另一路one shot模式TCPWM作为触发信号，来映射到多路TCPWM的reload事件上。

- 需要确保采样通道对应的IO管脚属性为Analog High-Z,Input buffer off,否则会出现采样结果异常的情况。

