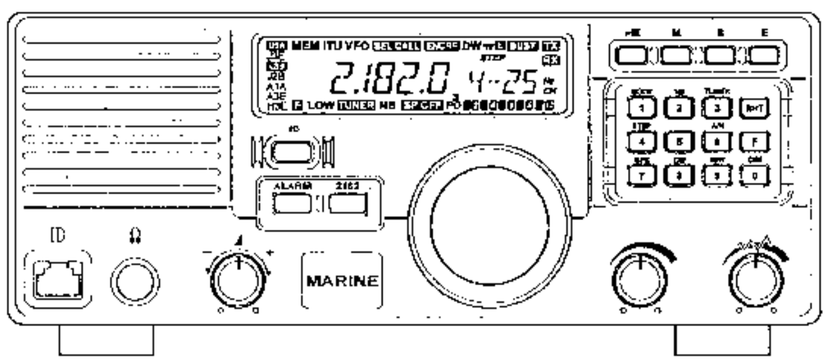
YAESU

Yaesu System 600

Service Manual



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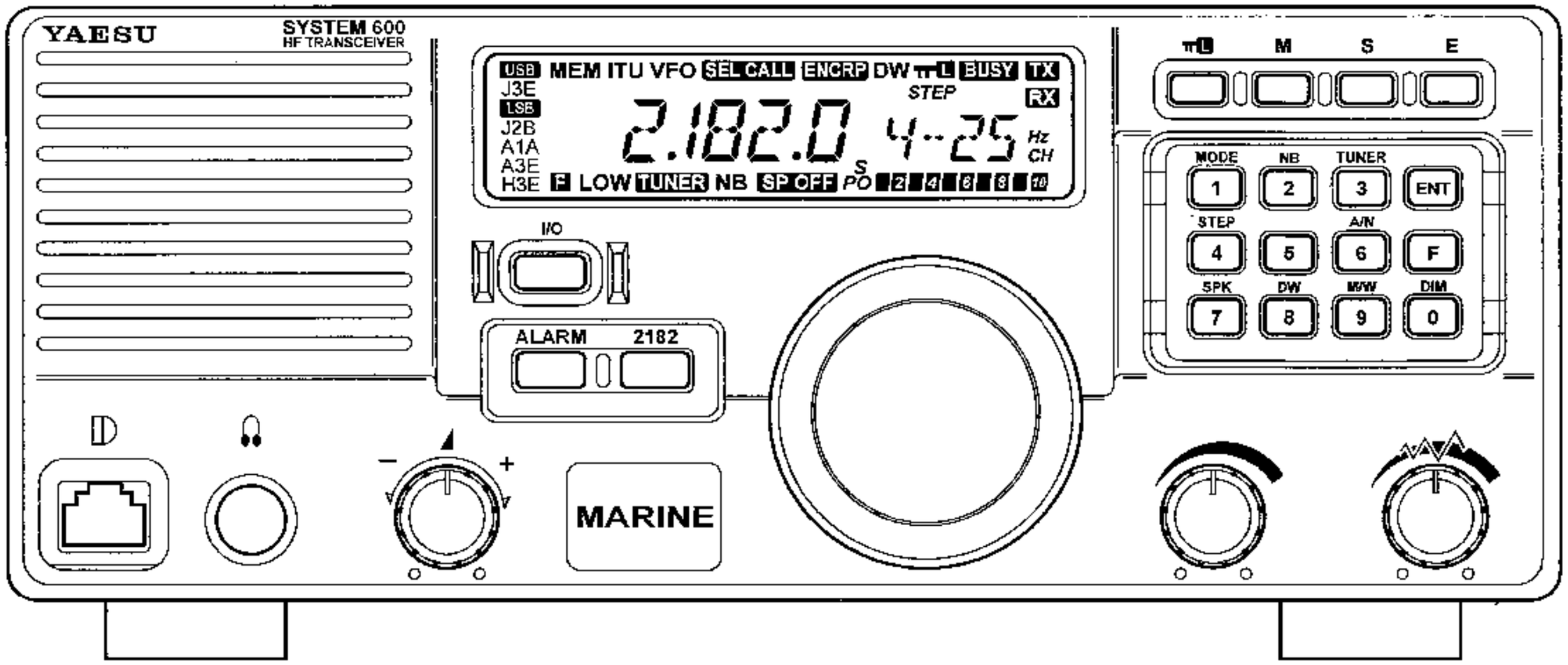


The manual provides the technical information necessary for servicing the Yaesu System 600 100 Watt HF communications transceiver.

Servicing this equipment requires expertise in handling surface-mount chip components. Attempts by non-qualified persons to service this equipment may result in permanent damage not covered by the warranty, and may be illegal in some countries.

Two PCB layout diagrams provided for each double-sided board in this transceiver. Each side of the board is referred to by the type of the majority of components installed on that side ("leaded" or "chip-only"). In most cases one side has only chip components, and the other has either a mixture of both chip and leaded components (trimmers, coils, electrolytic capacitors, ICs, etc.), or leaded components only.

While we believe the information in this manual to be correct, Yaesu Musen assumes no liability for damage that may occur as a result of typographical or other errors that may be present. Your cooperation in pointing out any inconsistencies in the technical information would be appreciated.

Specifications

General

Receiver Frequency Range: 50 kHz ~ 29.99999 MHz

Transmitter Frequency Range:

1.8 ~ 29.99999 MHz (Selected memory channels, depending on ITU Marine channels or general coverage configuration)

Emission Types:

A1A (CW)
J2B (USB, LSB)
J3E (USB, LSB)
H3E (2182 Mode only, Marine version only)
A3E (AM)

Frequency Synthesizer Step Resolution:

10 Hz, 100 Hz, 1 kHz

Frequency Stability:

±10 ppm from 0 °C ~ +40 °C (Standard Version)
±2 ppm from 0 °C ~ +50 °C (w/TCXO-4 Option)

Operating Temperature Range: -10°C ~ +50°C

Antenna Impedance:

50 Ω nominal (2:1 Maximum Permitted SWR)

Supply Voltage: 13.5 V DC ±10%, negative ground

Power Consumption:

1.2 A (Receive, no signal)
20 A (Transmit, 100 watts output)

Dimensions (WHD): 244 x 104 x 286 mm

Weight (Approx.): 4.5 kg (9.9 lbs.)

Transmitter

Power Output:

100 watts (J2B, J3E, A1A)
25 watts AM Carrier (A3E, H3E)

Modulation Types:

SSB: Balanced modulator, filtered carrier
AM: Low-level (early stage)

Spurious Radiation: 40 dB below peak output

SSB Carrier Suppression:

> 40 dB below peak output

Undesired Sideband Suppression:

At least 50 dB below peak output @ 1.5 kHz modulation input

SSB Audio Response:

Not more than -6 dB from 400 Hz ~ 2600 Hz

Occupied Bandwidth:

A1A: < 0.5 kHz
J2B: < 3.0 kHz
J3E: < 3.0kHz
H3E: < 3.0 kHz
A3E: < 6.0kHz

3rd-Order IMD:

-25 dB or better @ 100W PEP (14 MHz)

Microphone Impedance: 500 ~ 600 Ω

Receiver

Circuit Type: Double-conversion Superheterodyne

Intermediate Frequencies:

1st: 47.055 MHz, 2nd: 8.215 MHz

Sensitivity (for 10 dB S/N):

0.5 ~ 1.8 MHz: J2B/J3E/A1A 2 μV, A3E 8 μV
1.8 ~ 29.999 MHz: J2B/J3E/A1A 0.25 μV, A3E 1μV

Squelch Sensitivity:

Better than 2 μV (1.8 ~ 29.999 MHz)

IF Rejection: Better than 60 dB (1.8 ~ 29.999 MHz)

Image Rejection: Better than 70 dB (1.8 ~ 29.999 MHz)

Selectivity:

J2B/J3E/A3E-Narrow/H3E-Narrow/A1A-Wide
2.2 kHz (-6 dB), 5.0 kHz (-60 dB)
A1A-Narrow 500 Hz (-6 dB), 1.2 kHz (-60 dB)
A3E 6.0 kHz (-6 dB), 12.0 kHz (-60 dB)

Clarifier Range: ±300 Hz

Audio Output:

At least 1.5 watts into 4 Ω (@ 10% THD or less)

Conducted Radiation: Less than -55 dBm

Spurious Responses:

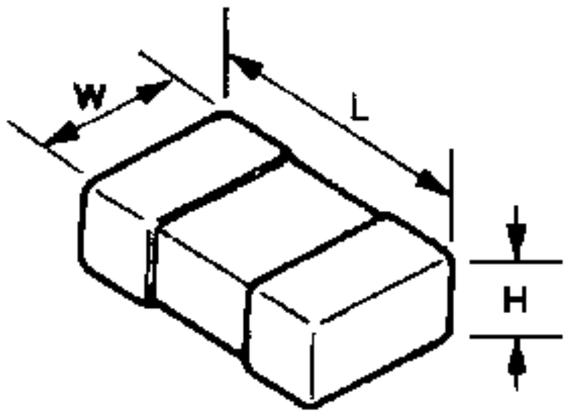
Below 1 mV equivalent signal level. (Except discrete spurious responses at 5.2428 MHz , 8.2150 MHz, 10.4857 MHz, and 19.6610MHz)

Specifications may be subject to change without notice.

Chip Component Information

The diagrams below indicate some of the distinguishing features of common chip components .

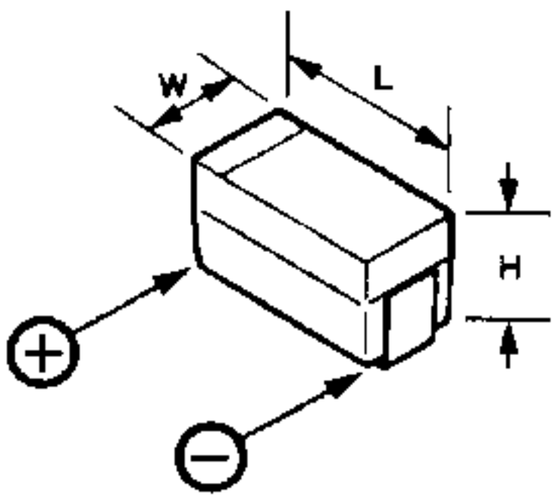
Capacitors



(Unit: mm)

Type	L	W	H
2125	2.0	1.25	0.35 ~ 0.5
1608	1.6	0.8	0.65 ~ 0.95
1005	1.0	0.5	0.45 ~ 0.55

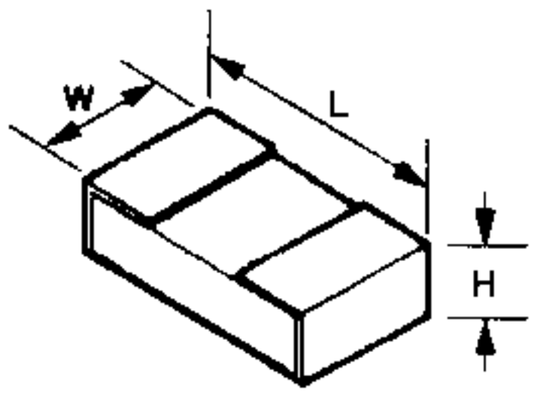
Tantalum Capacitors



(Unit: mm)

Type	L	W	H
I'	2.0	1.25	1.2
A	3.2	1.6	1.6
B	3.4	2.8	1.9
C	5.8	3.2	2.3

Resistors



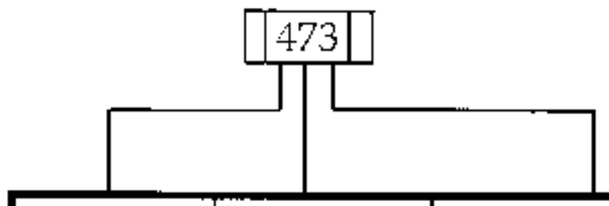
Indicated Letters

1 2 3 4 5 6 7 8 9 0 .

(Unit: mm)

Type	L	W	H
1/10	2.0	1.25	0.5
1/16	1.6	0.8	0.45
1/16S	1.0	0.5	0.35

Marking* 100, 222, 473...



Ten unit	One unit	Multiplier code
0	0	10^0
1	1	10^1
2	2	10^2
3	3	10^3
4	4	10^4
5	5	10^5
6	6	10^6
7	7	10^7
8	8	10^8
9	9	10^9

Examples: 100=10Ω
222=2.2kΩ
473=47kΩ

Chip Component Information

Replacing Chip Components

Chip components are installed at the factory by a series of robots. The first one places a small spot of adhesive resin at the location where each part is to be installed, and later robots handle and place parts using vacuum suction.

For single sided boards, solder paste is applied and the board is then baked to harden the resin and flow the solder. For double sided boards, no solder paste is applied, but the board is baked (or exposed to ultra-violet light) to cure the resin before dip soldering.

In our laboratories and service shops, small quantities of chip components are mounted manually by applying a spot of resin, placing with tweezers, and then soldering by very small dual streams of hot air (without physical contact during soldering). We remove parts by first removing solder using a vacuum suction iron, which applies a light steady vacuum at the iron tip, and then breaking the adhesive with tweezers.

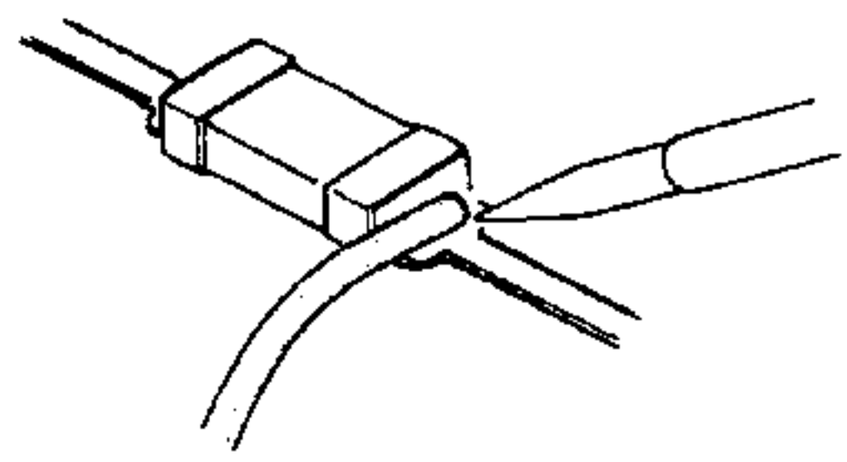
The special vacuum/desoldering equipment is recommended if you expect to do a lot of chip replacements. Otherwise, it is usually possible to remove and replace chip components with only a tapered, temperature-controlled soldering iron, a set of tweezers and braided copper solder wick. Soldering iron temperature should be below 280°C (536°F).

Precautions for Chip Replacement

- ○ Do not disconnect a chip forcefully, or the foil pattern may peel off the board.
- ○ Never re-use a chip component. Dispose of all removed chip components immediately to avoid mixing with new parts.
- ○ Limit soldering time to 3 seconds or less to avoid damaging the component and board.

Removing Chip Components

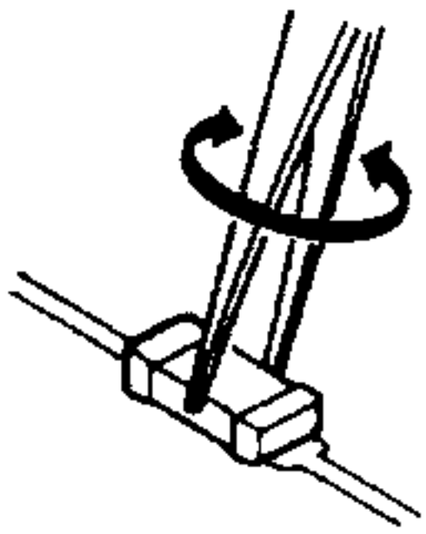
❒ Remove the solder at each joint, one joint at a time, using solder wick whetted with nonacidic fluxes as shown below. Avoid applying pressure, and do not attempt to remove tinning from the chip's electrode.



❒ Grasp the chip on both sides with tweezers, and gently twist the tweezers back and forth (to break the adhesive bond) while alternately heating each electrode. Be careful to avoid peeling the foil traces from the board.

Dispose of the chip when removed.

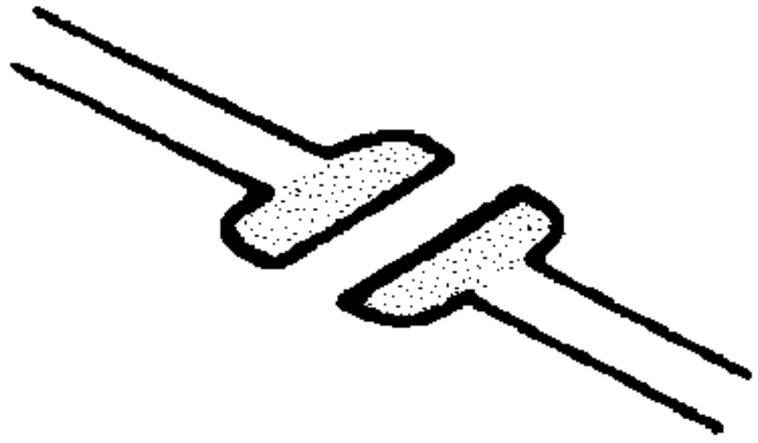
❒ After removing the chip, use the copper braid and soldering iron to wick away any excess solder and smooth the land for installation of the replacement part.



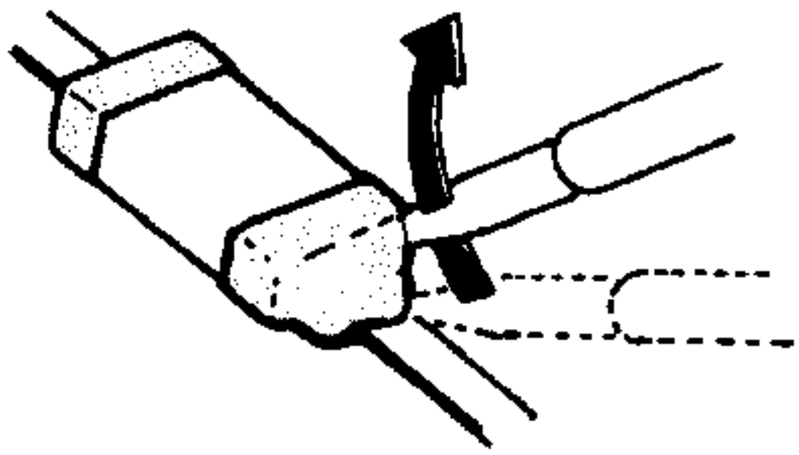
Installing a Replacement Chip

As the value of some chip components is not indicated on the body of the chip, be careful to get the right part for replacement.

❒ Apply a small amount of solder to the land on one side where the chip is to be installed. Avoid too much solder, which may cause bridging (shorting to other parts).



❒ Hold the chip with tweezers in the desired position, and apply the soldering iron with a motion line as indicated by the arrow in the diagram below. Do not apply heat for more than 3 seconds.



❒ Remove the tweezers and solder the elec trode on the other side in the manner just described.

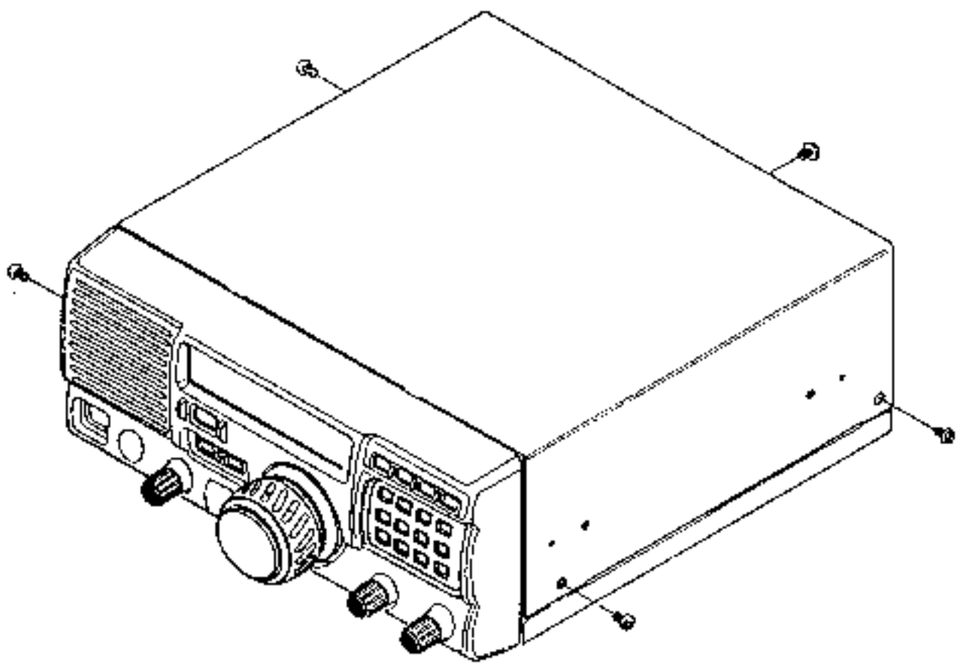
Circuit Board Access

Unit Access

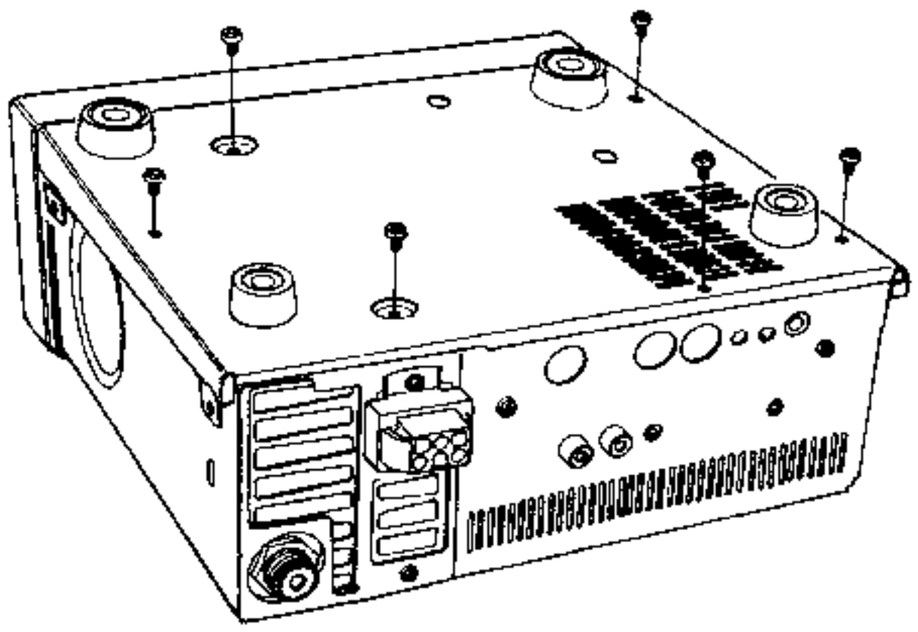
Turn the transceiver off and disconnect all cables.

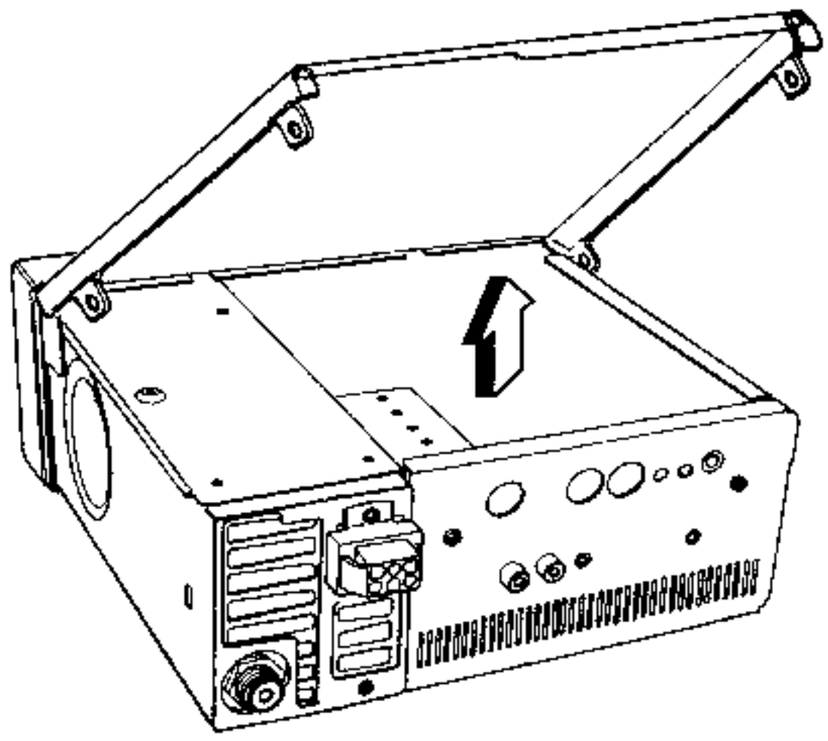
Remove the 5 screws affixing the top cover.

You may now remove the top cover to expose the component side of the Main Unit.

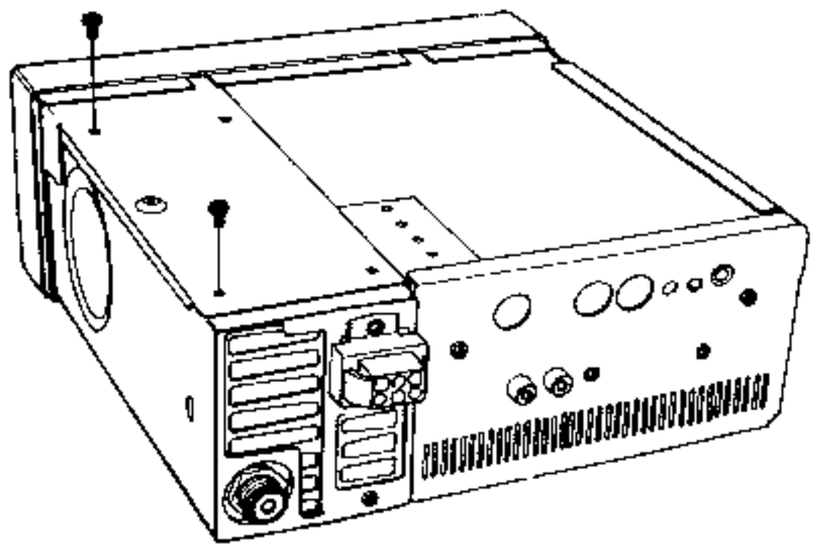


Place the set upside-down on the work surface, then remove the 6 screws affixing the bottom cover. Remove the cover to expose the components side of the Local Unit.

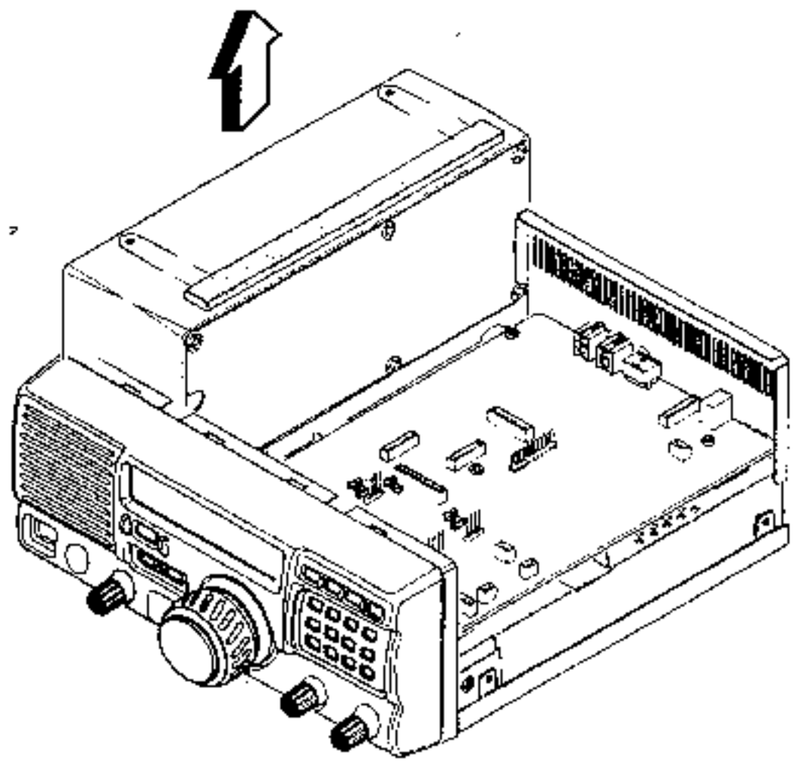




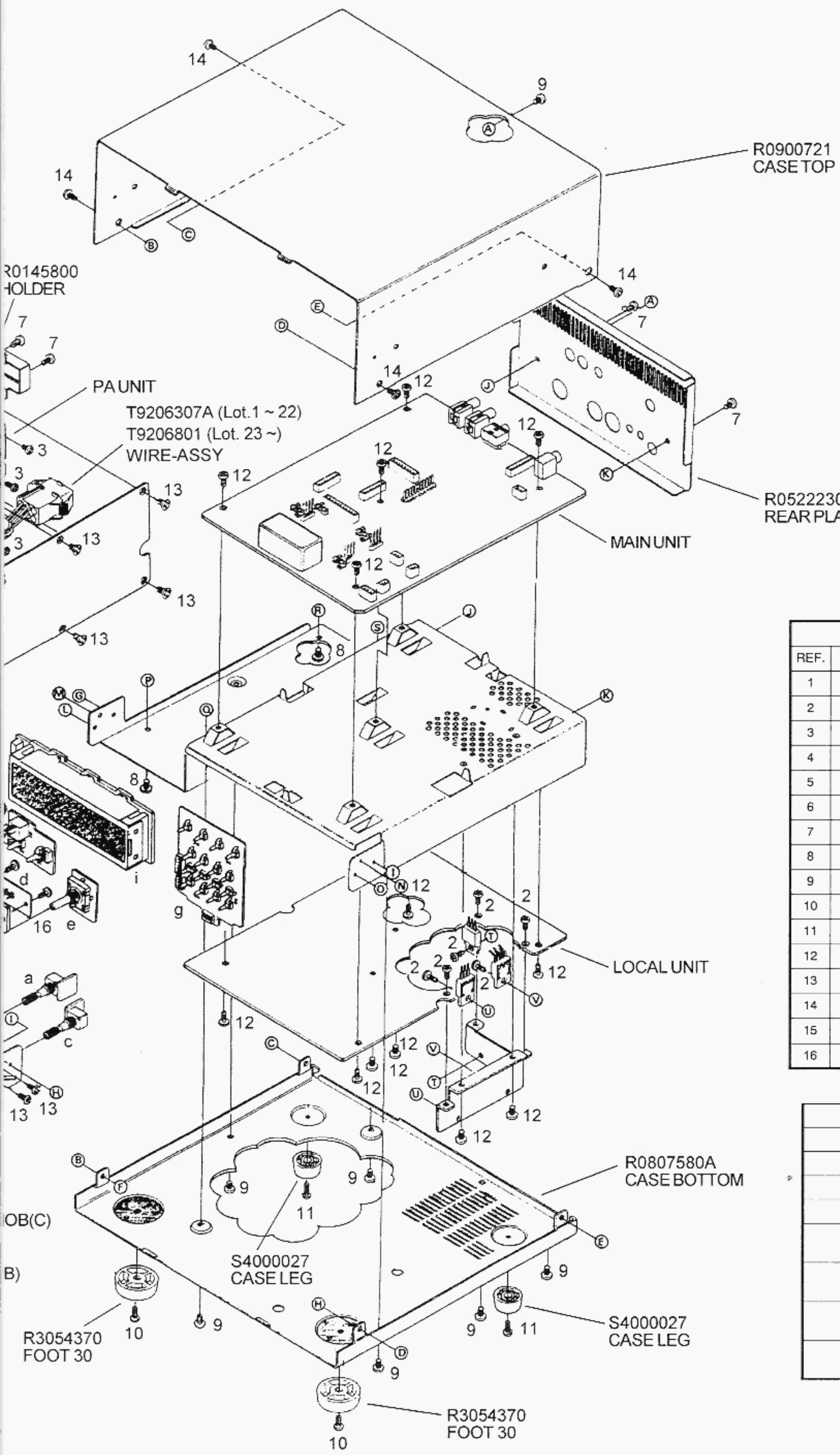
To remove the PA Unit (with the set upside-down), remove the 2 screws affixing the PA Unit to the transceiver chassis.



Next remove the connecting wire and coaxial cables leading from the Main and Local Units, then remove the PA Unit from the chassis.



Exploded View & Miscellaneous Parts

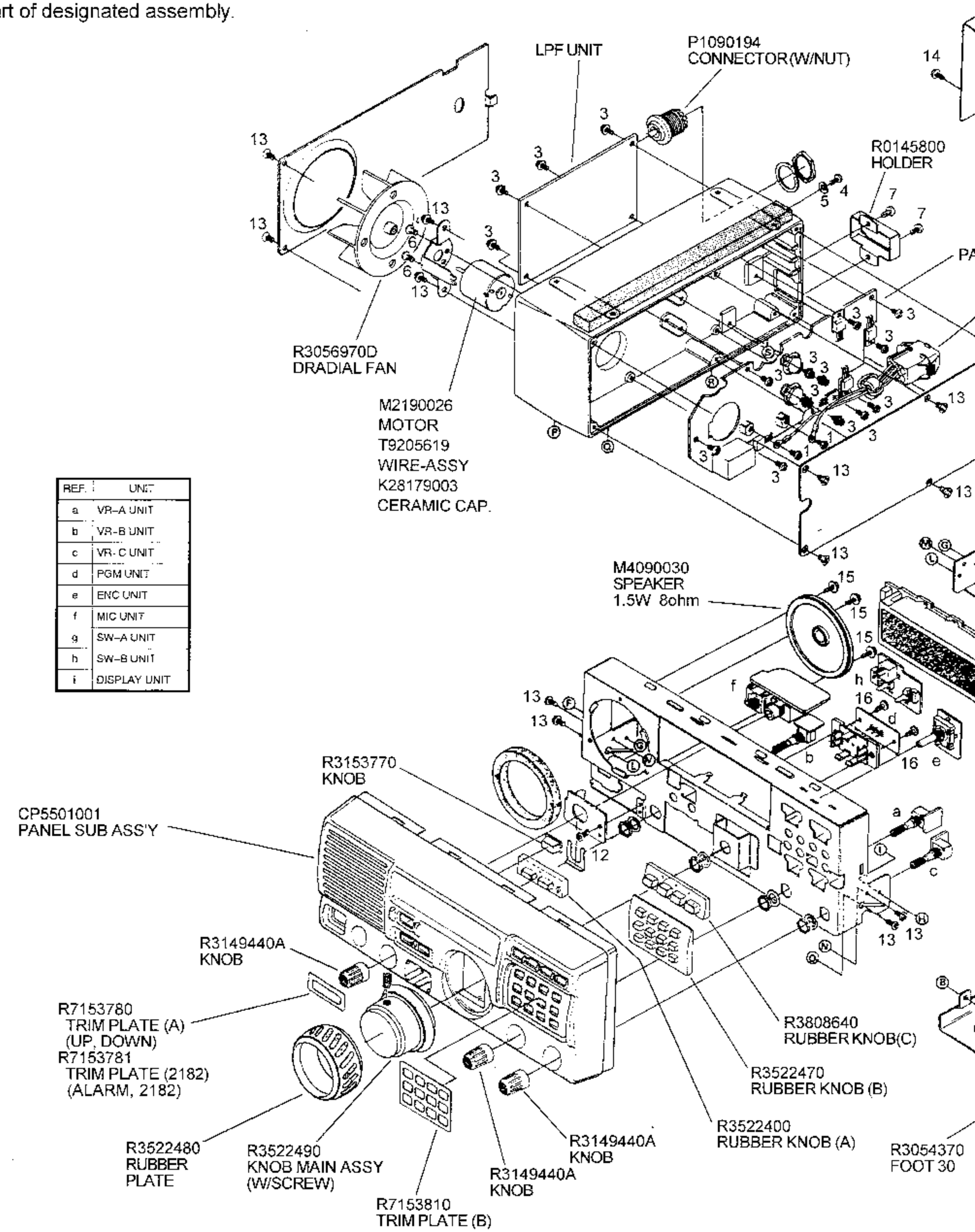


Screw List			
REF.	YAESU P/N	Description	Qty.
1	U02306001	SEMS SCREW SM3X6	2
2	U24206001	TAPTITE SCREW M2.6X6	6
3	U03308001	SEMS SCREW ASM3X8	16
4	U04310002	SEMS SCREW HSM3X10NI	1
5	U73004002	TOOTHED LOCK WASHER IW4NI	1
6	U20304001	BINDING HEAD SCREW M3X4	2
7	U20305002	BINDING HEAD SCREW	4
8	U20306001	BINDING HEAD SCREW	2
9	U20306007	BINDING HEAD SCREW	7
10	U20406007	BINDING HEAD SCREW	2
11	U20408007	BINDING HEAD SCREW	2
12	U24306001	TAPTITE SCREW M3X6	14
13	U30306001	FLAT HEAD SCREW M3X6	14
14	U31306007	OVAL HEAD SCREW M3X6B	4
15	U9900010	TAPTITE SCREW HM3X6B	3
16	U23210001	TAPTITE SCREW M2.6X10	2

Basic Accessories	
Description	YAESU P/N
20-Amp Fuse	Q0000009
DC Cable	T9018320
3.5mm Plug (Stereo)	P0091046
Key Cover Jig (Release Plate)	R0154420
Keypad Cover (SUB Panel A)	R3522420
2182/ALARM Cover (SUB Panel B)	R3522430
"ITU-Disable" Plug (Connector)	P1090737

Non-designated parts are available
only as part of designated assembly.

REF.	UNIT
a	VR-A UNIT
b	VR-B UNIT
c	VR-C UNIT
d	PGM UNIT
e	ENC UNIT
f	MIC UNIT
g	SW-A UNIT
h	SW-B UNIT
i	DISPLAY UNIT



Alignment

Introduction and Precautions

The Yaesu System 600 is carefully designed to allow the knowledgeable operator to make nearly all adjustments required for various station conditions, modes and operator preferences simply from the controls on the front and rear panels, without opening the case of the transceiver. These adjustments, plus certain internal settings, are described in the Yaesu System 600 Operating Manual.

The following procedures cover the sometimes critical and tedious adjustments that are not normally required once the transceiver has left the factory. However, if damage occurs and some parts are subsequently replaced, realignment may be required. If a sudden problem occurs during normal operation, it is likely due to component failure; realignment should not be done until after the faulty component has been replaced.

We recommend that servicing be performed only by authorized Yaesu service technicians, experienced with the circuitry and fully equipped for repair and alignment. So if a fault is suspected, you should contact the selling dealer for instructions regarding repair. Authorized Yaesu service technicians have the latest modification information, and realign all circuits and make complete performance checks to ensure compliance with factory specifications after replacing faulty components.

Those who do undertake any of the following alignments are cautioned to proceed at their own risk. Problems caused by unauthorized attempts at realignment are not covered by the warranty policy. Also, Yaesu reserves the right to change circuits and alignment procedures in the interest of improved performance, without notifying owners.

Under no circumstances should any alignment be attempted unless the normal function and operation of the transceiver are clearly understood, the cause of the malfunction has been clearly pinpointed and any faulty components replaced, and the need for realignment determined to be absolutely necessary.

The following test equipment (and thorough familiarity with its correct use) is necessary for complete realignment. Correction of problems caused by misalignment resulting from use of improper test equipment is not covered under the warranty policy. While most steps do not require all of the equipment listed, the interactions of some adjustments may require that more complex adjustments be performed afterwards. Do not attempt to perform only a single step unless it is clearly isolated electrically from all other steps. Rather, have all test equipment ready before beginning, and follow all of the steps in a section in the order they are presented.

Required Test Equipment

- ○ Digital DC Voltmeter (high-Z, >1 M ohm/V)
- ○ DC Ammeter
- ○ AC Voltmeter
- ○ RF Voltmeter
- ○ RF Standard Signal Generator w/calibrated output and dB scale, 0 dBμ = 0.5μV
- ○ AF Signal Generator with calibrated output
- ○ AF Voltmeter
- ○ Frequency Counter
- ○ 50-ohm Dummy Load (150 - 250 watts)
- ○ 16.6-ohm Dummy Load (150 watts)
- ○ In-Line Wattmeter (150 - 250 watts, 50-ohm)
- ○ RF Attenuator (150 watts, 40-dB) or Coupler

Alignment

Alignment Preparation & Precautions

A 50-ohm dummy load and in-line wattmeter must be connected to the antenna jack in all procedures that call for transmission, except where specified otherwise. Correct alignment is not possible with an antenna.

Except where specified otherwise, the transceiver should be tuned to 14.200 MHz,

USB mode, and these controls set as indicated:

○ SQL & VOL fully ccw (minimum)

○ CLARIFIER to 12 o'clock

After completing one step, read the following step to determine whether the same test equipment will be required. If not, remove the test equipment (except the dummy load and wattmeter, if connected) before proceeding.

Correct alignment requires that the ambient temperature be the same as that of the transceiver and test equipment, and that this temperature be held constant between 20

and 30 ºC (68 - 86 ºF). If the transceiver is brought into the shop from hot or cold air it

should be allowed some time for thermal equalization with the environment before alignment.

Alignments must only be made with oscillator shields and circuit boards firmly affixed in place. Only one extender board should be installed at a time for access to the board being aligned. Also, the test equipment must be thoroughly warmed up before beginning.

Alignment values assume a DC supply voltage of 13.5V DC.

Note: Signal levels in dB referred to in alignment are based on 0 dBµ = 0.5 µV.

Local Unit

Refer to the Local Unit Alignment Diagram on page 2-11. To prevent PLL unlock from interfering with the Local Unit alignment process, connect TP2004 to ground. Remember to disconnect TP2004 when finished with the alignment!

Reference Oscillator

❒ Connect the frequency counter to JP2001, and the voltmeter to TP2005.

❒ If the counter frequency differs by more than 3 Hz from 5.242880 MHz, adjust the TCXO-4 trimmer (if the TCXO is installed) or TC2701.

❒ Confirm a level of at least 900 mVrms on the RF voltmeter.

DDS 1 Check

❒ Tune the transceiver to 7.045.1 MHz, and select LSB mode.

❒ Connect the voltmeter to Q2036, pin 2, and confirm that the RF voltmeter indicates at least 110 mVrms.

DDS 2 Check

❒ Tune the transceiver to 7.045.1 MHz, and select LSB mode.

❒ Connect the RF voltmeter to Q2044, pin 2, and confirm an indication of at least 65 mVrms.

PLL BPF

❒ Connect the RF voltmeter to TP2001.

❒ Tune the transceiver to 7.005.6 MHz, and select LSB mode.

❒ Adjust T2001, T2002 and T2003 alternately several times for peak indicated RF voltage (at least 190 mVrms).

Carrier Level Adjust & Frequency Check

❒ Connect RF voltmeter to TP2015.

❒ Alternately adjust T2004 and T2005 several times for peak indicated RF voltage (at least 320 mVrms).

❒ Replace the voltmeter with a frequency counter.

❒ Select the indicated mode and frequency, according to the following table. Press the PTT-button to transmit.

Frequency	Mode
8.213.50 MHz	J3E (LSB)
8.216.50 MHz	J3E (USB)
8.215.80 MHz	A1A
8.215.80 MHz	A3E
8.213.00 MHz	J2B (LSB)
8.217.00 MHz	J2B (USB)

❒ Confirm that the carrier frequency is within ± 20 Hz of the displayed counter frequency.

PLL Main Loop VCO

❒ Connect the DC voltmeter to TP2013, then adjust and check the VCO voltage according to Table 1 as shown below.

Table 1. VCO Voltage Alignment

Tune to:	Adjust:	for indicated voltage of:
30.000.0 MHz	L2027	7.9 to 8.1 V
21.500.0 MHz	confirm	2.0 to 3.0 V
21.499.9 MHz	L2019	7.9 to 8.1 V
14.500.0 MHz	confirm	2.0 to 3.0 V
14.499.9 MHz	L2017	7.9 to 8.1 V
7.500.0 MHz	confirm	2.0 to 3.0 V
7.499.9 MHz	L2011	7.9 to 8.1 V
0.100.0 MHz	confirm	2.0 to 3.0 V

❒ Tune the transceiver to 30.000.0 MHz, USB mode, connect the voltmeter to L2005, and confirm a level of more than 60 mVrms.

1st L.O. Output Level Check

❒ Connect the RF voltmeter to TP2014.

❒ Tune the transceiver to 30.000.0 MHz, and select USB mode. Confirm a level of at least 600 mVrms.

Receiver Circuits

Refer to the Main Unit Alignment Diagram on page 2-12 for location of components.

IF Interstage Transformers (1)

(coarse alignment - Rx Carrier Balance)

❒ Connect the RF signal generator to the ANT jack, and an AF voltmeter with speaker to the EXT-SPKR jack.

❒ Set VR1003 & IF SHIFT to the 12 o'clock position, then set VR1004 and VR1007 fully clockwise. Inject a +100 dB signal at 14.200.0 MHz, then adjust transformers, T1001 to T1008 and T1010 to T1012 in succession several times for peak indication on the voltmeter.

❒ Reduce the SG output level for an S-meter indication of 3 to 5-meter, then adjust VR1006 for peak AF output or max. 3-meter indication.

IF Interstage Alignment

❒ Inject a +0 dBμ Signal at 14.200.0 MHz. Connect the AF voltmeter across an 4-ohm load to the EXT-SPKR jack on the rear panel.

❒ Preset VR1004 fully clockwise, and adjust transformers T1001 to T1008 and T1010 to T1012 in succession several times for peak AF output or S-meter indication (adjust the SG

level as necessary to keep the meter approximately mid-scale).

1st Mixer Balance

❒ Preset VR1003 fully clockwise, then, in LSB mode, tune to the internal heterodyne around 15.310 MHz, and adjust VR1003 alternately several times for a null in AF output.

IF Gain

❒ Inject a +8 dBμ signal at 14.200.0 MHz to the antenna jack and adjust VR1004 for an S-l meter deflection.

Squelch Threshold

❒ In the USB mode, with no signal at the antenna jack, set the SQL control to the l0 o'clock position, and adjust VR1005 so that the squelch just closes.

NB

❒ Inject a +20 dBμ signal at 14.200.0 MHz, then connect a voltmeter to TP1001. Press the NB key, then adjust T1022 and T1023 alternately several times for a minimum indication on the DC voltmeter.

Cellcall Tone Decord

❒ In the USB mode, with no signal at the antenna jack, connect a Frequency Counter to the VR1022 center pin.

❒ Adjust VR1022 on the Main Unit for 1850 Hz ± 10 Hz.

Transmitter

Connect the 50-ohm dummy load to the antenna jack for all procedures. Refer to the Main Unit Alignment Diagram on page 2-12 for location of components.

PA Unit Idling Current

❒ Connect a DC Ammeter to TP5001(-) and TP5002(+), and select USB mode.

❒ Key the transceiver and adjust VR5001 for 400 mA ± 50 mA.

Transmitter IF Interstage Transformers (2)

❒ Connect an in-line wattmeter and 50-ohm RF dummy load to the ANT jack.

❒ Tune to 14.200.0 MHz, and select the USB mode. Key the transceiver and adjust transformers, T1016 to T1021 several times for peak indication on the wattmeter (approx. 100 W).

CM Coupler Balance

❒ With the 50-ohm dummy load connected to the antenna jack, tune the transceiver to 14.200.0 MHz, and select the USB mode. Connect the DC voltmeter between pins 2 (-) and 3 (+) of J1022, key the transmitter and adjust TC4001 on the LPF Unit for minimum indication on the DC voltmeter.

RF Power Output Adjust

❒ With the in-line wattmeter and dummy load still connected, set the VR1010 fully counter clockwise .

❒ Select A1A mode and tune to 14.200.0 MHz. Key the transmitter and adjust VR1010 for 100 W ±5 W as indicated on the in-line wattmeter.

50W RF Power Output Adjust

❒ Set switch S1001 to the 50 W position, then set the RF PWR control fully clockwise .

❒ Select A1A mode and tune to 14.200.0 MHz.

Key the transmitter and adjust VR1016 for 50 W ±2.5 W as indicated on the in-line wattmeter.

Ext. Antenna Tuner RF Power Adjust

- ❒ Turn the transceiver off, then jumper TP1002 to chassis ground.
- ❒ Set switch S1001 to the "100 W" position, tune to 14.200.0 MHz, A1A mode.
- ❒ Turn the transceiver on, key the transmitter and adjust VR1011 for 10 W.

TX IF Gain

- ❒ Connect an AF signal generator and voltmeter to the MIC jack, and inject a 0.5 mV signal at 1kHz, and tune to 14.200.0 MHz, USB mode.
- ❒ Key the transmitter and adjust VR1007 for 50 W (increase AF SG level to 1 mVrms, if necessary, to permit deflection).

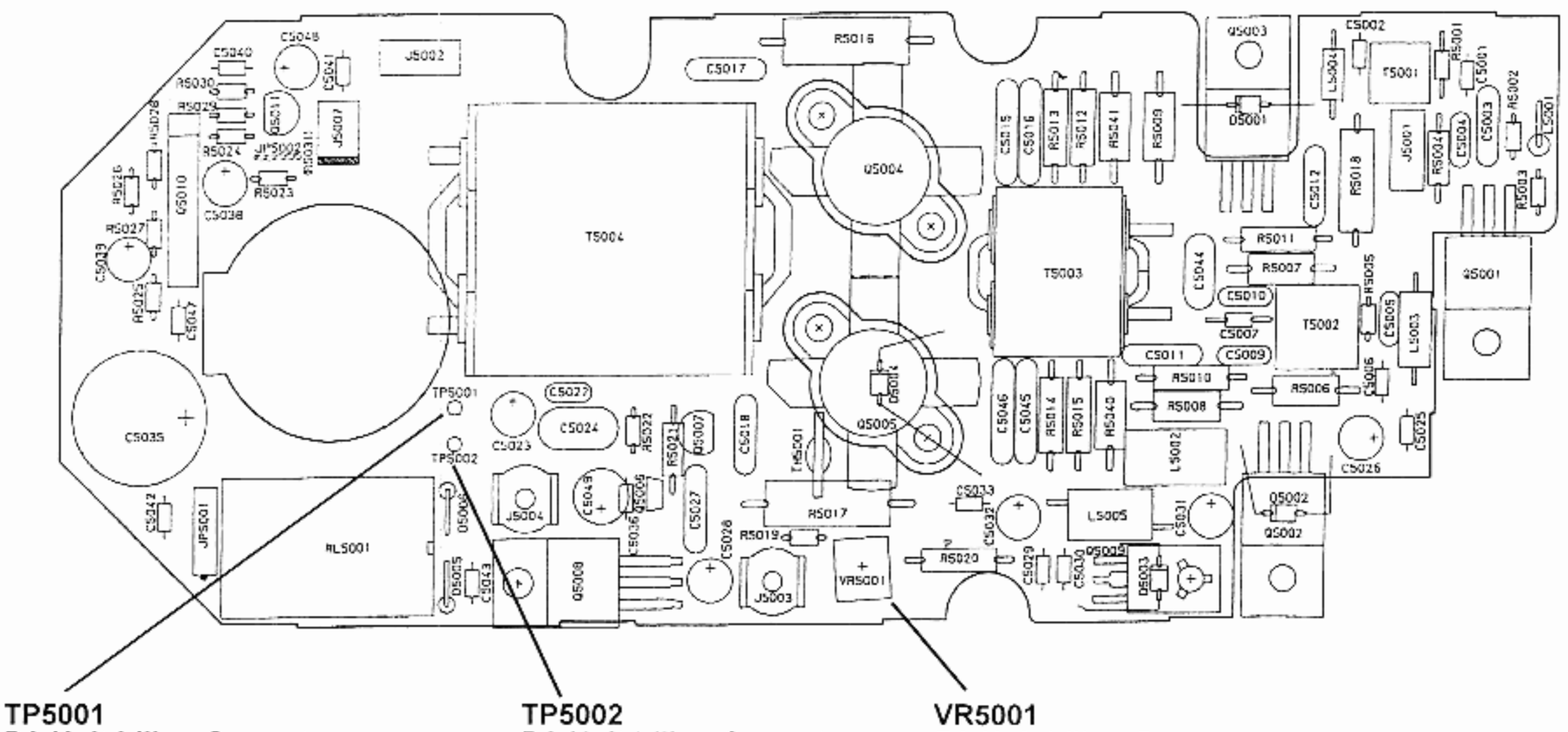
PO Meter Calibration

- ❒ With the in-line wattmeter and dummy load connected to the antenna jack, tune to 14.200.0 MHz, USB mode.
- ❒ Then adjust VR1019 so the PO meter also indicates 10 position.

S-Meter Reverse PO Indication

Reverse ALC (SWR Turndown)

- ❒ Connect the in-line wattmeter and a 16.6-ohm dummy load (or three 50-ohm loads in parallel) to the antenna jack.
- ❒ With the transceiver set to the A1A mode on 14.200.0 MHz, key the transmitter and adjust VR1017 for 40 W on the wattmeter.



PA Unit Alignment Diagram

Alignment

J3E Modulator Balance

❒ With the transceiver tuned to 14.200.0 MHz, USB mode, connect a 50-ohm dummy load to the antenna jack, and RF voltmeter to J1005.

❒ Key the transmitter, and adjust VR1008 for minimum indication on the RF voltmeter.

A3E Output Adjust

❒ Tune the transceiver to 14.200.0 MHz, AM mode, and connect the wattmeter and 50- ohm dummy load to the antenna jack.

❒ Next, key the transmitter and (with no modulation) adjust VR1020 for 25 W on the wattmeter.

Side-Tone & Beep Level

❒ Connect a AF voltmeter across a 4-ohm resistor or speaker connected to the EXT-SPKR jack.

❒ Adjust VR2001 on the Local Unit for 150 mV ±20 mV.

Alarm Tone Level

❒ Connect a AF voltmeter across a 4-olm resistor or speaker connected to the EXT-SPKR jack.

❒ Press the ALARM key, then Adjust VR2002 on the Local Unit for loud pitch and low pitch for an average of 150 mV ±20 mV.

Transmitter Carrier Point

Temporarily jumper TP2003 to TP2006.

Connect an AF signal generator to the MIC jack, and set for 2 mV injection at 1.5 kHz.

USB Carrier Point

❒ Set the transceiver to 6.000.0 MHz, USB mode.

❒ Press the FUNC key and 2/NB key to set the USB carrier point-setting mode. "CA ADJ" will be displayed.

❒ Then perform the following:

(a) Key the transmitter and inject 2 mV at 1.5 kHz from the AF generator to the MIC jack, and then adjust the injection level to just above the point where the ALC meter indication no longer rises.

(b) Adjust the AF generator gain control for 80 W on the wattmeter.

(c) Tune the AF generator to 300 Hz, and adjust the transceiver frequency so that 20 watts output is obtained.

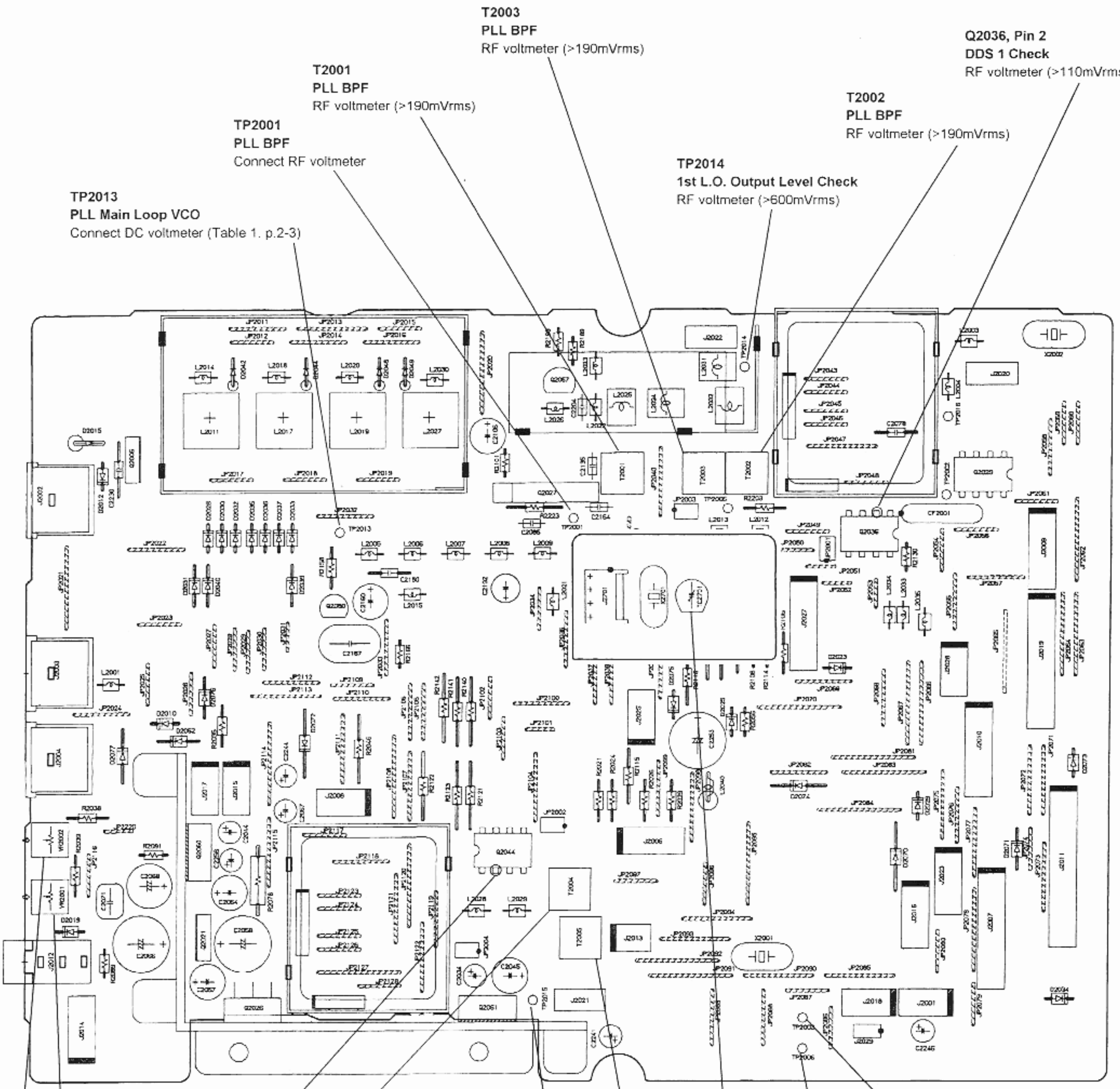
LSB Carrier Point

❒ Again press the 1/MODE key to set the LSB carrier point-setting mode.

❒ Repeat steps (a) to (c) to adjust the LSB carrier point.

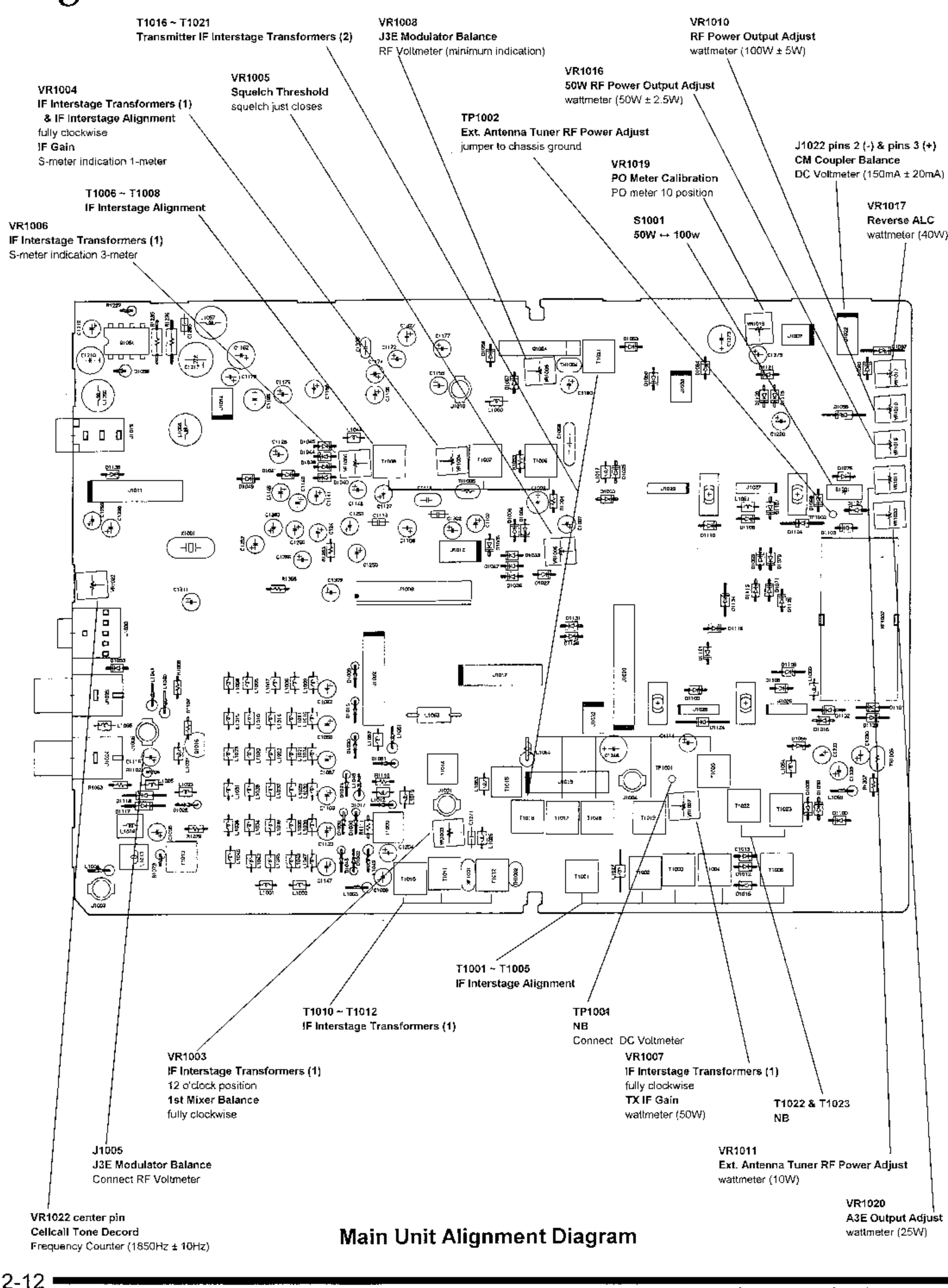
Press the 2/NB key to save the settings and return the display to normal.

Turn the transceiver off and *remove the jumper from TP2003 to TP2006!*



Local Unit Alignment Diagram

Alignment



Main Unit Alignment Diagram

Receive Signal Circuitry

RF Circuit

The RF signal from the ANT connector passes through the Relay RL4013 in the LPF-UNIT, and enters the MAIN-UNIT.

The signal just arrived at MAIN-UNIT is then led through the bandpass filter (BPF) via the 5th-order Butterworth low-pass filter whose cut-off frequency is 30 MHz.

The output from BPF has a frequency range of 50kHz to 30MHz, and the signal is divided into seven bands by switching diodes D1001 through D10043 according to the receiving frequencies before they are applied at the 1st Mixer circuit.

1st Mixer Circuit/1st IF Circuit

The 1st Mixer circuit comprises two FETs (FET Q1006 and 1012), and each of the source terminals receives the first local signal(47.105 to 77.055 MHz) from LOCAL UNIT.

The resulting output signal (the difference between the local and received signals) passes through monolithic crystal filter (MCF) XF1001(BW: [+/-] 7.5kHz) to obtain the 1st IF signal having a center frequency of 47.055 MHz. The signal is fed to the 2nd IF circuit after it has been amplified by FET Q1007.

2nd Mixer Circuit/2nd IF Circuit

The 2nd Mixer circuit comprises FET Q1011 (on MAIN-UNIT), and the gate terminal receives the second local signal(38.840 MHz) from LOCAL UNIT.

The resulting 2nd Mixer output signal is selected at the bandpass filter (BPF) that is composed of RF transformers (T1002 ,T1003 and T1004) and capacitor C1040, and becomes 2nd IF signal (8.215 MHz). The 2nd IF signal that has just passed the BPF enters the noise blanker gate (NB GATE) that is composed of diodes D1012, D1013 and D1016. It is then routed through crystal filter XF1002, according to the receiving mode (CW, SSB or AM), and sent to the 2nd IF circuit.

Noise Blanker Circuit

The signal sampled from the 2nd IF circuit is amplified by FET Q1055/Q1056 on MAIN-UNIT, and then detected (with twofold voltage amplitude) by diodes D1098 and D1099. This detected output controls the gain of above-mentioned FET by an average AGC voltage responsible for transistor Q1058 . Also, noise pulses contained in the detected output is amplified by the transistor Q1057 to be utilized for controlling NB GATE.

The 2nd IF signal (8.215 MHz) is amplified by FET Q1008 through Q1010, and then sent to the SSB demodulation circuit and the two circuits (AGC and AM demodulation by way of transistor Q1003 in the buffer amplifier).

AGC Circuit/AM Demodulator Circuit

The AGC circuit consists of detector diodes D1004, D1006 and Q1005 (on MAIN-UNIT).

Its output is fed to the FETs in the 1st and 2nd IF circuits in order to control the gains.

The AM demodulator circuit performs envelope detection of the 2nd IF circuit through D1005 and C1017. Its output is applied to Q1017.

SSB Demodulator Circuit

The 2nd IF signal is fed to the diodes D1038, D1040, D1044 and D1045 in the SSB demodulator (SSB EDT) circuit on MAIN-UNIT. Its output is demodulated into audio signal by

utilizing the carrier signal from DDS-2 UNIT, and then applied to transistor Q1017.

Audio Amplifier Circuit

The audio signal detected by SSB is fed to the ring detector that consists of the diodes D1038, D1040, D1044 and D1045, and applied to Q1017 for amplification, passed through a diode switch, and then applied to Q1017. The signal at Q1017 then passes through an active lowpass filter for higher frequency to be cut. The final output of 1.5 W (max.) is obtained at IC Q2026 with VR7201 for voice level adjustment on VR-A-UNIT.

An internal speaker (or an external speaker) can be connected.

AFSK Circuit

The AFSK (Audio Frequency-shift Keying) output is available at the terminal J1030 of the following signal path: the active lowpass filter with Q1014, the analog switch with Q1072, and the audio amplifier with Q1065.

Selective Call Circuit

The FSK signal for the selective call appears at Q1014 (the output stage of the active lowpass filter), then distributed to both IC Q1080 (a tone decoder) and IC Q1076 (FSK MODEM). At Q1080, a coming signal is checked to see if it is a SELCALL. If it is, the signal is directed to the J1011 (on MAIN UNIT), to J2007 (on LOCAL UNIT), and then to the pin 48 on CPU Q2009. As for the FSK MODEM signal, it is first converted into serial data at the MODEM, directed to J1011, to J2007, and then to the pin 47 on Q2009 in the same manner as with Q1080. The message "SELCALL" on LCD will blink and CPU Q2009 will provide a call signal at pin 79, if the serial data stored in CPU Q2009 has been identified as the data with the same ID as this station. The call signal is applied to an amplifier Q2064, a low-pass filter, and then a speaker at AF IC Q2026 (a power amplifier stage).

Encryption Circuit

Demodulated signal by the encryption process, derived from active LPF Q1014 , first enters amplifier Q1073 and is applied to pin 4 of the Encryption Unit (ENC-UNIT) to be decoded. The signal is then decoded into original voice signal(available at pin 5), passes through J1012 on MAIN UNIT, passes through VR-A-UNIT, and then input at AF IC Q2026 (on LOCAL UNIT).

Transmit Signal Circuitry

Microphone Amplifier Circuit

The voice signal arriving at the jack J7102 passes through the board connector JP7103, Q1027 (a low noise transistor on MAIN UNIT), IC Q1026-2 (an analog switch), Q1025/Q1028 (amplifier stages), and Q1024 (the Balanced Modulator circuit).

Balanced Modulator (BM)

The BM IC Q1024 receives both the carrier signal, selected according to transmitting mode (CW, SSB or AM) from LOCAL-UNIT, and modulation signals from the microphone circuit. The modulated signal (or 1st IF signal) from the BM IC is then applied at the crystal filter (on MAIN-UNIT).

ALC (Automatic Level Control) Circuit

The screwdriver control potentiometer VR1010 is adjusted and fixed so that the transmitter output of 100 W may be attained. The FWD (traveling-wave) voltage from LFP-UNIT is compared with the VR1010 at the operational amplifier Q1043-1 whose output is applied at the base of Q1042. The ALC output from Q1042 is input at the second gate of Q1023, and serves for maintaining a constant transmitter output.

Keying Circuit

The objective of this circuit is to generate the continuous wave (CW). The input signal from the KEY passes through Q1044 and Q1039. The transistor Q1039 causes both the base bias to Q1021 (TX RF amplifier) and gate bias to Q1020/Q1029 (the TX Mixer circuit) to change in order to get the CW. The resistors R1149/R1192 and capacitors C1176/C1322 are to limit bandwidth of the keyed waves.

1st IF Circuit/1st Mixer Circuit

The 1st IF signal (8.215 MHz) modulated in the BM is band-limited by the crystal filter XF1002 according to the selected mode (CW, SSB or AM), amplified by FET Q1023, and applied at FET Q1020/Q1029 (the 1st Mixer circuit). Gate 2 of FET Q1023 is fed by the ALC voltage to stabilize TX output.

The 2nd Mixer is fed by the local signal (38.840 MHz) from LOCAL-UNIT, and converts this local signal into the 2nd IF signal (47.055 MHz).

2nd IF Circuit/2nd Mixer Circuit

The 2nd IF signal is input at the 2nd Mixer circuit by way of a bandpass filter that consists of RF transformers T1016/T1017.

The 2nd Mixer circuit (DBM IC D1015), which comprises diodes, receives the local signal (48.855 MHz to 77.055 MHz) generated by the PLL Frequency Synthesizer, and converts this local signal into 1.8 MHz to 30 MHz.

TX Preamplifier Circuit

The TX output from the DBM IC is amplified by the wide bandwidth high-frequency transistor Q1021, passed through a BPF, amplified again by Q1016, and sent to the PA-UNIT by way of the J1006.

Power Amplifier Circuit

The output from the RF-UNIT is fed to the 100 W PA-UNIT via connector J5001. The input TX signal (1.8 MHz to 30 MHz) is fed to pre-driver, driver and the final stages (Q5001 through Q5005 for all stages). Its output is available at connector J5002, and sent to LPF-UNIT.

Lowpass Filter Circuit

The TX RF output from the power amplifier circuit is input at P4004, passes through the Chebyshev LPF network (1.8 MHz to 30 MHz, composed of the relays RL4001 through RL4012, coils L4001 through L4012, and capacitors with this network being divided into six bands), passes through CM coupler coil L4013 and ANT relay RL4013, and finally is delivered at ANT connector.

The CM coupler consists of coil L4013, trimmer TC4001, capacitor C4036, and checks the traveling and reflected waves by extracting a small portion of the output. The sampled TX RF is detected by diodes D4002 and D4003 as negative voltage to used in ALC (Automatic Level Control).

AFSK (Audio Frequency-shift Keying)

The AFSK signal from the terminal unit enters at J1030 on MAIN UNIT, passes through active LPF Q1081, is amplified by Q1028/Q1025, and becomes the modulated signal. The voice signal from the microphone is interrupted, because switching transistors Q1031/Q1071 cut off analog switch Q1026-2.

Selective Call Circuit

An ID code entered at the panel keyboard is dispatched from CPU IC Q2009 (with 46 pins, and located on LOCAL UNIT) on a serial data bus, routed through J2007 on LOCAL UNIT, routed through J1011 on MAIN UNIT, and input at pin 11 of FSK MODEM IC Q1076. The MODEM IC then converts this signal from CPU into two-tone FSK signals (mark = 1650 Hz, space = 1850 Hz). The FSK signal becomes a modulated signal, after it is routed through analog switch Q1026-1 and then amplified by Q1028/Q1025. On transmitting an ID signal for the selective call, voice signal from the microphone is interrupted by analog switch Q1026-2 (which is turned OFF under control of transistors Q1031/Q1071).

Encryption Circuit

Original voice signal to be processed by Encryption circuit is derived from the collection of MIC amplifier Q1027, amplified by Q1064, input at pin 2 of the ENC-UNIT for processing.

The signal just processed is available at pin 3 of ENC-UNIT, passes through analog switch Q1026-1, amplified by Q1028/Q1025, and then becomes a modulated signal. The original signal from Q1027 is interrupted by analog switch Q1026-2 (which is turned OFF under control of transistors Q1031/Q1071).

Alarm Circuit

Alarm signal for emergency communication is generated at pin 62 of CPU Q2009 on LOCAL UNIT, passes through active LPF Q2066 to attenuate harmonics, passes through both J2017 and J1012 (on MAIN UNIT), and is input at pin 1 (input from external signal) of FSK MODEM IC Q1076. In addition, this signal passes through a line drive amplifier inside the MODEM IC, and becomes a modulated alarm signal (available at pin 17 just as in the selective call FSK signal) to be transmitted. Voice signal from the microphone is interrupted on transmitting alarm signal. This inhibition against the voice signal also occurs when transmitting the selective call ID signal.

Alarm signal provided at Q2066 is adjusted for its level by VR2002, fed to AF IC Q2026, and connected to a speaker to have monitor sound.

PLL Frequency Synthesizer

Master Reference Oscillator Circuit

The master reference oscillator consists of crystal vibrator X2701, PLL IC2048, trimmer capacitor TC2701, capacitor C2701/C2702, etc., and has a frequency of 10.48567 MHz. If the option TCXO-4 is used, the oscillator output must be fed to pin 1 of PLL IC Q2048.

The output is supplied to Q2035 -1(divide-by-2 frequency divider) and DDS-1/DDS-2 via buffer amplifier Q2059.

Voltage Controlled Oscillator (VCO)

VCO covers the frequency range for the 1st local oscillation frequency (47.105 MHz to 77.055

MHz) by using VCO1 through VCO4 circuits in order to divide the range in four bands. The VCO consists of oscillator FET Q2034/Q2040/Q2046/Q2052, variable capacity diodes D2043/D2045/D2047/D2050, coils L2011/L2017/L2019/L2027, feedback capacitors, etc. The switching among the four circuits is performed by using switching transistors Q2039/Q2043/Q2051/Q2058 which are driven as follows:

Decode IC Q2020 receives the band data from CPU IC Q2009, and makes a selected switching transistor conduct the corresponding FET. The frequency of each VCO is controlled by control voltage (VCV) from the loop filter.

2nd Local Oscillator Circuit

The 38.84 MHz 2nd Local Oscillator Circuit is a Colpitts oscillator. Its output is fed to the TX and RX mixers (on MAIN-UNIT) via buffer amplifier Q2030, LPF, and connector J2020.

DDS-1/DDS-2 UNIT

DDS (Direct Digital Synthesizer) is composed of DDS IC Q2501/Q2601, the shift registers, selectors, phase accumulators, ROM, etc. A ROM inside the IC has information on a sine wave over a half cycle:

A half cycle sine wave is sliced to have phase addresses versus amplitude for each slice.

The ROM provides users with address vs. amplitude information on each slice.

The input signal (the 10.48576 MHz master reference signal) is utilized as the clock for this circuit. The frequency setting signal from CPU IC is input to the Phase Accumulator via shift registers and selectors. The Phase Accumulator accumulates input data in sync with the clock, and its output designates an address of the ROM. The ROM provides a digital output data that corresponds to the address given, and the digital output data is converted into an analog voltage after D/A conversion through ladder resistors RB2501/R2601, amplification by buffer amplifiers Q2502/Q2602, and generation of sine wave together with LPF have been performed. The DDS-1 has the frequency range of 432.600 to 514.520 kHz; DDS-2,1133.880 to 1136380 kHz (center freq. = 1135.380 kHz).

PLL Circuit

PLL IC Q2048 consists of prescaler, programmable and reference dividers, phase comparator, oscillator, shift register, etc. The 10.48576 MHz master reference signal is input to the phase comparator as a 81.92 kHz comparison reference frequency, after the master signal has been divided by 128 in the PLL IC reference divider. The resultant output of the ceramic filter CF2001 has a frequency range of 5.67548 to 5.75740 MHz, after the DDS-1 UNIT signal (432.60 to 514.52 kHz) and the 1/2 divider Q2035-1 (5.24288 MHz) have been mixed at the mixer Q2036 by addition. Furthermore, the ceramic filter output is mixed with 2nd local signal (38.84 MHz) at mixer Q2029 (the frequency range by this addition : 44.51548 to 44.59740 MHz), passes through BPF T2002/T2003, and is amplified by transistor Q2032. The output of transistor Q2032 is then mixed at mixer Q2027 (the frequency range by this subtraction : 2.58952 to 32.52224 MHz) with the VCO signal (47.105 to77.055 MHz), passes through both LPF/buffer Q2041, and input at PIN 13 of PLL IC FIN. The output at PIN 13 of PLL IC FIN is then fed to the Phase Comparator, after it has been transformed into an input comparison frequency determined by the program-

mable divider and the frequency setting of CPU IC Q2009. Phase Comparator provides a pulse proportional to the phase difference between the input comparison frequency and the 81.92 kHz comparison reference frequency. This pulse is integrated by the loop filter to get a control voltage (VCV) which controls oscillation frequency of the VCO.

The CPU IC notify PLL IC that the following information should be converted into parallel data in PLL IC:

The frequencies and divider ratios (at the power ON time, the TX/RX switching time, and frequency setting change time) should be sent to the shift registers and latches as serial data inside the PLL IC.

This serial data is converted into the parallel data to be used as the "comparison dividing ratio" and "reference dividing ratio".

The transmission prohibition signal is sent to CPU at unlock time by inverting the UL signal with transistor Q2053 depending on the results obtained at the Phase Comparator.

Loop Filter

Loop filter consists of active filter (made up of FET Q2049, transistor Q2050, R2157/R2166, C2167, etc.) and 1st order lowpass filter. The loop filter is to get a control voltage (VCV) proportional to the phase difference at the Phase Comparator in order to control oscillation frequency of the VCO. The VCV is obtained by integrating the pulses from the Phase Comparator.

1st Local Oscillator Signal

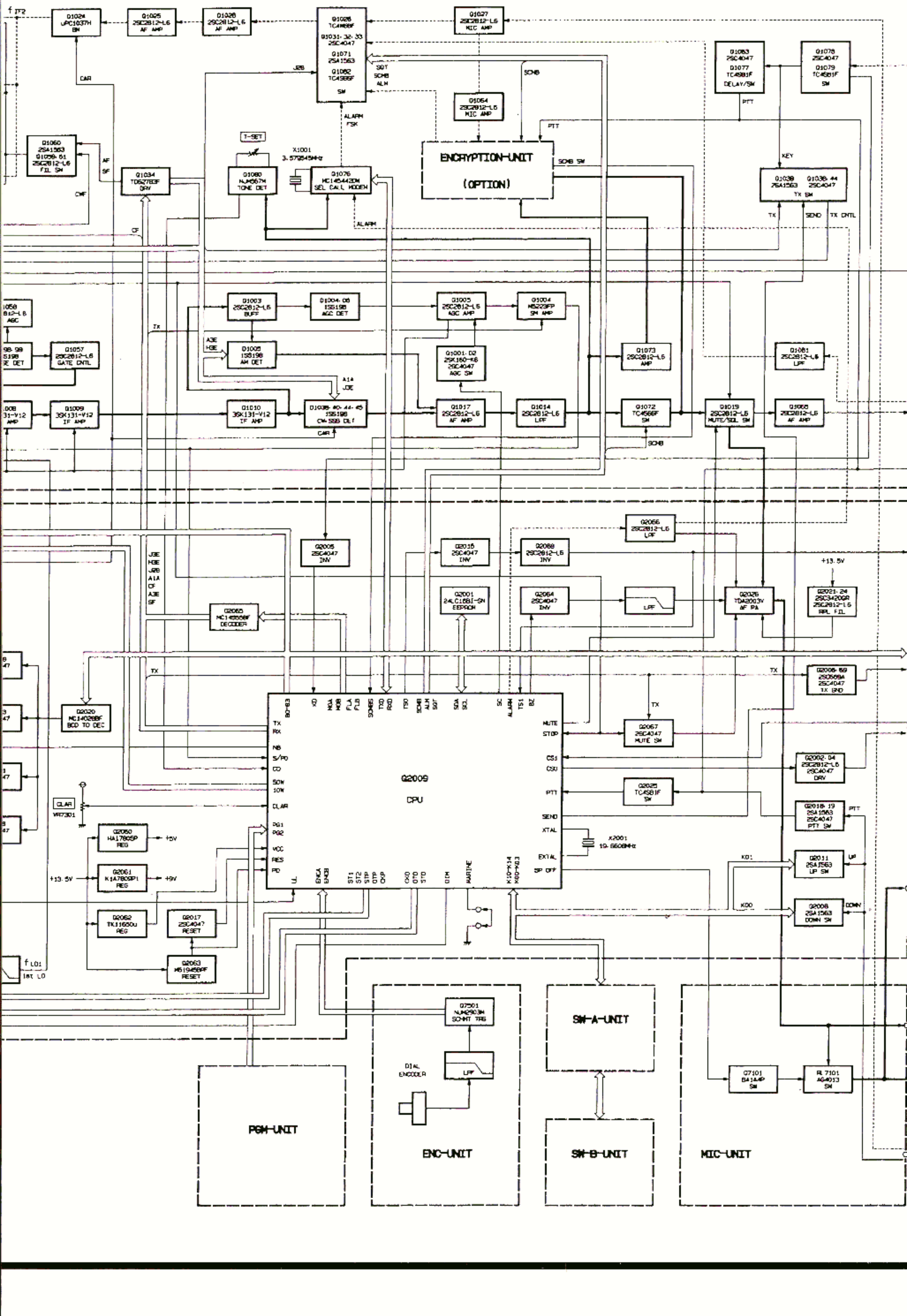
The oscillation frequency of the VCO is amplified at FET Q2038, buffer-amplified at Q2056, amplified by transistor Q2057, passes through LPF/HPF, and finally supplied to the TX and RX frequency mixers (on MAIN-UNIT) via connector J2022.

Carrier Oscillation Signal Circuit

The carrier oscillation signal is obtained by the following process:

The DDS-2-UNIT output (1133.88 to 1136.38 kHz) and the 1/2 freq. divider Q2035-1 output (5.24288 MHz) are mixed at mixer Q2044 to obtain a differential signal between 4.10900 MHz and 4.10650 MHz. Filtered by a LPF. Amplified by transistor Q2054, and passes through BPF T2004/T2005. Amplified by twofold freq. multiplier. Buffer-amplified at Q2055. The carrier oscillation signal of 8.21300 to 8.21800 MHz (cf = 8.215 MHz) is supplied to Balanced Modulator (BM)(on MAIN UNIT) and the demodulator(SSB DET) via connector J2021.

Block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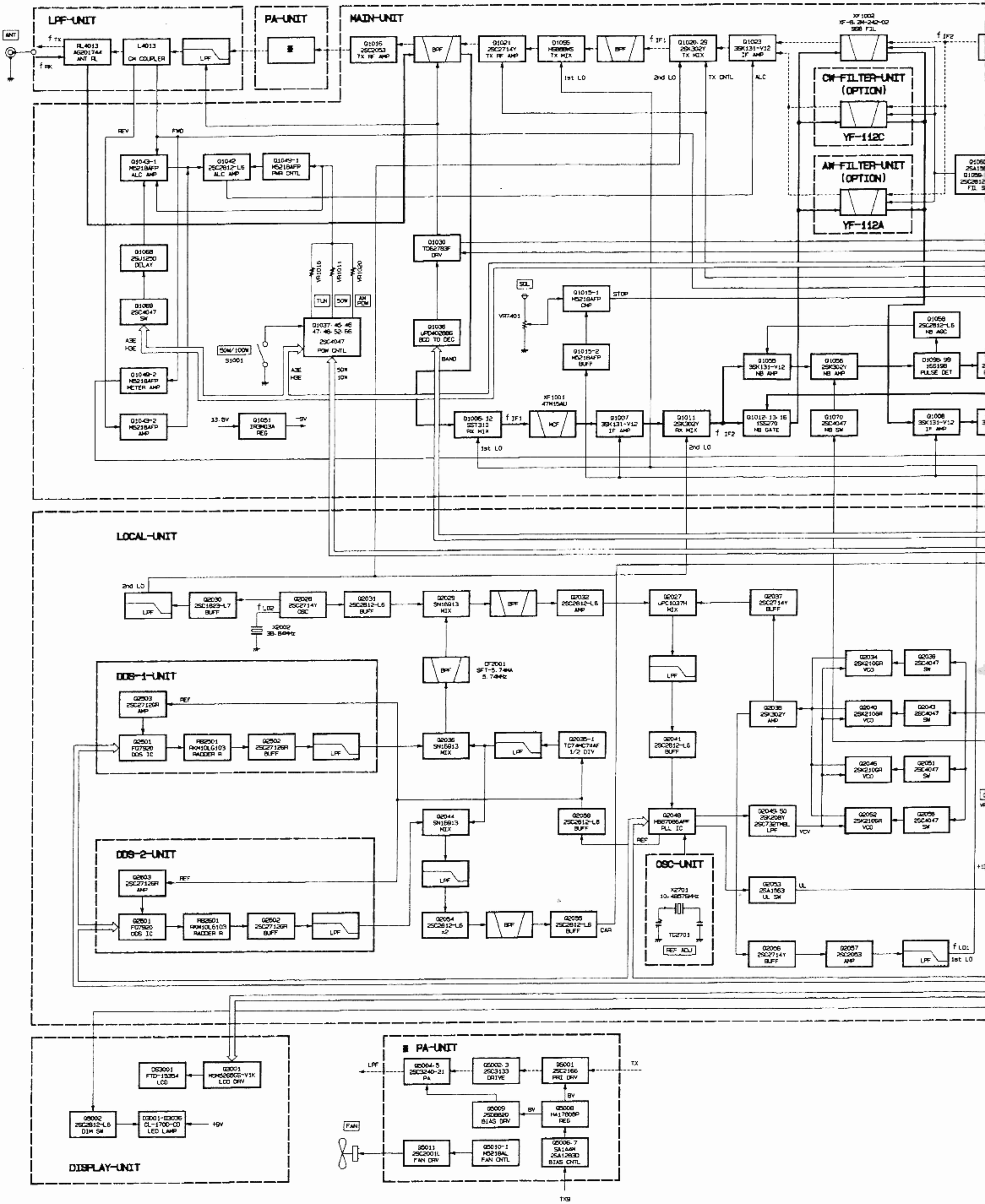
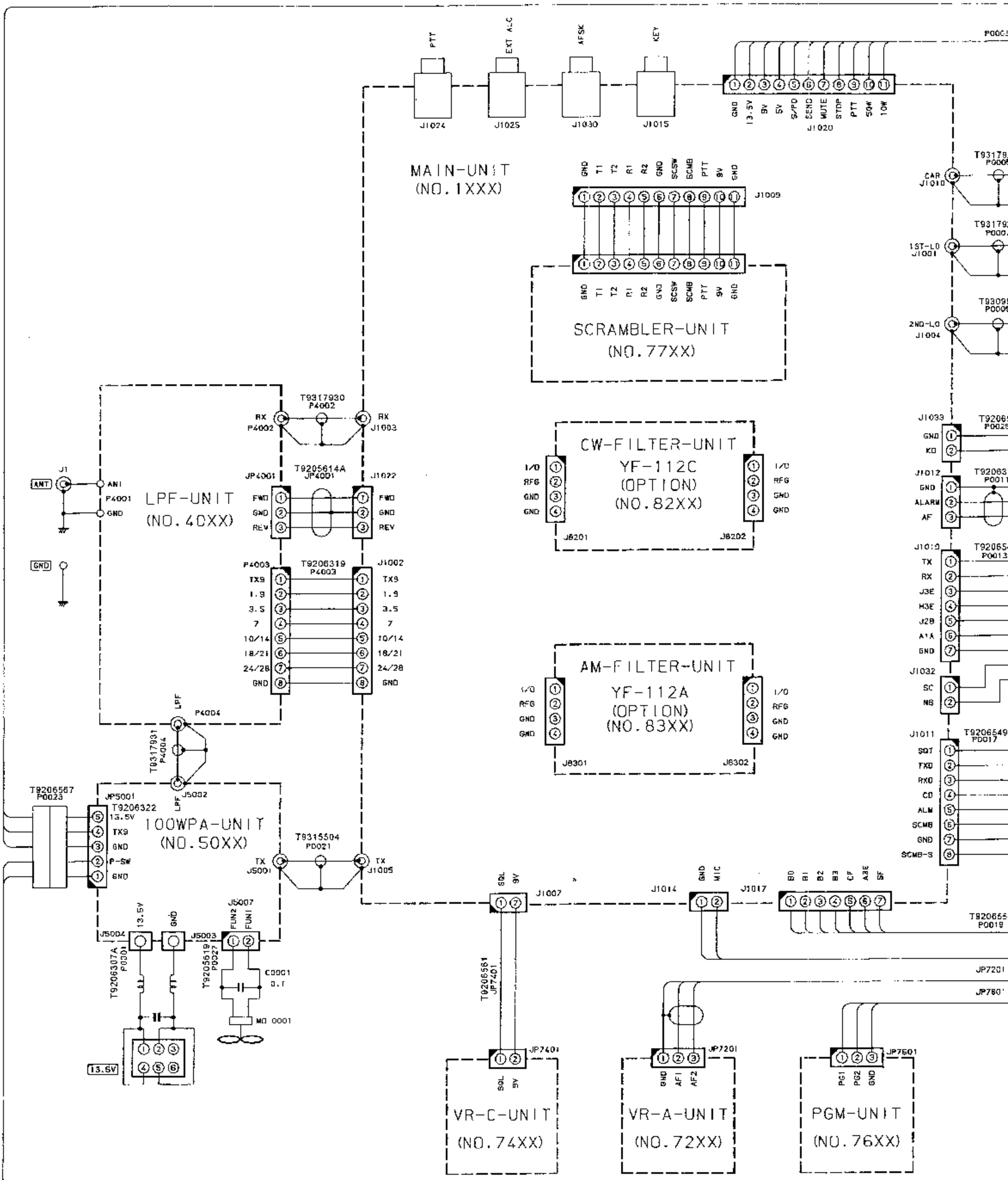
(OPTION)
CPU
PGM-UNIT
ENC-UNIT
SW-A-UNIT
SW-B-UNIT
MIC-UNIT


LPF-UNIT
PA-UNIT
MAIN-UNIT
ANT
RL4013
L4013
CH COUPLER
LPF
Q1016 2SC2053 TX RF AMP
BPF
Q1021 2SC2714Y TX RF AMP
Q1055 HSB88WS TX MIX
Q1020-29 2SK302Y TX MIX
Q1023 3SK131-V12 IF AMP
XF1002 XF-8.2M-242-02 SSB FIL
CW-FILTER-UNIT (OPTION)
YF-112C
AM-FILTER-UNIT (OPTION)
YF-112A
1st LO
2nd LO
TX CNTL
ALC
REV
FWD
Q1043-1 M5218AFP ALC AMP
Q1042 2SC2812-L6 ALC AMP
Q1049-1 M5218AFP PWR CNTL
Q1030 TD62783F DRV
Q1068 2SJ1250 DELAY
Q1069 2SC4047 SW
Q1049-2 M5218AFP METER AMP
Q1043-2 M5218AFP AMP
13.5V
Q1051 IR3M03A REG
-9V
VR1018
VR1019
VR1020
TUN
SQN
AM PON
Q1037-45-46 47-48-52-56 2SC4047 PON CNTL
S1001
50M/100M
ASE
HSE
Q1036 UPD4029BG BCD TO DEC
BAND
SQL
VR7401
Q1015-1 M5218AFP DNP
Q1015-2 M5218AFP BUFF
STOP
Q1006-12 SST310 RX MIX
f IF1
XF1001 47M15AU
MCF
Q1007 3SK131-V12 IF AMP
Q1011 2SK302Y Rx MIX
f IF2
Q1012-13-16 1SS270 NB GATE
Q1070 2SC4047 NB SW
Q1055 3SK131-V12 NB AMP
Q1056 2SK302Y NB AMP
Q1058 2SC2812-L6 NB AGC
Q1059-99 1SS198 PULSE DET
Q1008 3SK131-V12 IF AMP
LOCAL-UNIT
2nd LO
Q2030 2SC1623-L7 BUFF
Q2028 2SC2714Y OSC
f LO2
X2002 38.840MHz
Q2031 2SC2812-L6 BUFF
Q2029 SN16913 MIX
BPF
Q2032 2SC2812-L6 AMP
Q2027 UPC1037H MIX
Q2037 2SC2714Y BUFF
DF2001 SFT-5.74MA 5.74MHz
DDS-1-UNIT
Q2503 2SC2712GR AMP
REF
Q2501 FQ7520 DDS IC
RB2501 RKM10LG103 RADDER R
Q2502 2SC2712GR BUFF
LPF
Q2036 SN16913 MIX
Q2035-1 TC74HC74AF 1/2 DIV
Q2041 2SC2812-L6 BUFF
Q2038 2SK302Y AMP
Q2034 2SK210GR VCO
Q2039 2SC4047 SW
Q2040 2SK210GR VCO
Q2043 2SC4047 SW
Q2046 2SK210GR VCO
Q2051 2SC4047 SW
DDS-2-UNIT
Q2603 2SC2712GR AMP
Q2601 FQ7520 DDS IC
RB2601 RKM10LG103 RADDER R
Q2602 2SC2712GR BUFF
Q2044 SN16913 MIX
Q2054 2SC2812-L6 x2
Q2055 2SC2812-L6 BUFF
Q2059 2SC2812-L6 BUFF
CAR
Q2048 M66786AFP PLL IC
OSC-UNIT
X2701 10.4857MHz
TC2701
REF ADJ
Q2045-50 2SK208Y 2SC3278MBL LPF
VCV
Q2052 2SK210GR VCO
Q2058 2SC4047 SW
Q2053 2SA1563 UL SW
UL
Q2006 2SC2714Y BUFF
Q2057 2SC2053 AMP
LPF
f LO1
1st LO
DISPLAY-UNIT
DS3001 FTD-13S54 LCD
Q3001 M24S256S-V1K LCD DRV
Q3002 2SC2812-L6 DIM SW
D3001-D3036 CL-170D-CO LED LAMP
+9V
PA-UNIT
Q5004-5 2SC3240-21 PA
Q5002-3 2SC3133 DRIVE
Q5001 2SC2166 PRI DRV
Q5009 2SD820 BIAS DRV
Q5008 M178M08P REG
8V
Q5011 2SC2001L FAN DRV
Q5010-1 M5218AL FAN CNTL
Q5006-7 SA1489 2SA1283D BIAS CNTL
FAN
TX9

Interconnection Diagram



P0003 T9206299

J2011: 1 GND, 2 13.5V, 3 9V, 4 5V, 5 S/PD, 6 SEND, 7 MLTE, 8 STOP, 9 PTT, 10 SDW, 11 10W

J2008: 1 GND, 2 TXD, 3 13.5V

J2002 BAND DATA

J2003 FC-803

J2004 CLONE

J2012 EXT SPKR

LOCAL UNIT
(NO.2XXX)

SP0001

MIC-UNIT
(NO.71XX)

J2025 — T9206556 JP7101 — JP7101
SP OFF 1 — 1 SP OFF
GND 2 — 2 GND
13.5V 3 — 3 13.5V

J2014 — T9206557 JP7102 — JP7102
GND 1 — 1 GND
AFOUT 2 — 2 AF OUT
EXT SP 3 — 3 EXT SP
INT SP 4 — 4 INT SP

J2009 — T9206558 JP7103 — JP7103
GND 1 — 1 GND
DOWN 2 — 2 DOWN
UP 3 — 3 UP
PTT 4 — 4 PTT
5V 5 — 5 5V
6 — 6 MICGND
MIC 7 — 7 MIC

T9317928 P0005 — CAR J2021

T9317928 P0007 — 1ST-LO J2022

T9309503 P0009 — 2ND-LO J2020

OSC-UNIT
(NO.27XX)

TCXO-UNIT
TCXO-4(OPTION)
(NO.28XX)

GND XI XO 9V

T9206551 P0025 — J2013: 1 GND, 2 KD

T9206310 P0011 — J2017: 1 GND, 2 ALARM, 3 AF

T9206548 P0013 — J2019: 1 TX, 2 RX, 3 J3E, 4 H3E, 5 J2B, 6 A1A, 7 GND, 8 SC, 9 NB

T9206549 P0017 — J2007: 1 SQT, 2 TXD, 3 RXD, 4 CD, 5 ALM, 6 SCNB, 7 GND, 8 SCNB-S

REF GND GND OUT — J2502 — DDS-1-UNIT (NO.25XX) — J2501: 1 5V, 2 ST2, 3 GND, 4 DTP, 5 CKP

REF GND GND OUT — J2602 — DDS-2-UNIT (NO.26XX) — J2601: 1 5V, 2 ST2, 3 GND, 4 DTP, 5 CKP

J2023 — T9206562 JP7501 — JP7501
GND 1 — 1 GND
ENC A 2 — 2 ENC A
ENC B 3 — 3 ENC B
5V 4 — 4 5V

ENC-UNIT
(NO.75XX)

J2004 — T9206560 JP7301 — JP7301
AGND 1 — 1 AGND
CLAR 2 — 2 CLAR
REF 3 — 3 REF

VR-B-UNIT
(NO.73XX)

J2028: CF, A3E, BF
J2005: B0, B1, B2, B3
J2015: GND, MF1, MF2
J2018: HG1, HG2, GND
J2010: K10, K11, K12, K13, K14, GND
J2016: K00, K01, K02, K03
J2027: DIM, 9V, DTO, CKO, STO, GND

T9206550 P0019

JP7201 T9206559

JP7601 T9206563

JP7002 T9206554

T9206553 JP7001

T9206555 JP7003

T9206552 JP3001

K10 GND K02 K03 — JP7051 — J7051: 1 GND, 2 P-SW — SW-B-UNIT (NO.705X)

K10 GND K02 K03 — JP7002

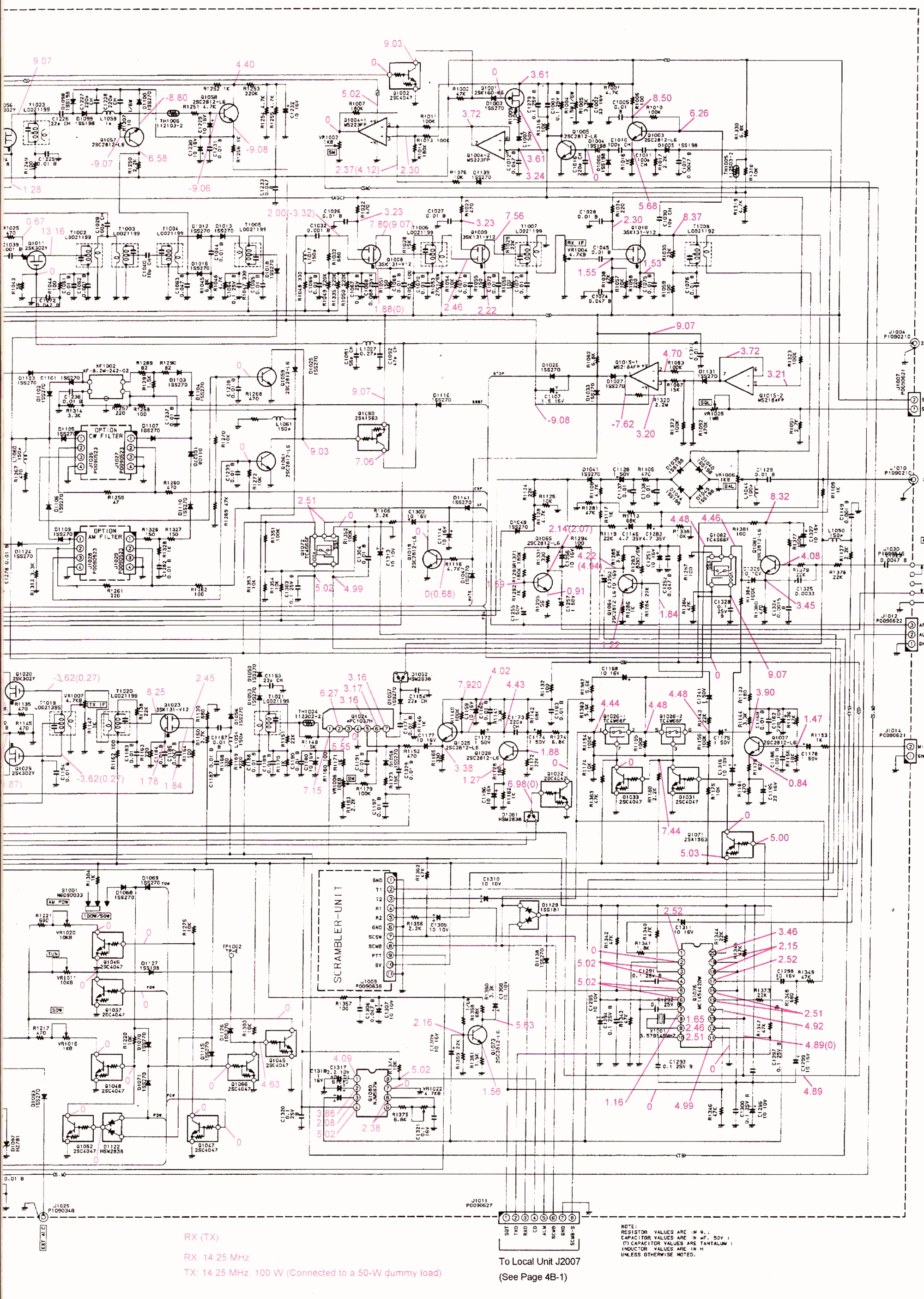
K10 K11 K12 K13 K14 GND — JP7001

K00 K01 K02 K03 — JP7003

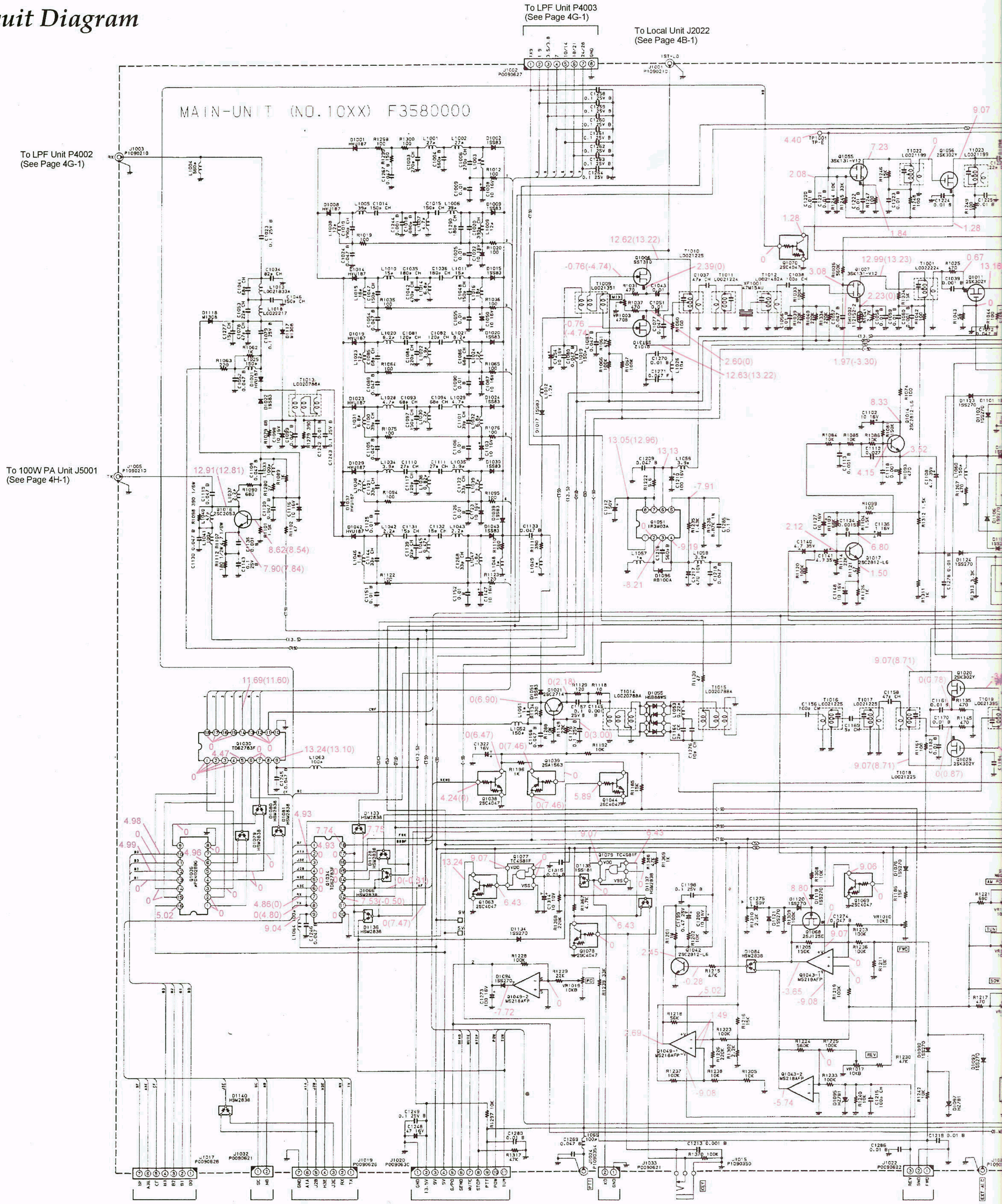
SW-A UNIT
(NO.70XX)

DIM 9V DTO CKO STO GND — JP3001

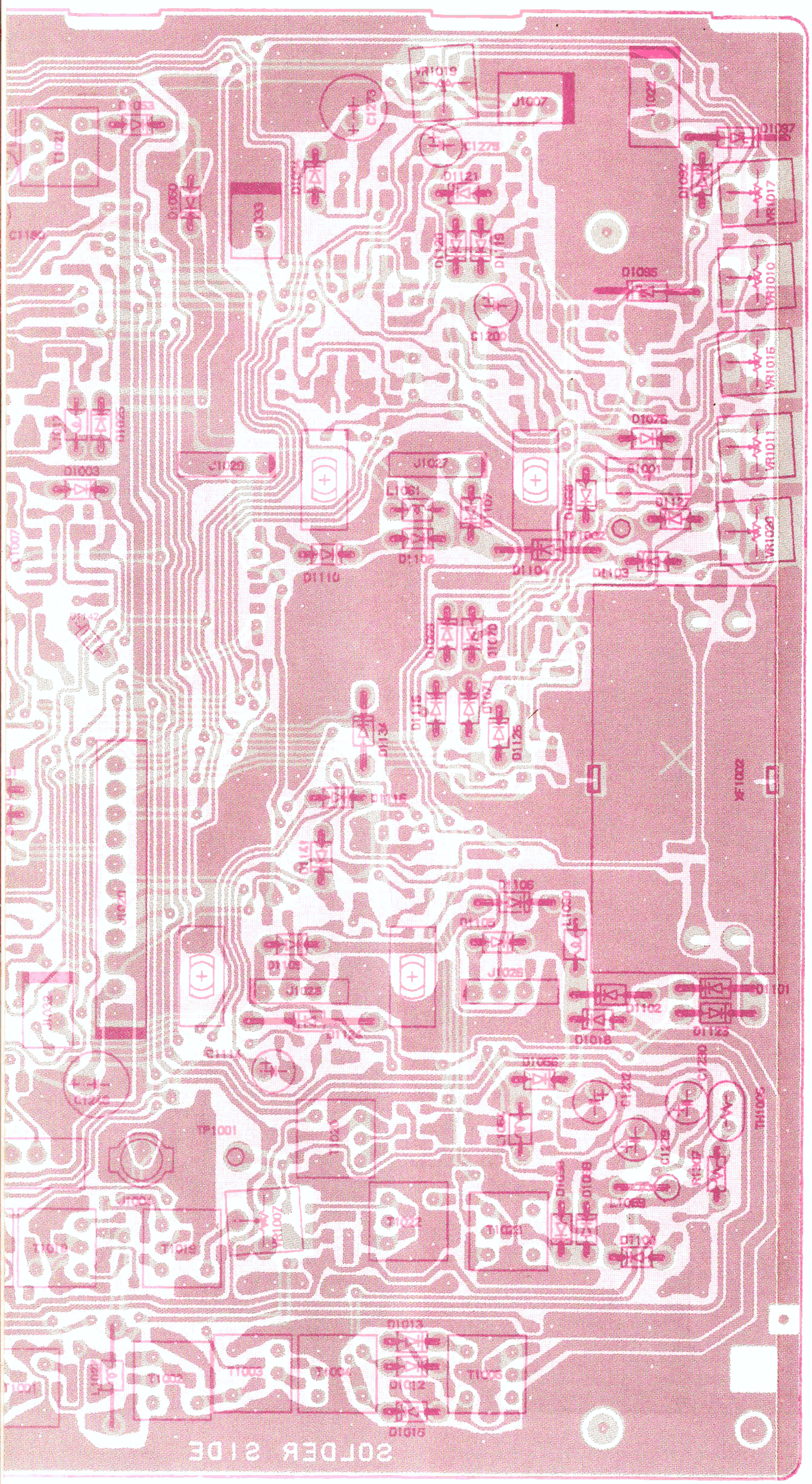
DISPLAY-UNIT
(NO.30XX)


RX (TX)
RX: 14.25 MHz
TX: 14.25 MHz, 100 W (Connected to a 50-W dummy load)
To Local Unit J2020 (See Page 4B-1)
To VR-C Unit JP7401 (See Page 4N-1)
To Local Unit J2021 (See Page 4B-1)
To Local Unit J2017 (See Page 4B-1)
To MIC Unit JP7103 (See Page 4K-1)
To Local Unit J2007 (See Page 4B-1)
NOTE:
RESISTOR VALUES ARE IN Ω.;
CAPACITOR VALUES ARE IN μF. 50V ;
(T) CAPACITOR VALUES ARE TANTALUM ;
INDUCTOR VALUES ARE IN H
UNLESS OTHERWISE NOTED.

Circuit Diagram



E F

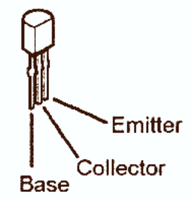


J1007: SQL, 9V

J1022: FWD, GND, REV

J1033: GND, K0

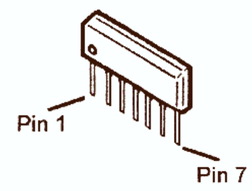
2SC2053 (Q1016)



J1029: GND, GND, RFG, I/O

J1027: GND, GND, RFG, I/O

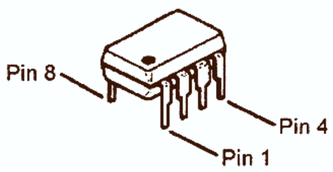
μPC1037H (Q1024)



J1012: AF, ALARM, GND

J1009: GND, T1, T2, R1, R2, GND, SCSW, SCMB, PTT, 9V, GND

IR3M03A (Q1051)



J1032: SC, NB

J1028: I/O, RFG, GND, GND

J1026: I/O, RFG, GND, GND

J1020: 10W, 50W, PTT, STOP, MUTE, SENO, S/PO, 5V, 9V, 13.5V, GND

J1017: B0, B1, B2, B3, CF, A3E, SF

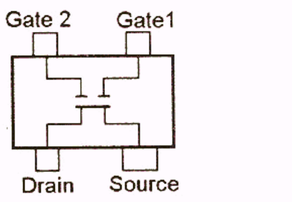
J1019: TX, RX, J3E, H3E, J2B, A1A, GND

J1002: TX9, 1.9, 3.5, 7, 10/14, 18//21, 24/28, GND

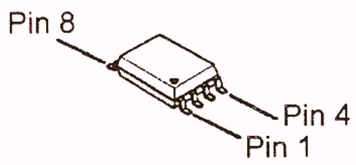
Component Side

Parts Layout

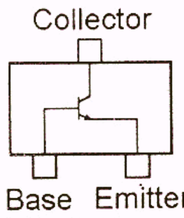
Main Unit



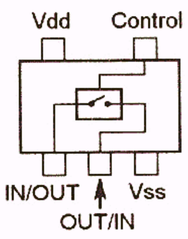
3SK131 (V12)
(Q1007,1008,1009,1010
1023,1055)



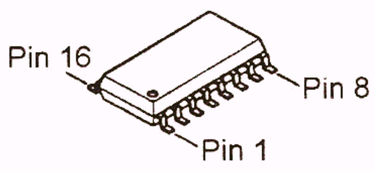
M5223FP
(Q1004)
M5218AFP
(Q1015,1043,1049)
NJM567M
(Q1080)



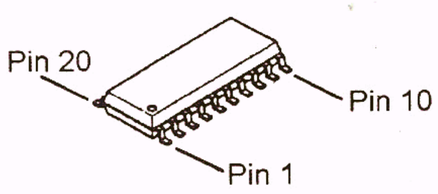
2SC2812 (L6)
(Q1003,1005,1014,1017
1019,1025,1027,1028
1042,1057,1058,1059
1061,1064,1065,1073
1081)
2SC2714Y (QY)
(Q1021)



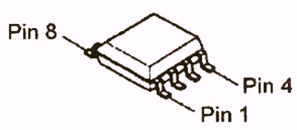
TC4S66F (C9)
(Q1072,101082)



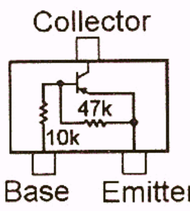
UPD4028BG
(Q1036)



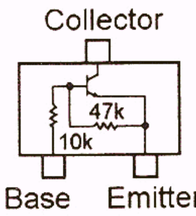
MC145442DWEL
(Q1076)



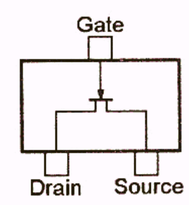
TC4W66F
(Q1026)



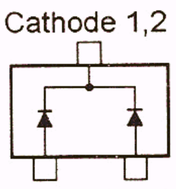
2SA1563 (RL)
(Q1039,1060,1071)



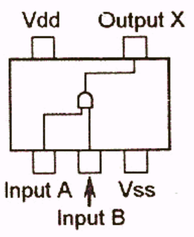
2SC4047 (ZY)
(Q1002,1031,1032,1033
1037,1038,1044,1045
1046,1047,1048,1052
1063,1066,1069,1070
1078)



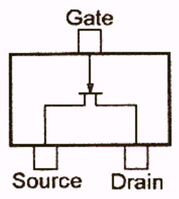
SST310 (Z0)
(Q1006,1012)



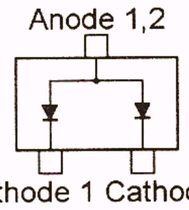
HSM2838 (A6)
(D1028,1052,1061,1066
1079,1080,1081,1084
1122,1128,1133,1136
1137,1140)



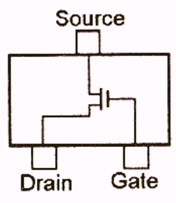
TC4S81F ()
(Q1077,1079)



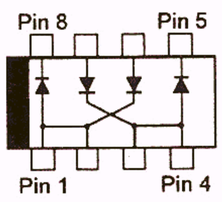
2SK160 (K6)
(Q1001)



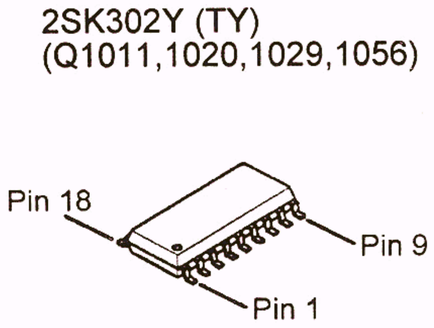
1SS181 (A3)
(D1129,1135)



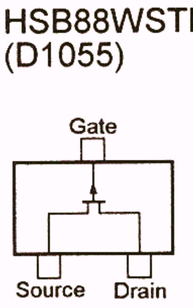
2SK302Y (TY)
(Q1011,1020,1029,1056)



HSB88WSTR
(D1055)

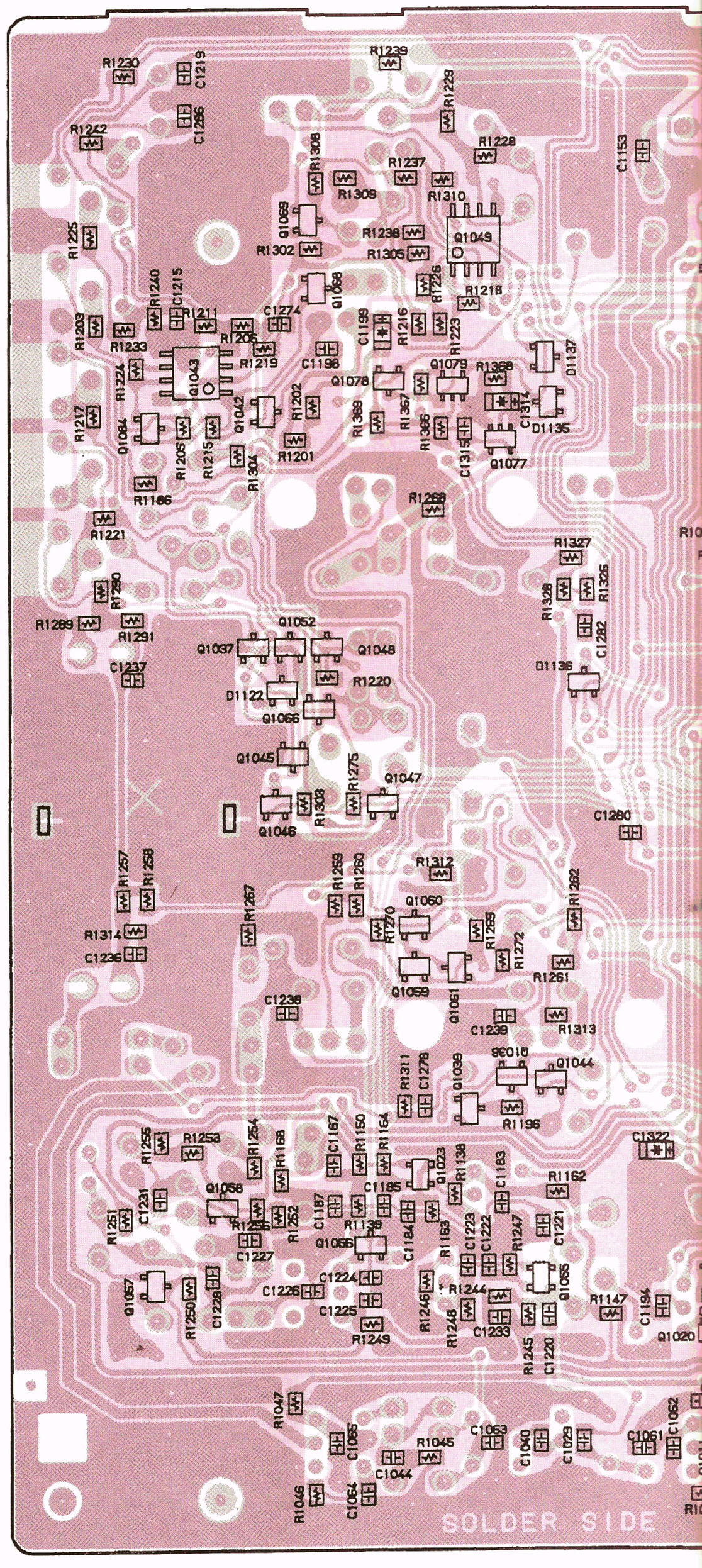


TD62783F
(Q1030,1034)

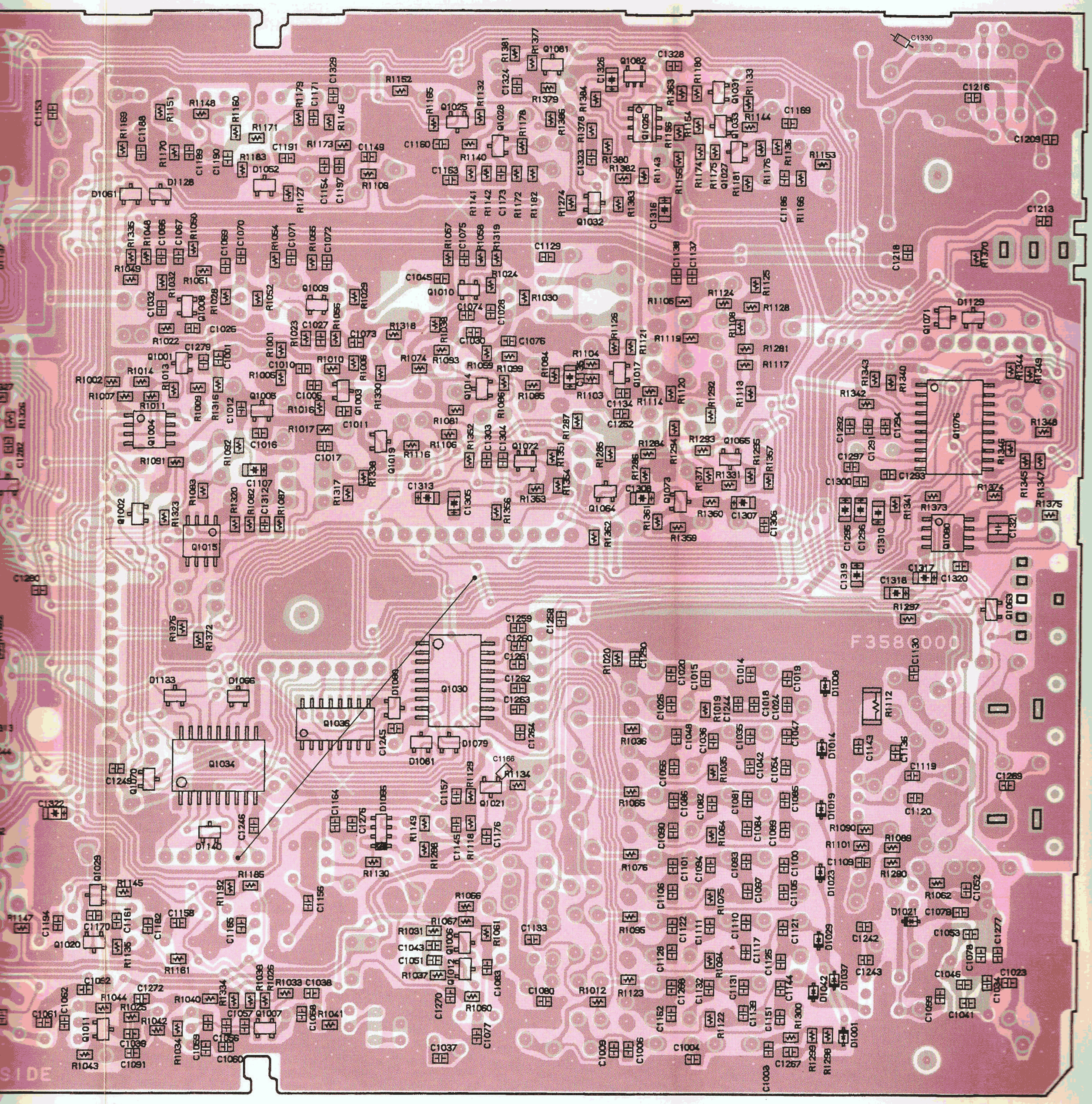


2SJ125D (JD)
(Q1068)

f e



d c b a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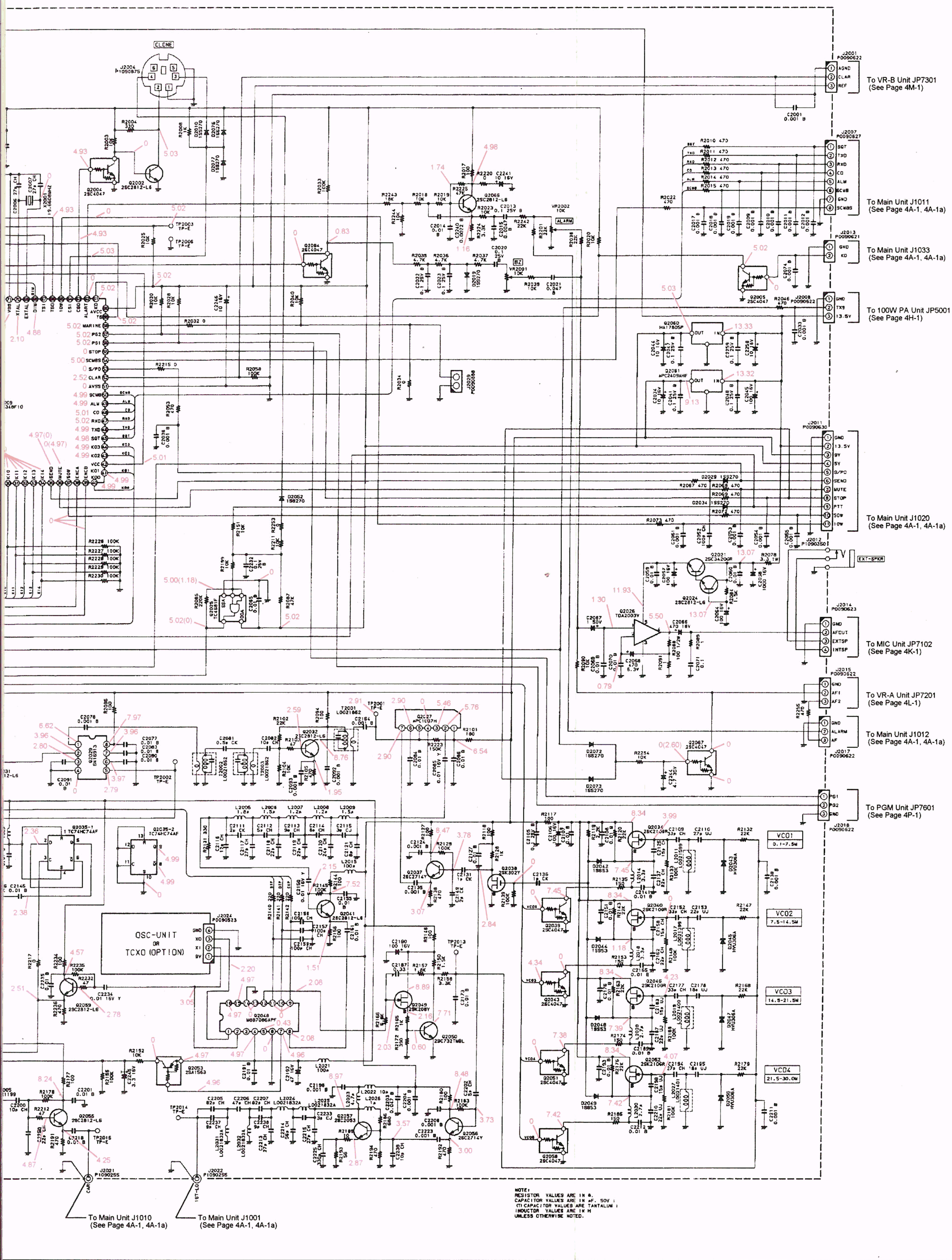
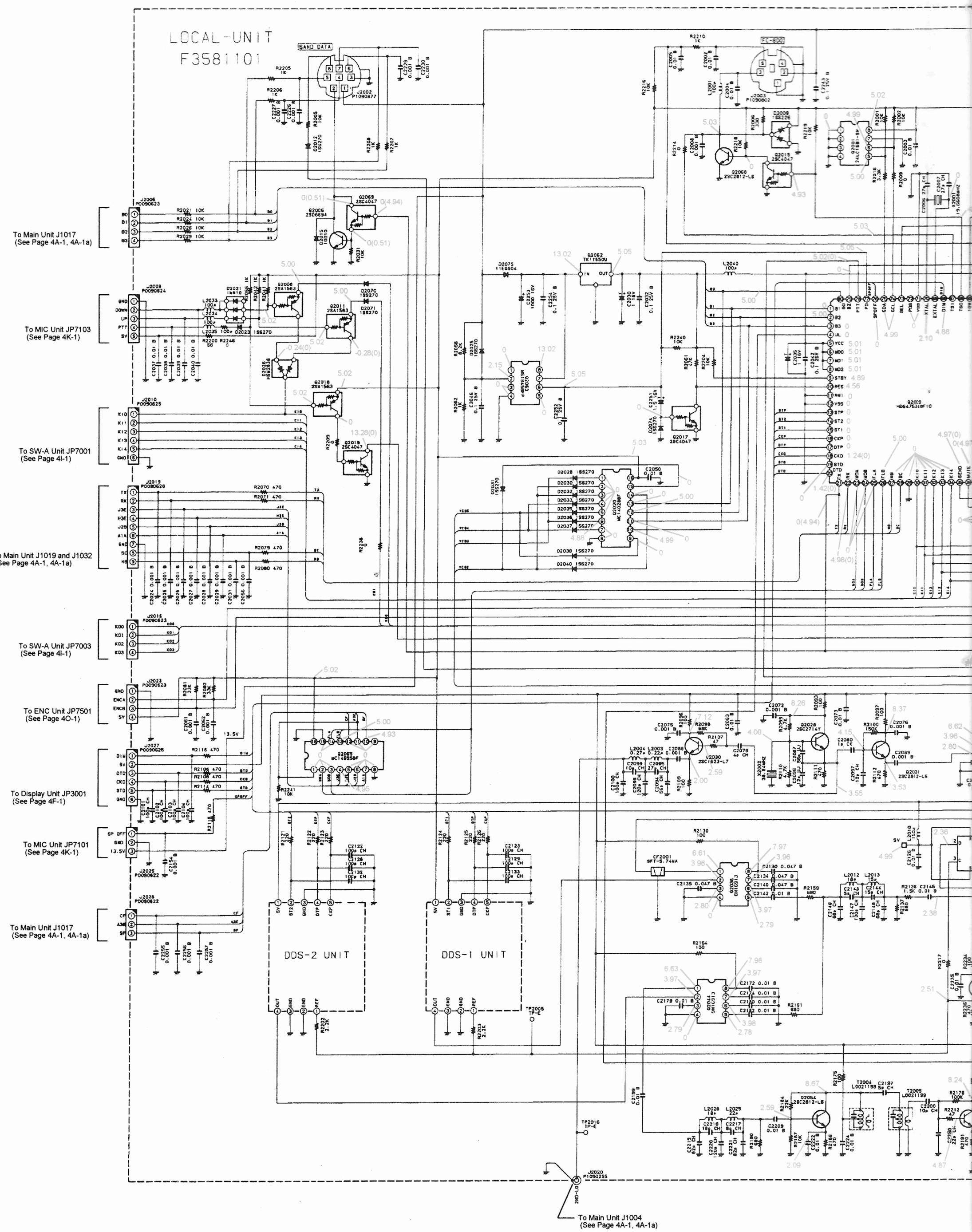

CLONE
J2004 P1090875
J2001 P0090622
AGND
CLAR
REF
To VR-B Unit JP7301 (See Page 4M-1)
J2007 P0090627
SQT
TXD
RXD
CD
ALM
SCWB
GND
SCWBS
To Main Unit J1011 (See Page 4A-1, 4A-1a)
J2013 P0090621
GND
KD
To Main Unit J1033 (See Page 4A-1, 4A-1a)
J2008 P0090622
GND
TX9
13.5V
To 100W PA Unit JP5001 (See Page 4H-1)
J2011 P0090630
GND
13.5V
9V
5V
S/PO
SEND
MUTE
STOP
PTT
SCW
10W
To Main Unit J1020 (See Page 4A-1, 4A-1a)
EXT-SPKR
J2014 P0090623
GND
AFOUT
EXTSP
INTSP
To MIC Unit JP7102 (See Page 4K-1)
J2015 P0090622
GND
AF1
AF2
To VR-A Unit JP7201 (See Page 4L-1)
GND
ALARM
AF
J2017 P0090622
To Main Unit J1012 (See Page 4A-1, 4A-1a)
PG1
PG2
GND
J2018 P0090622
To PGM Unit JP7601 (See Page 4P-1)
VCO1
0.1-7.5M
VCO2
7.5-14.5M
VCO3
14.5-21.5M
VCO4
21.5-30.0M
OSC-UNIT OR TCXO (OPTION)
J2024 P0090323
GND
XO
X1
9V
J2021 P1090255
CAR
J2022 P1090255
187-LO
To Main Unit J1010 (See Page 4A-1, 4A-1a)
To Main Unit J1001 (See Page 4A-1, 4A-1a)
NOTE:
RESISTOR VALUES ARE IN Ω.
CAPACITOR VALUES ARE IN μF, 50V ;
(T) CAPACITOR VALUES ARE TANTALUM ;
INDUCTOR VALUES ARE IN H
UNLESS OTHERWISE NOTED.

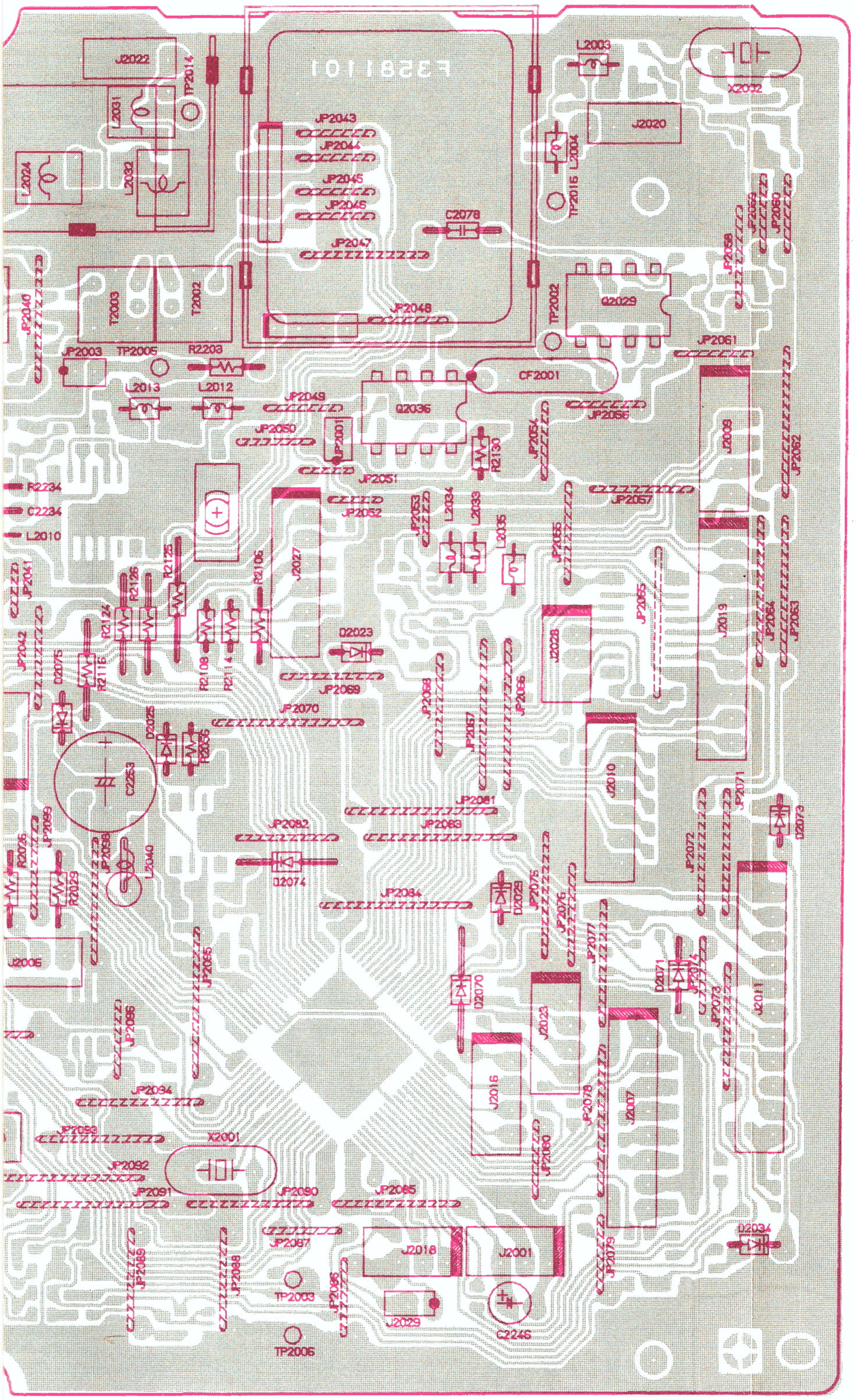
Circuit Diagram



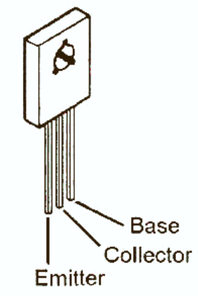
Parts Layout

E F

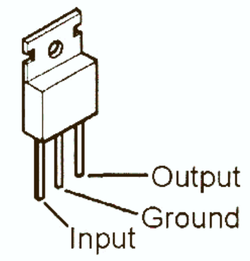
1ST-LO J2022



2ND-LO J2020



2SD669A
(Q2006)



HA17805P
(Q2060)

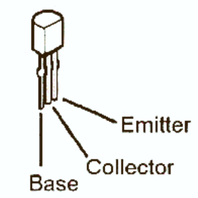
J2009
GND
DOWN
UP
PTT
5V

J2027
DIM
9V
DTD
CKD
STD
GND

J2028
CF
A3E
SF

TX
RX
J3E
H3E
J2B
A1A
GND
SC
NB

J2019



2SC2053
(Q2057)

SP OFF
GND
13.5V

J2025

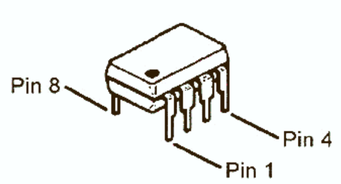
K10
K11
K12
K13
K14
GND

J2010

J2023
GND
ENC A
ENC B
5V

GND
13.5V
9V
5V
S/PO
SEND
MUTE
STOP
PTT
50W
10W

J2011



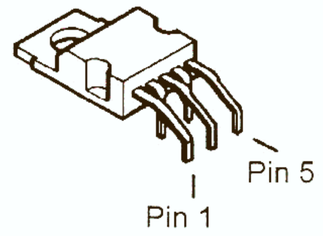
SN16913P
(Q2029,2036,2044)

K00
K01
K02
K03

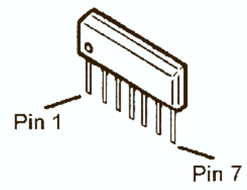
J2016

SQT
TXD
RXD
CD
ALM
SCMB
GND
SCMB-S

J2007



TDA2003
(Q2026)



μPC1037H
(Q2027)

B0 B1 B2 B3

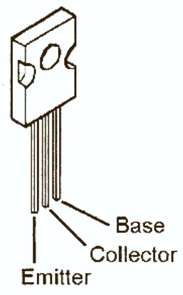
J2006

GND PG2 PG1

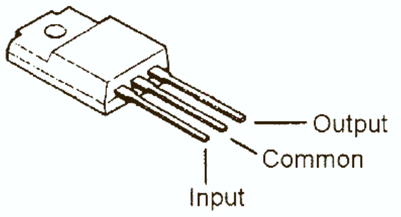
J2018

REF CLAR AGND

J2001



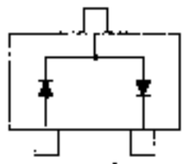
2SC3420GR
(Q2021)



KIA7809PI
(Q2061)

Component Side

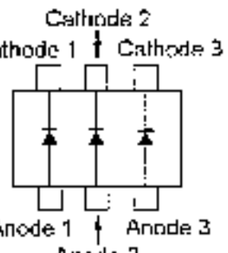
Cathode 1, Anode 2



Anode 1 Cathode 2

1SS226 (C3)
(D2009)

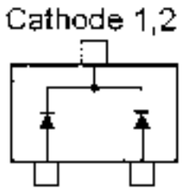
Cathode 2
Cathode 1 Cathode 3



Anode 1 Anode 3
Anode 2

IMN10 (N10)
(D2021)

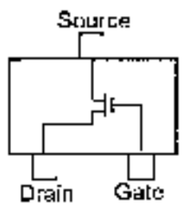
Cathode 1,2



Anode 1 Anode 2

HSM2838 (A6)
(D2026)

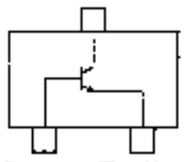
Source



Drain Gate

2SK302Y (TY)
(Q2038)

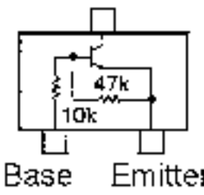
Collector



Base Emitter

2SC2714Y (QY)
(Q2037,2056)
2SC2812 (L6)
(Q2014,2054,2055
2059,2066,2068)

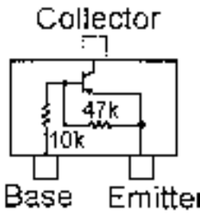
Collector



Base Emitter

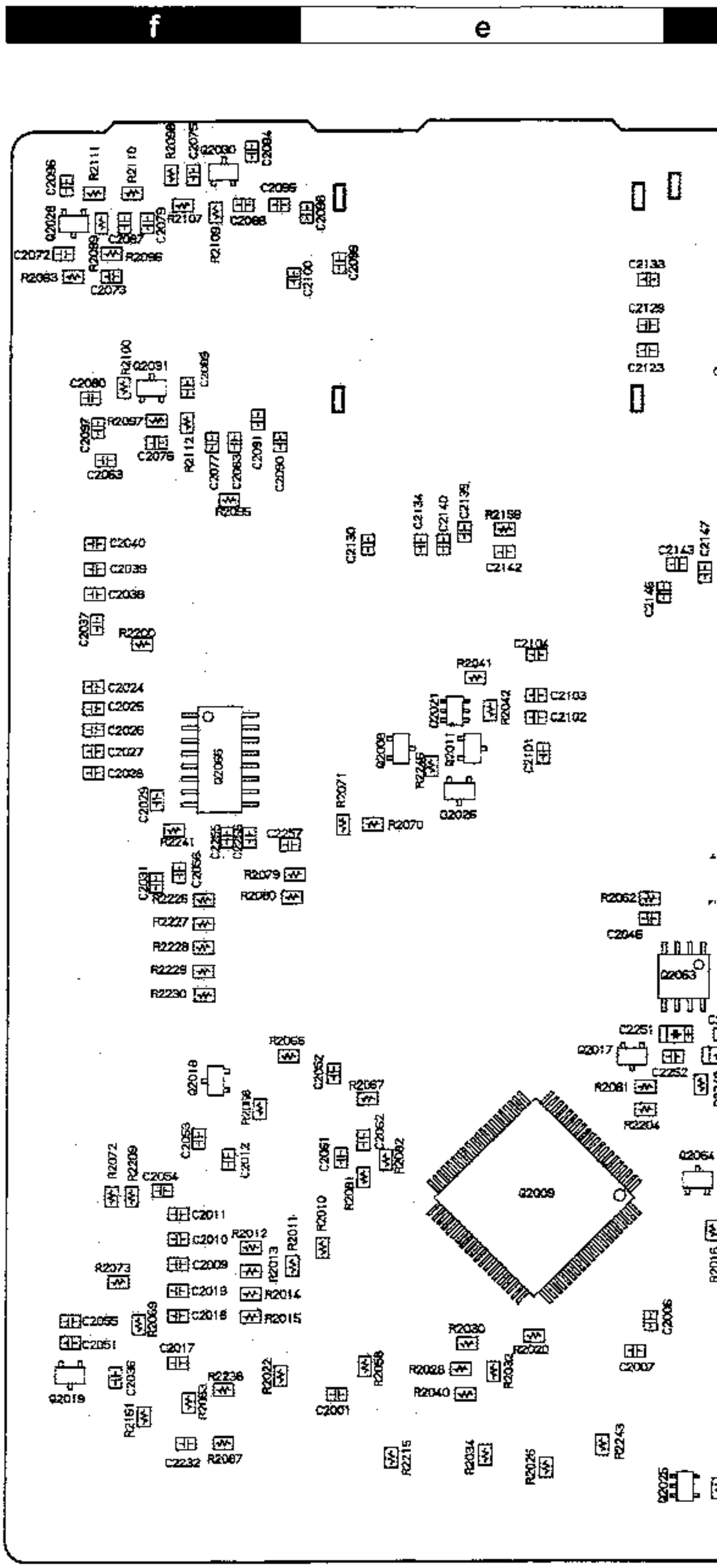
2SC4047 (ZY)
(Q2039,2043,2051,2058
2064,2067,2069)

Collector



Base Emitter

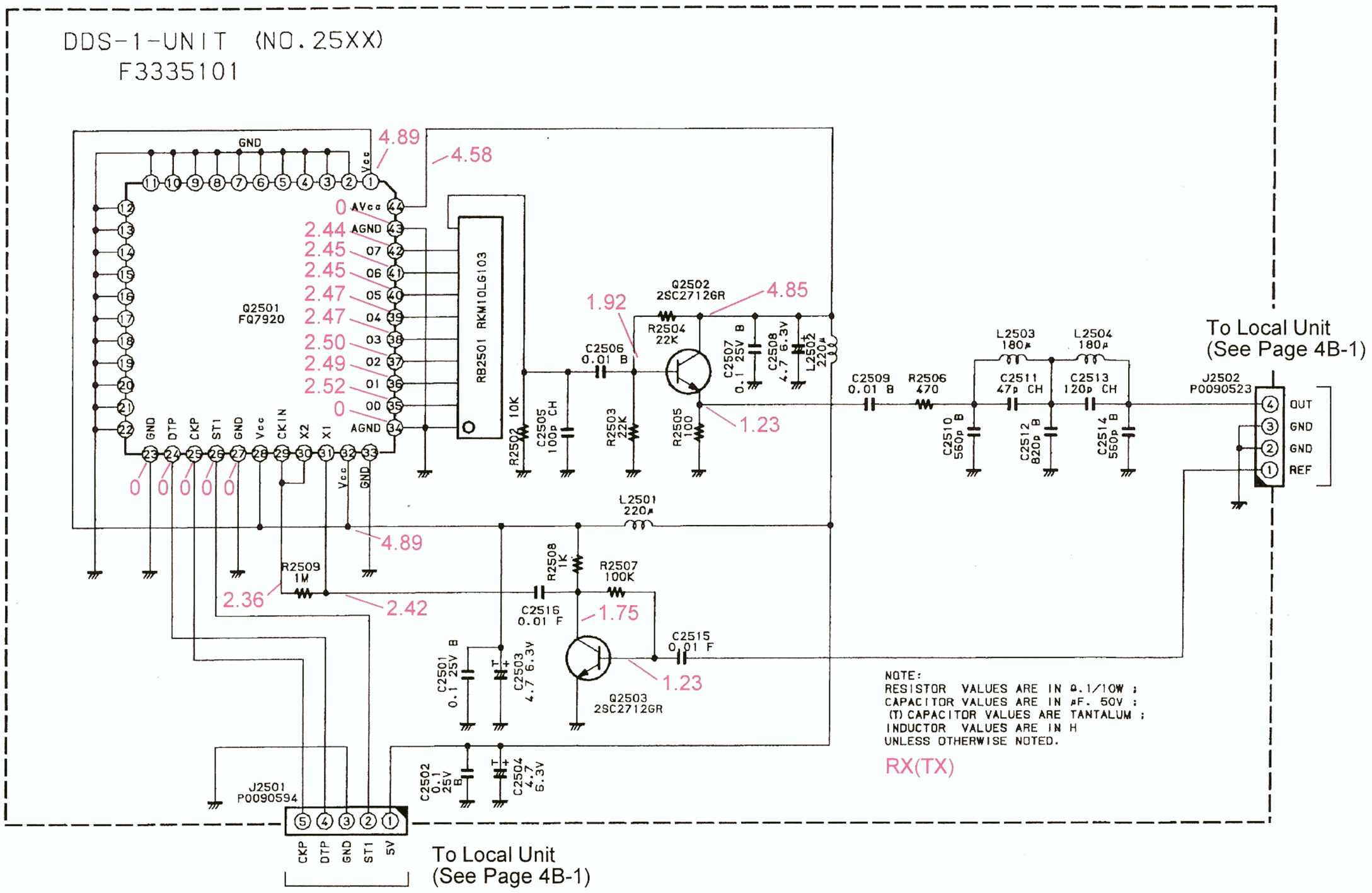
2SA1563 (RL)
(Q2053)



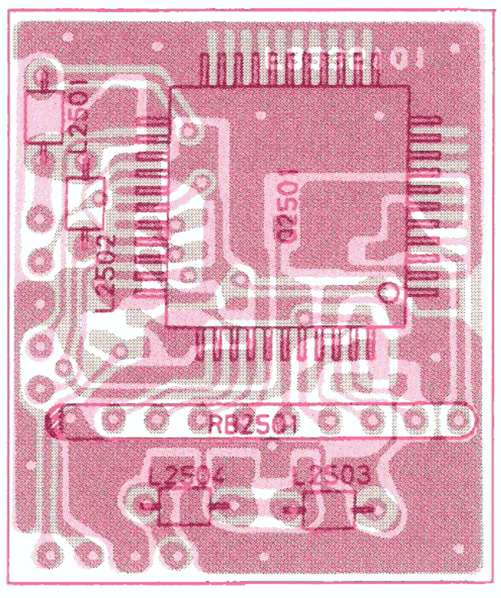
d c b a

Chip Side

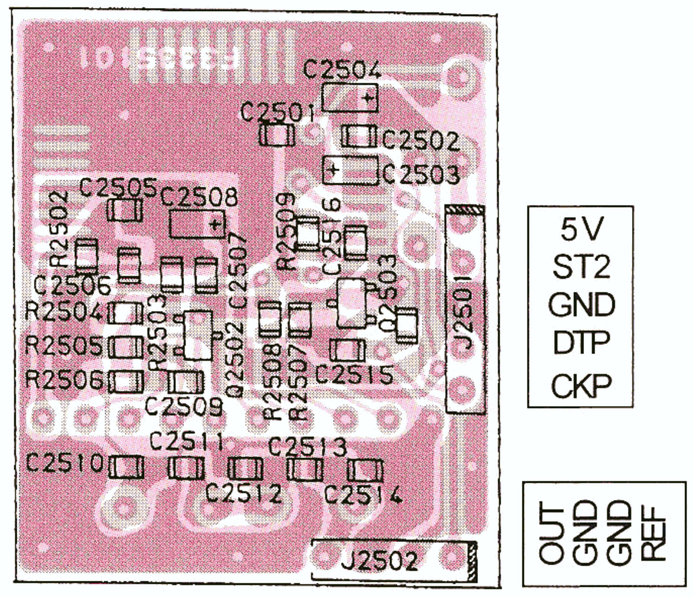
Circuit Diagram



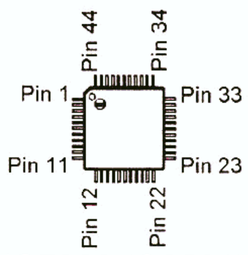
Parts Layout



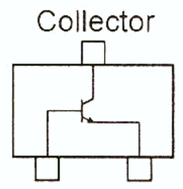
Component Side



Connector Side



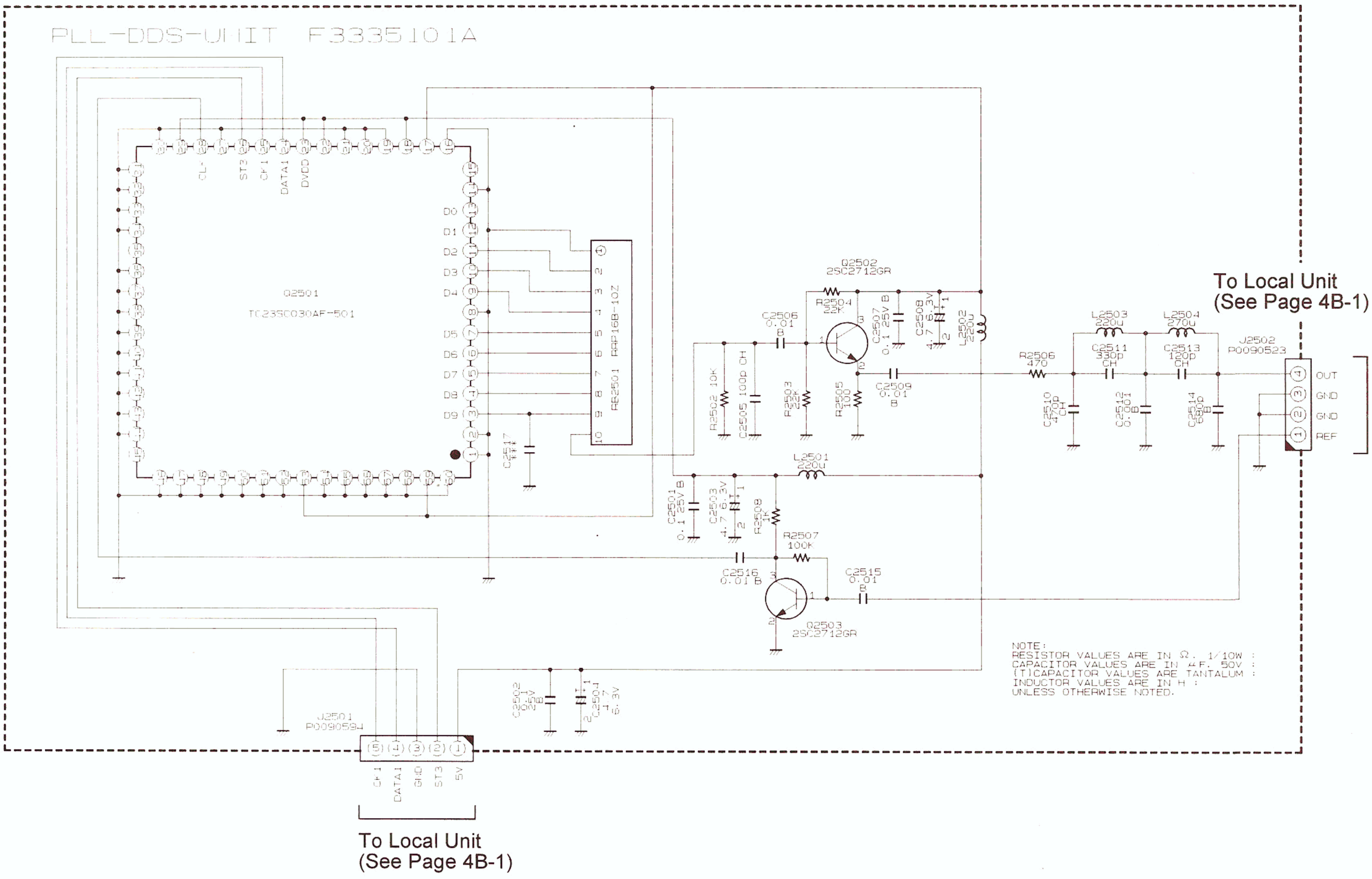
FQ7920 (Q2501)



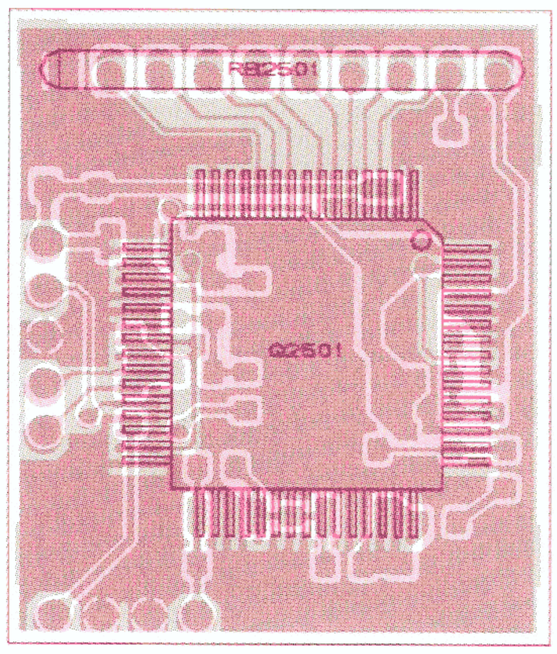
2SC2712GR (LG)
(Q2502,2503)

DDS-1 Unit (Lot. 11~)

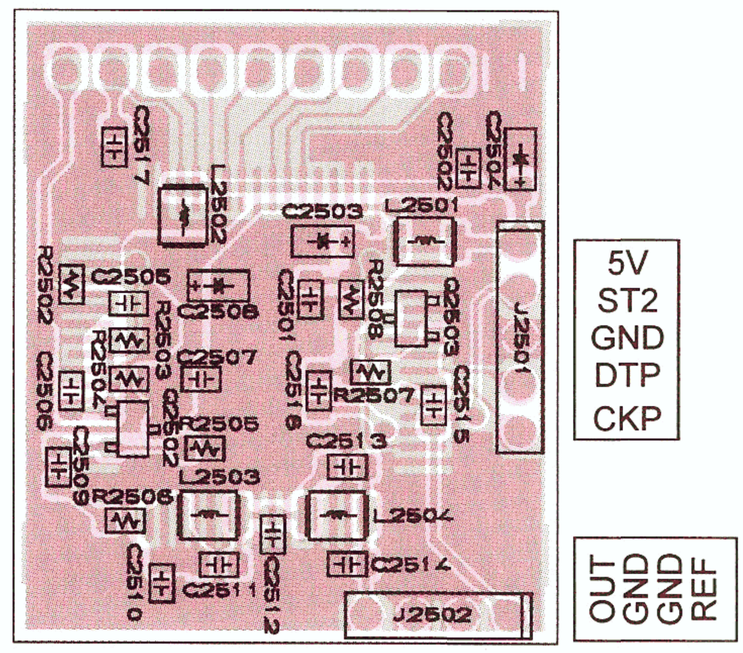
Circuit Diagram



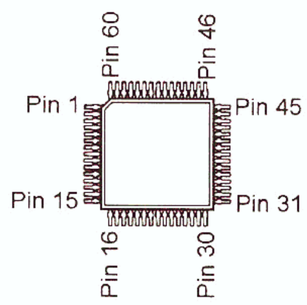
Parts Layout



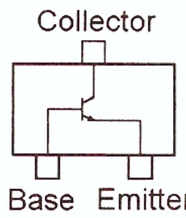
Compornent Side



Connector Side

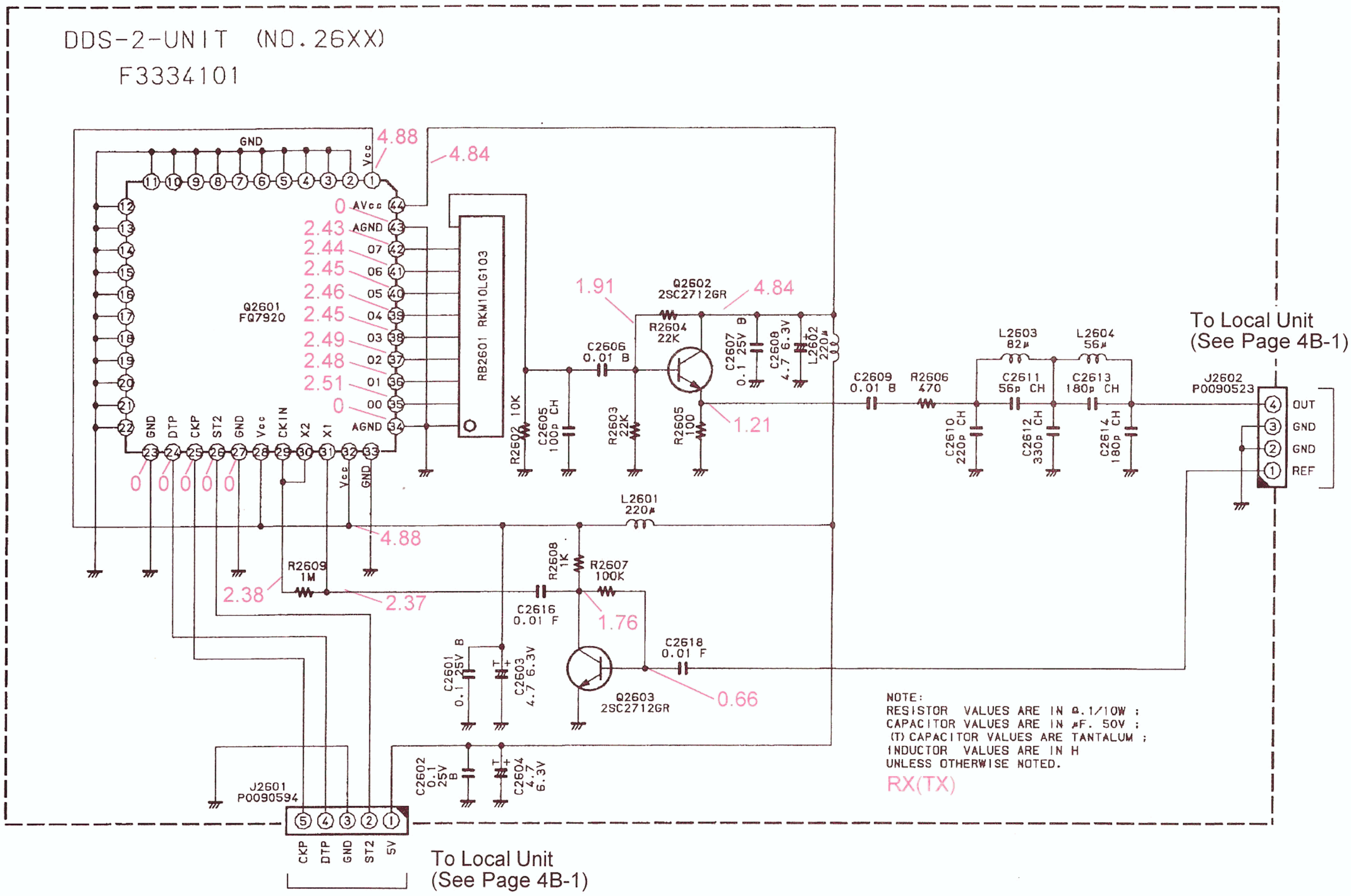


TC23SC030AF-501
(Q2501)

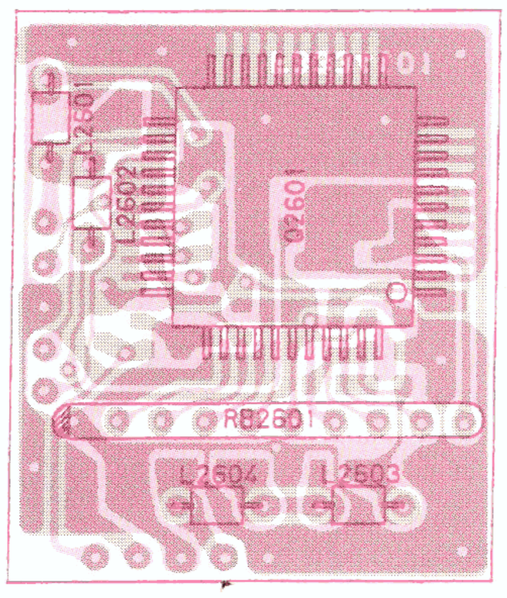


2SC2712GR (LG)
(Q2502, 2503)

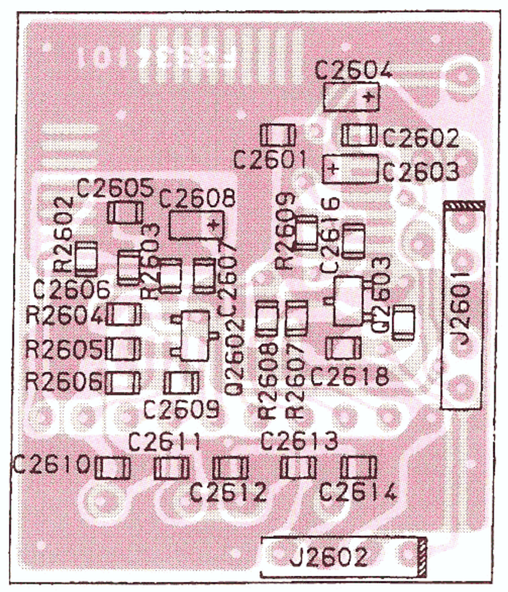
Circuit Diagram



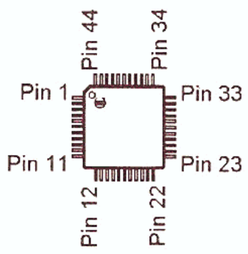
Parts Layout



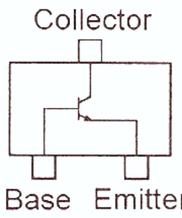
Component Side



Connector Side



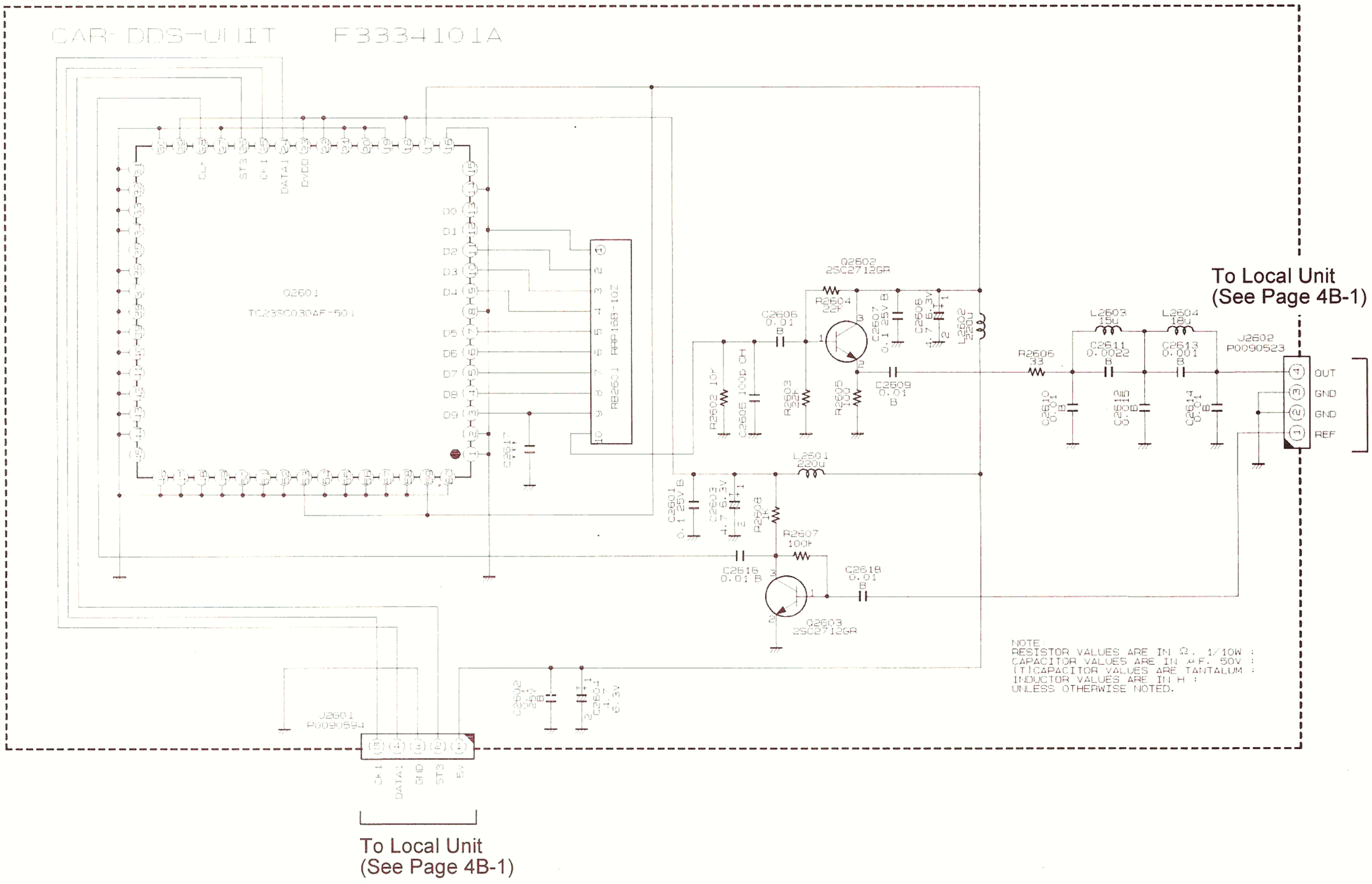
FQ7920 (Q2601)



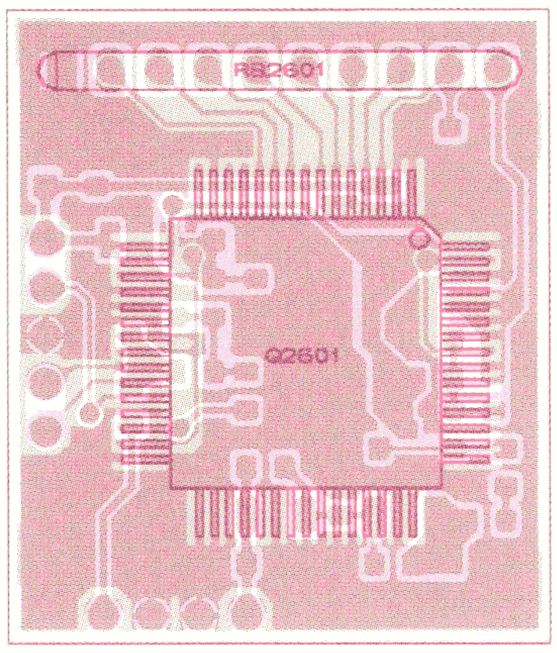
2SC2712GR (LG)
(Q2602,2603)

DDS-2 Unit (Lot. 11~)

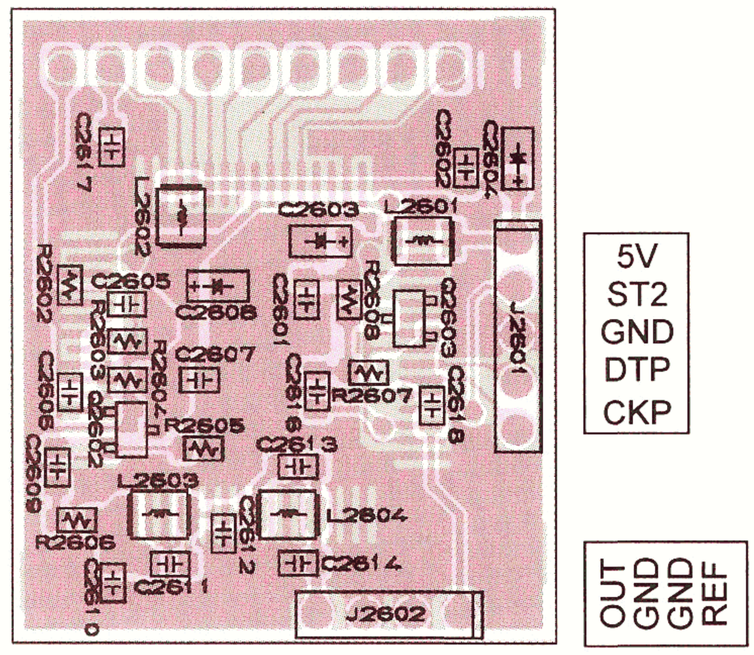
Circuit Diagram



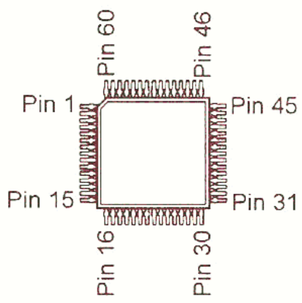
Parts Layout



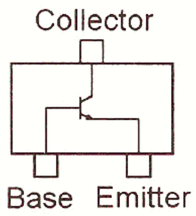
Component Side



Connector Side



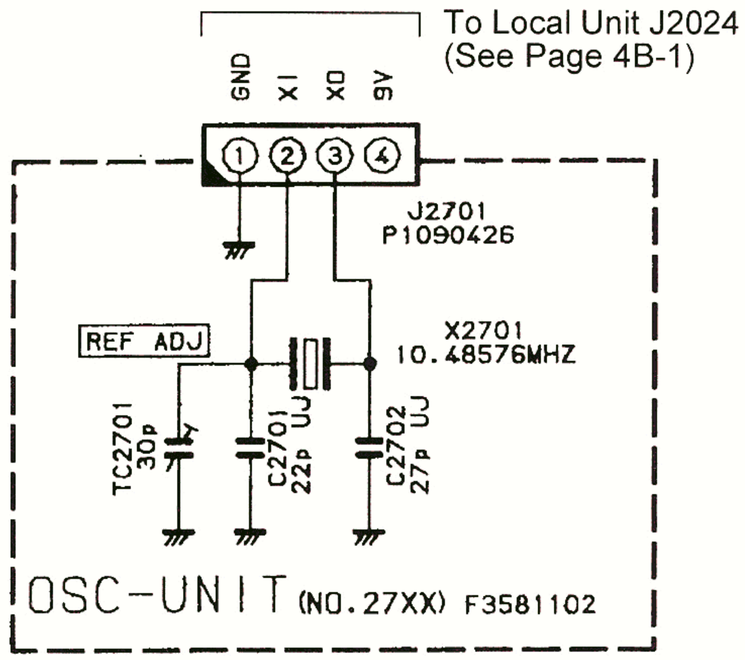
TC23SC030AF-501
(Q2601)



2SC2712GR (LG)
(Q2602,2603)

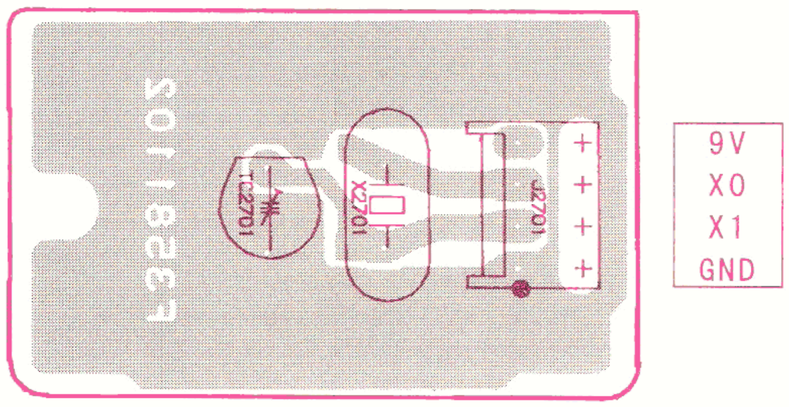
OSC Unit

Circuit Diagram



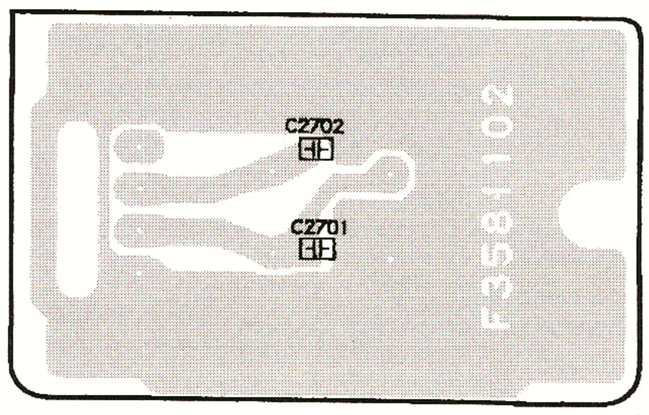
NOTE:
CAPACITOR VALUES ARE IN μF. 50V ;
UNLESS OTHERWISE NOTED.

Parts Layout



9V
XO
X1
GND

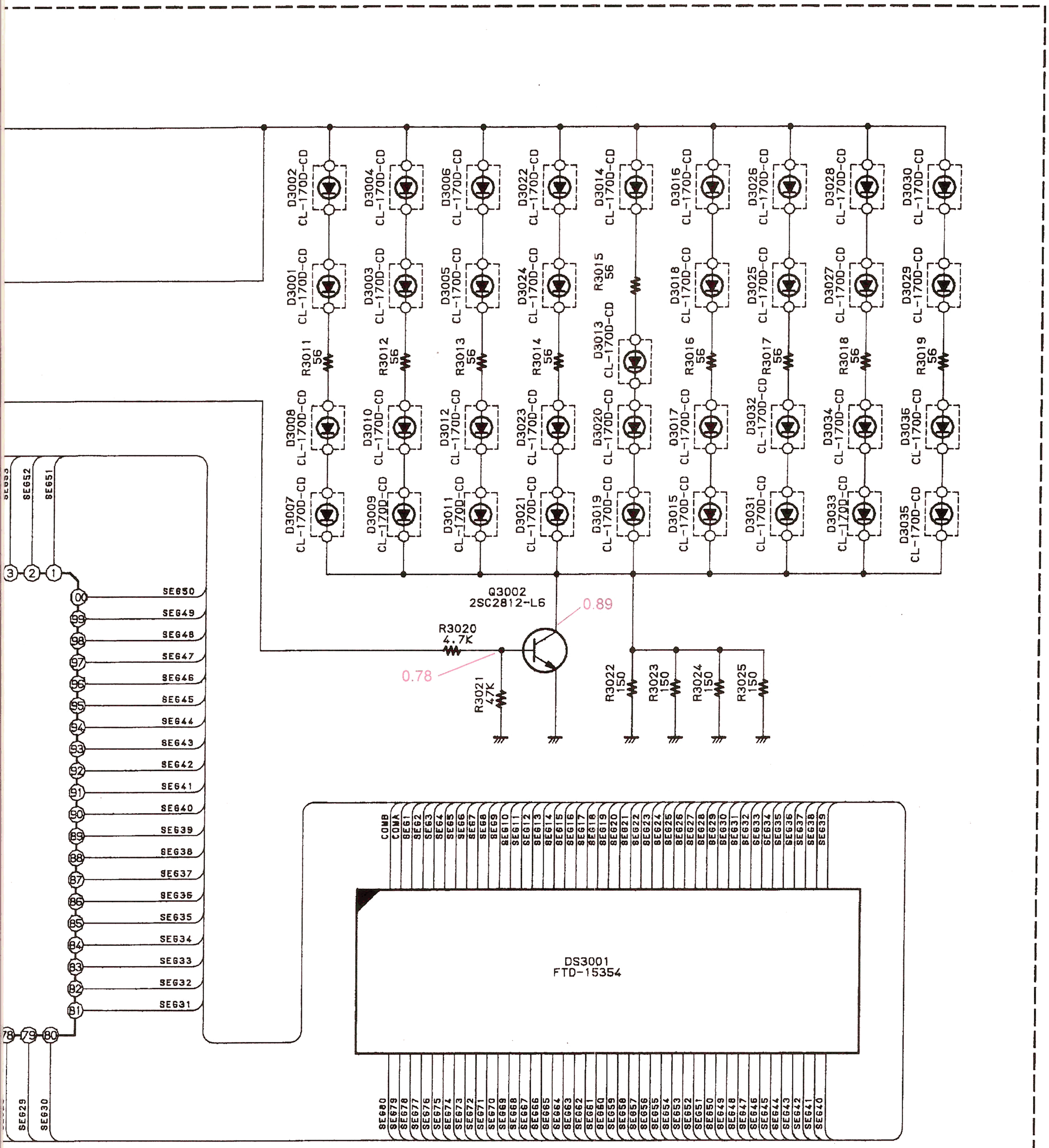
Component Side



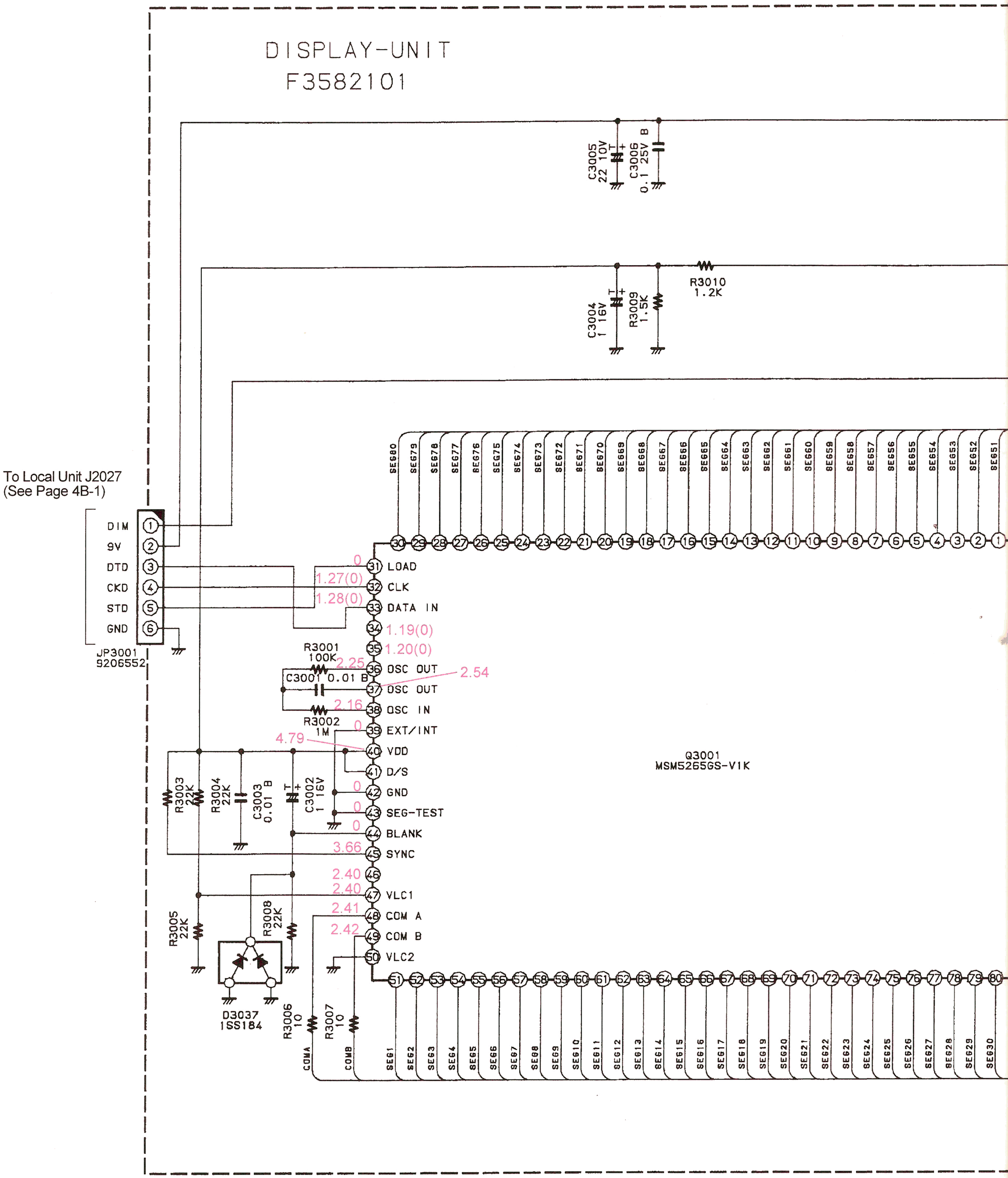
Chip Side

Parts List

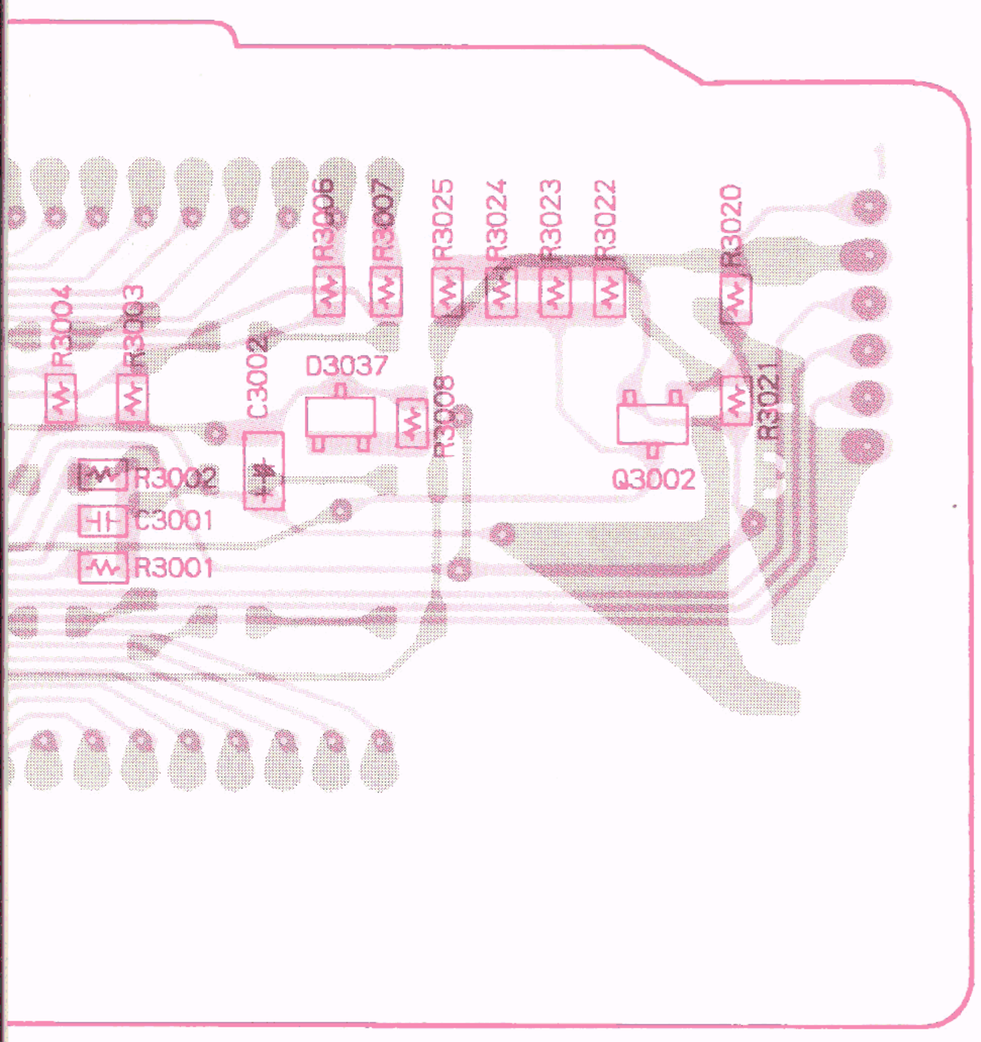
REF.	DESCRIPTION	VALUE	WV	TOL.	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
			*** OSC UNIT ***						
	PCB with Components					CA1583001			
	Printed Circuit Board					F3581102			
C 2701	CHIP CAP.	22pF	50V	UJ	GRM40UJ220J50PT	K22170319			
C 2702	CHIP CAP.	27pF	50V	UJ	GRM40UJ270J50PT	K22170321			
J 2701	CONNECTOR				5124-04BHPB	P1090426			
TC2701	TRIMMER CAP.	30pF			VCT51F	K91000093			
X 2701	XTAL	10.48576MHz				H0102990			

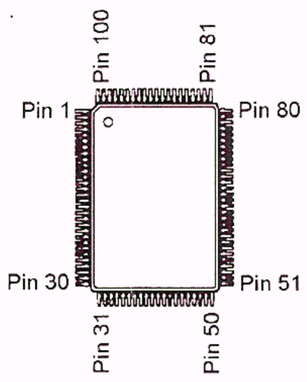


NOTE:
RESISTOR VALUES ARE IN Ω.1/10W ;
CAPACITOR VALUES ARE IN μF. 50V ;
UNLESS OTHERWISE NOTED.

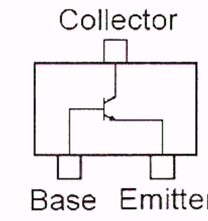

DISPLAY-UNIT
F3582101
C3005 22 10V
C3006 0.1 25V B
C3004 1 16V
R3009 1.5K
R3010 1.2K
To Local Unit J2027
(See Page 4B-1)
DIM
9V
DTD
CKD
STD
GND
JP3001
9206552
R3001 100K
C3001 0.01 B
R3002 1M
R3003 22K
R3004 22K
C3003 0.01 B
C3002 1 16V
R3005 22K
R3008 22K
D3037
1SS184
R3006 10
R3007 10
LOAD
CLK
DATA IN
OSC OUT
OSC OUT
OSC IN
EXT/INT
VDD
D/S
GND
SEG-TEST
BLANK
SYNC
VLC1
COM A
COM B
VLC2
COMA
COMB
Q3001
MSM5265GS-V1K

E

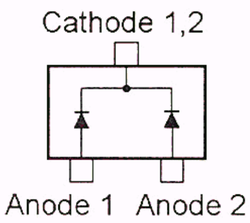




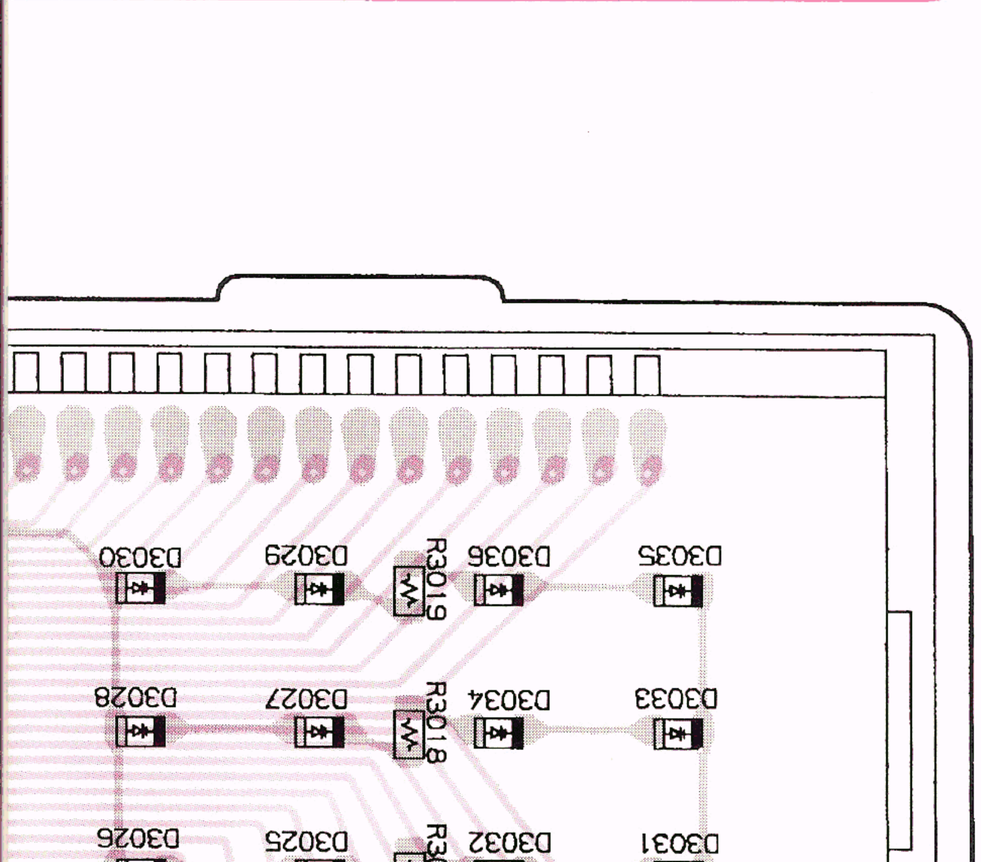
MSM5265GS
(Q3001)

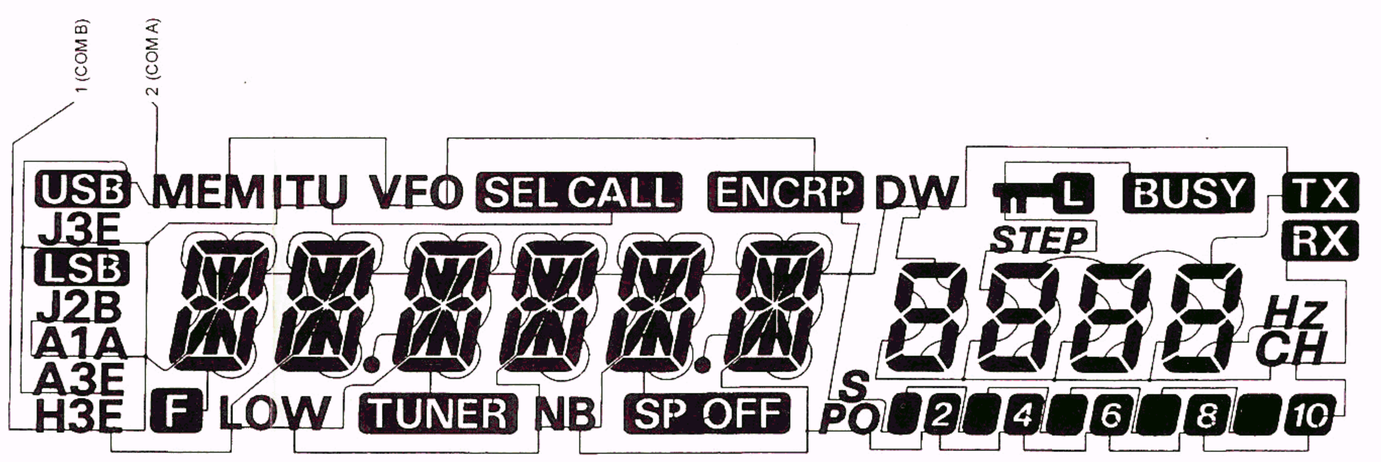


2SC2812 (L6)
(Q3002)

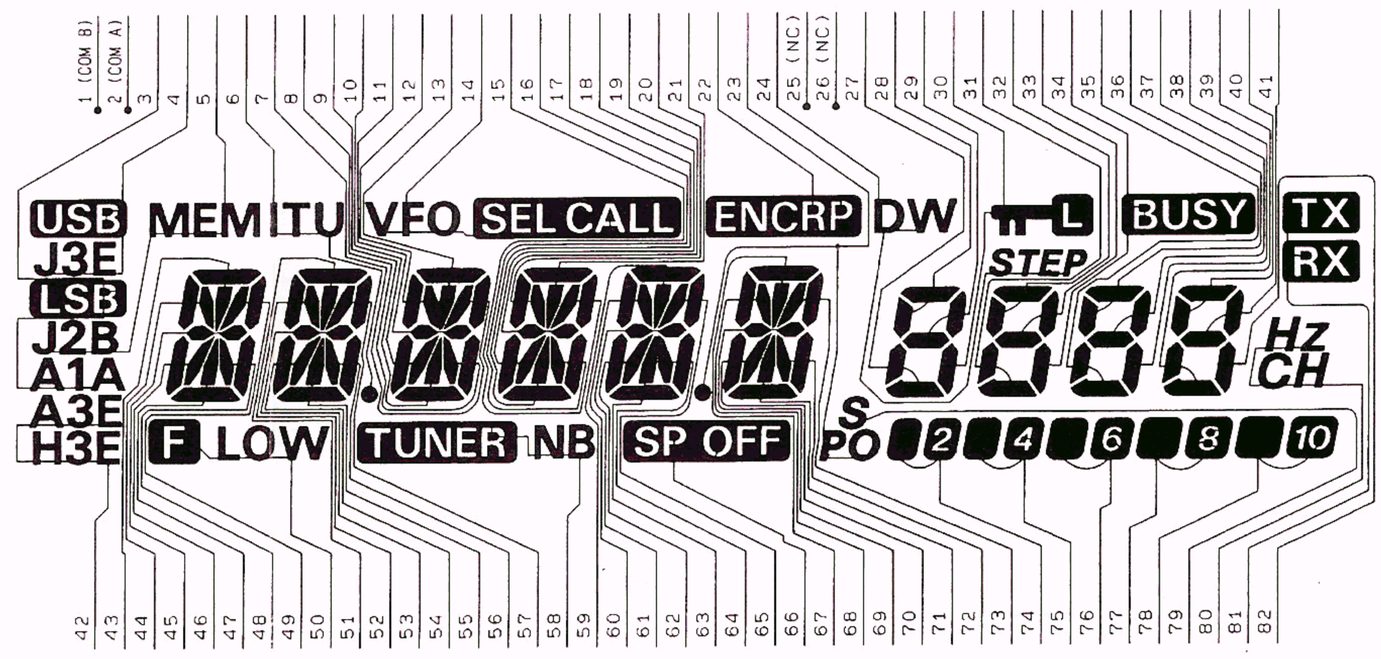


1SS184 (B3)
(D3037)





LCD Backplane Circuit Diagram

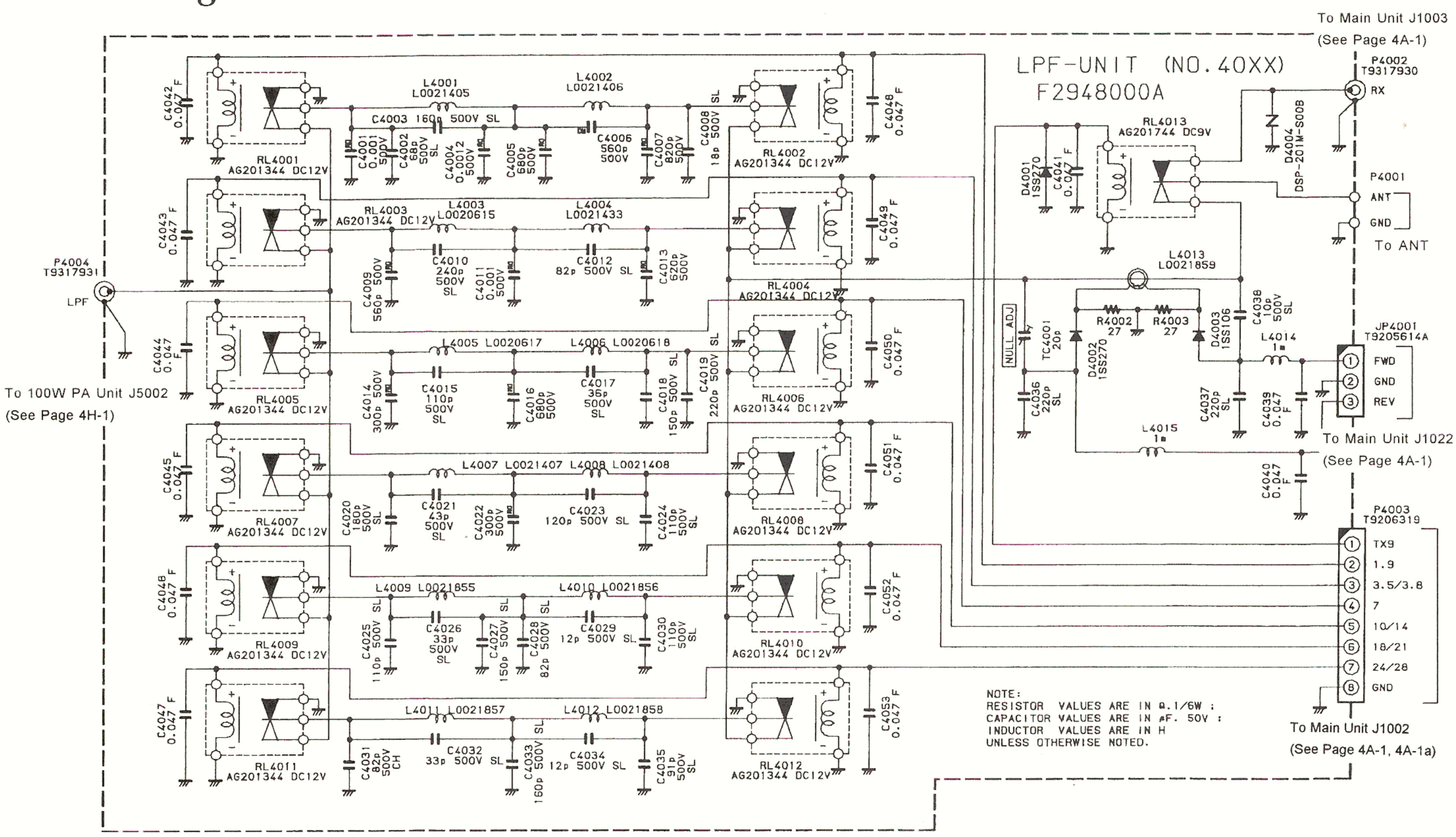


LCD Segmentation Circuit Diagram

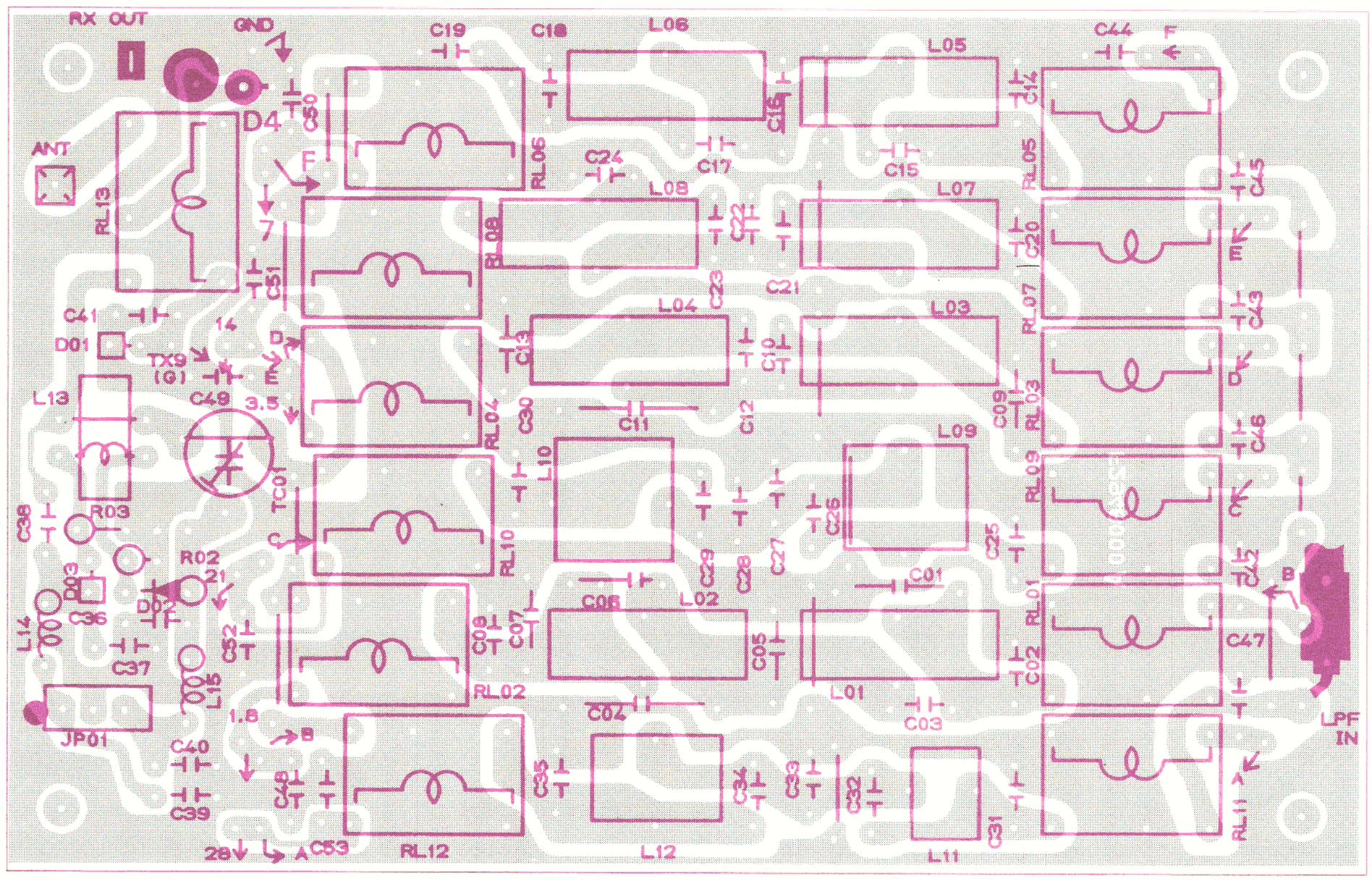
A
B
C
D
1
2
3
4
Q3001
DS3001
JP3001
DIM
9V
DTD
CKD
STD
GND
C3003
C3005
C3006
C3004
R3005
R3004
R3009
R3010
R3011
R3012
R3013
R3014
R3015
R3016
CPU Side
LCD Side

LPF Unit

Circuit Diagram



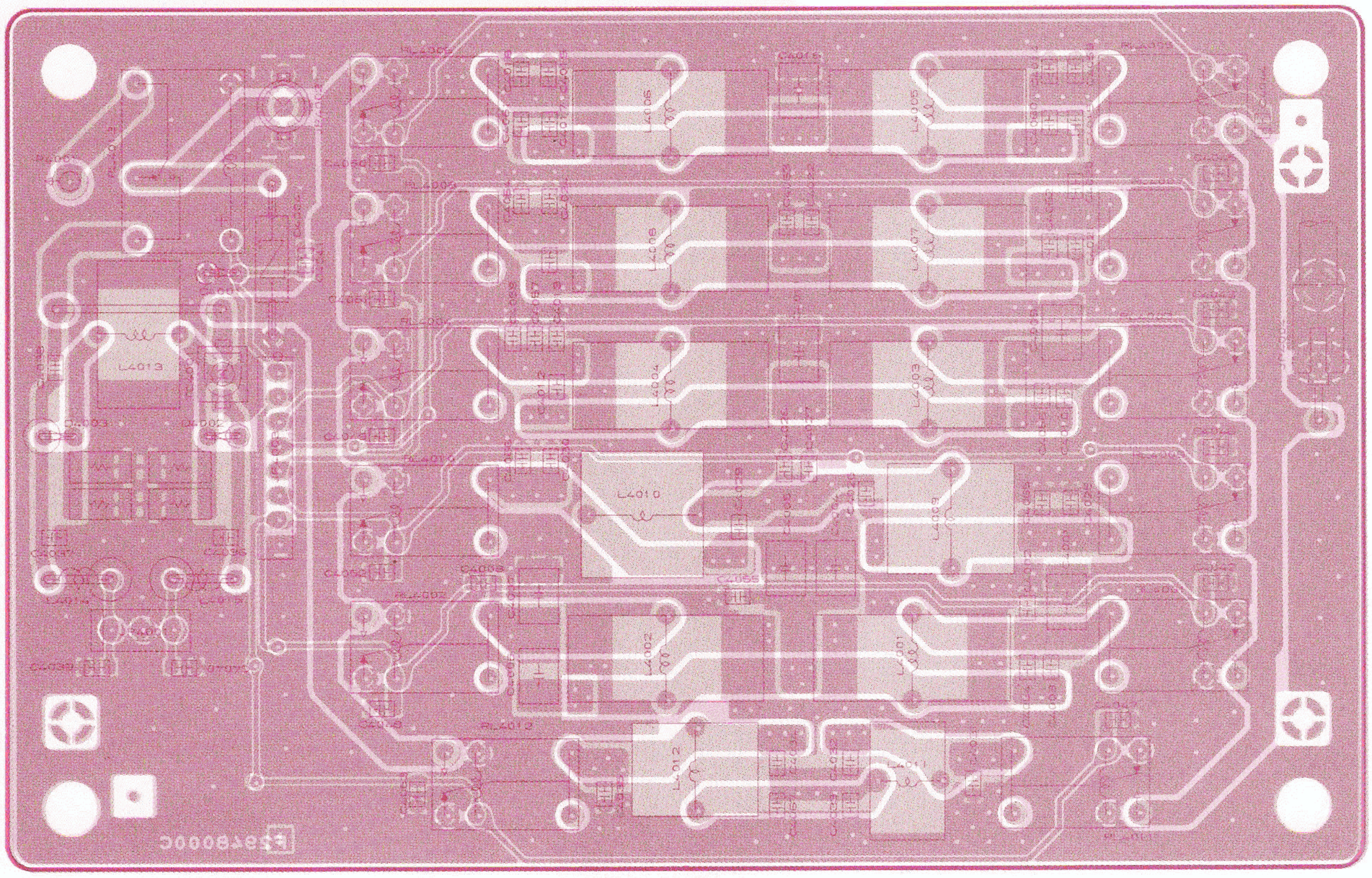
Parts Layout



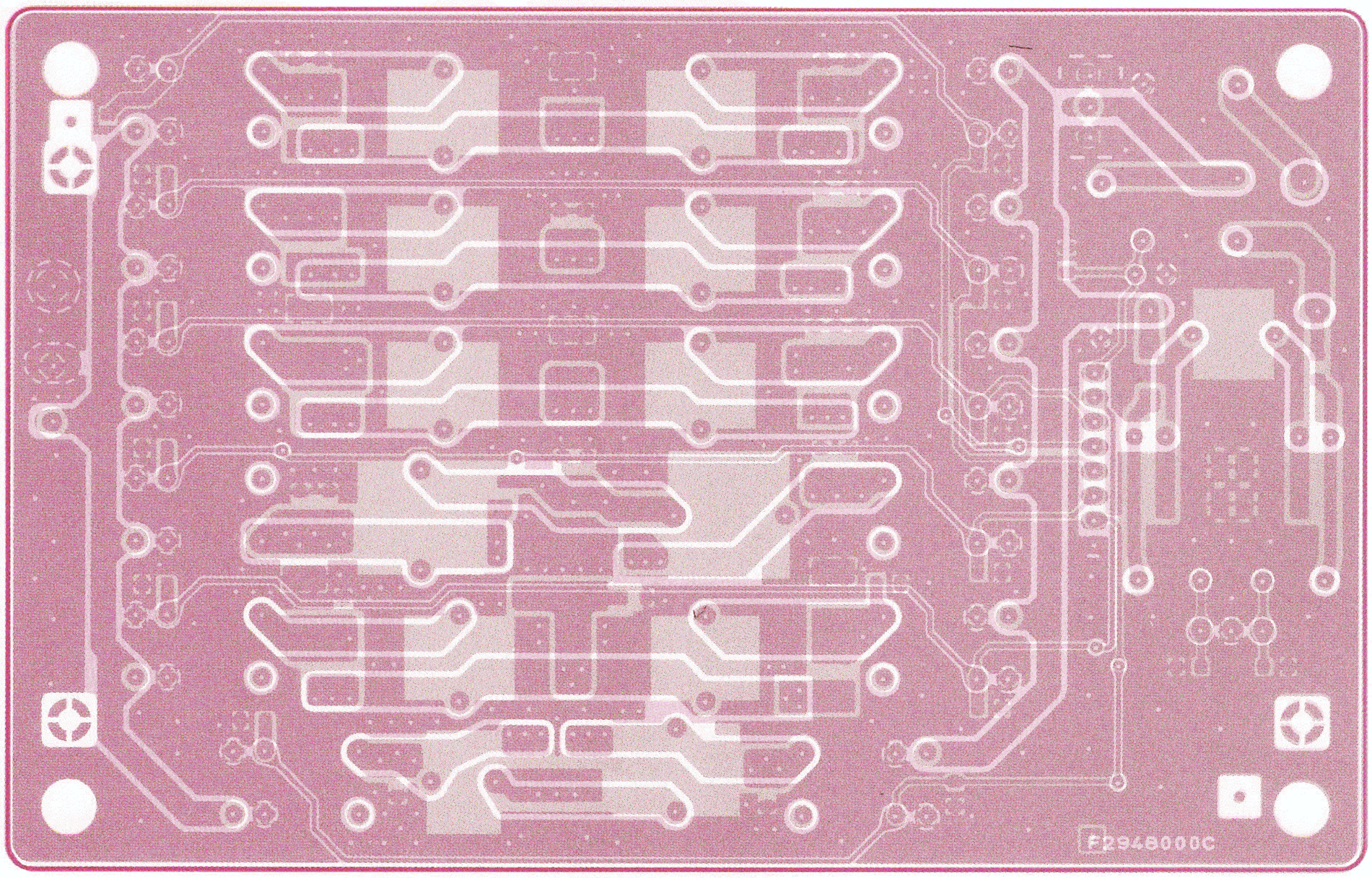
Component Side

LPF Unit (Lot. 23~)

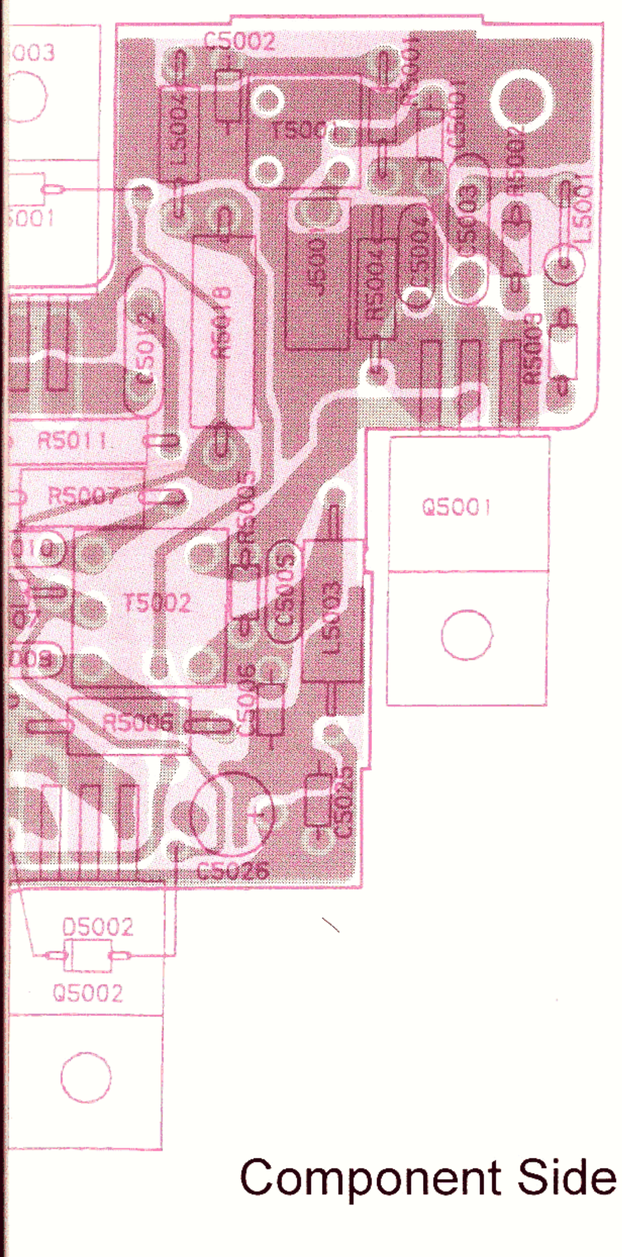
Parts Layout



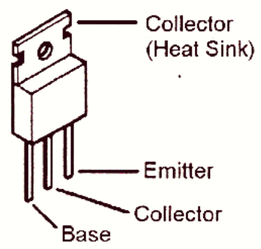
Component Side



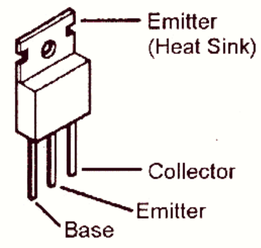
Solder Side



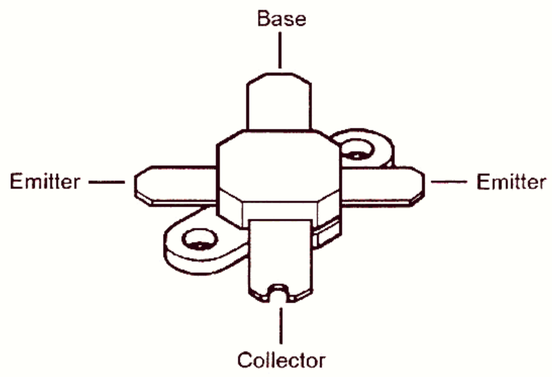
Component Side



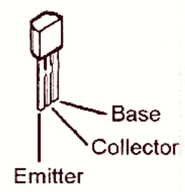
2SC2166
(Q5001)

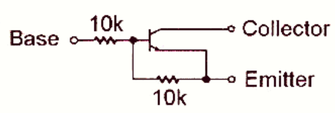


2SC3133
(Q5002,5003)

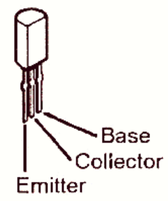


2SC3240
(Q5004,5005)

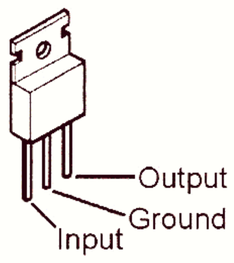




BA1A4M
(Q5006)



2SA1283D
(Q5007)
2SC2001
(Q5011)



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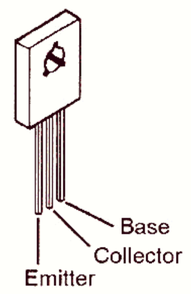
(Q5008)



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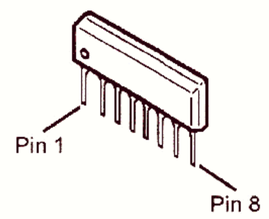
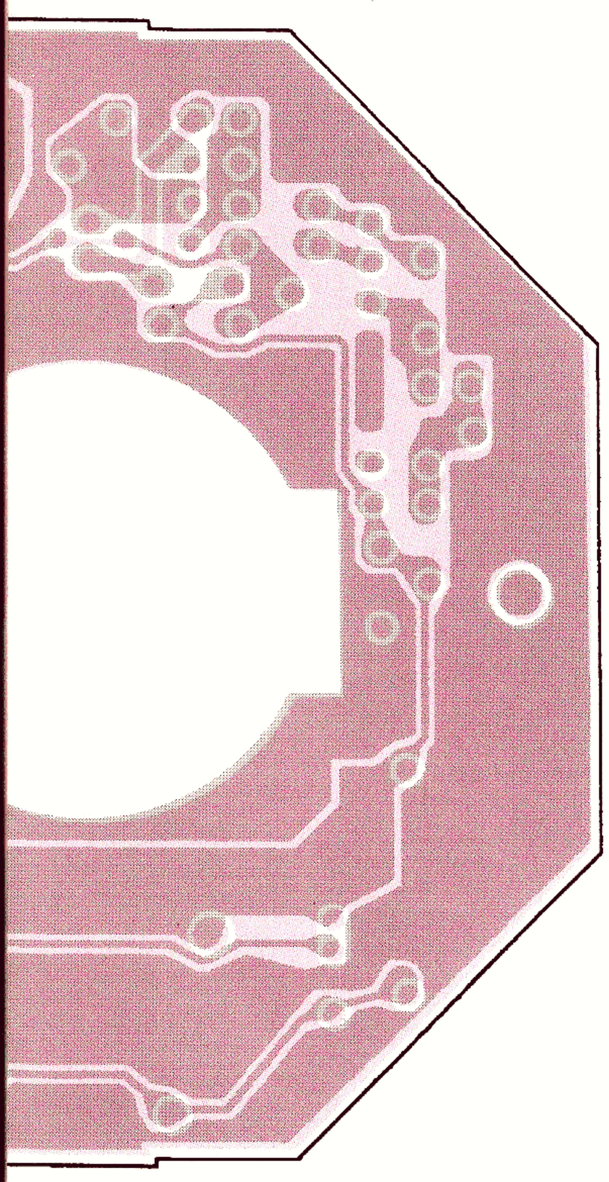
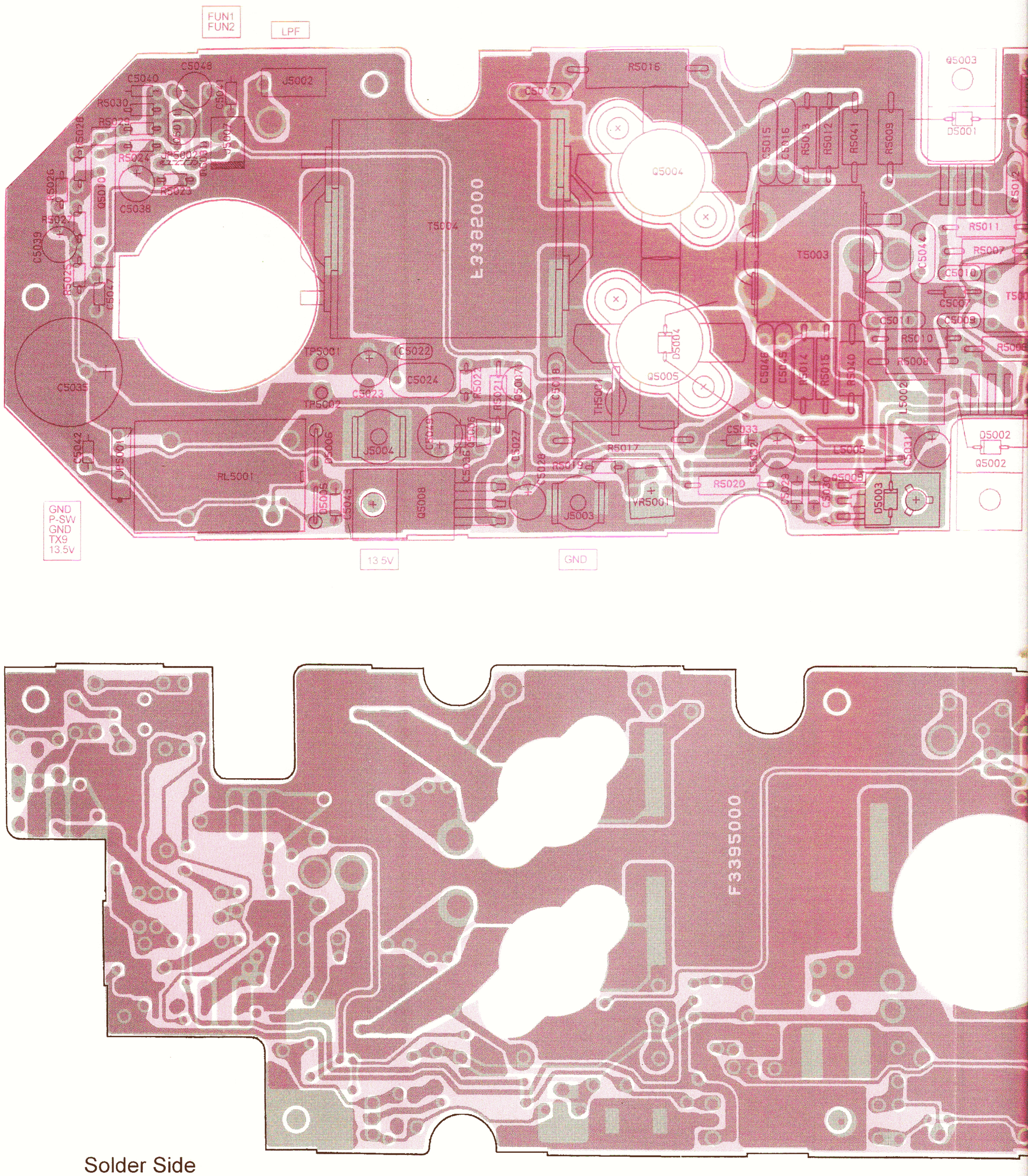
(Q5009)

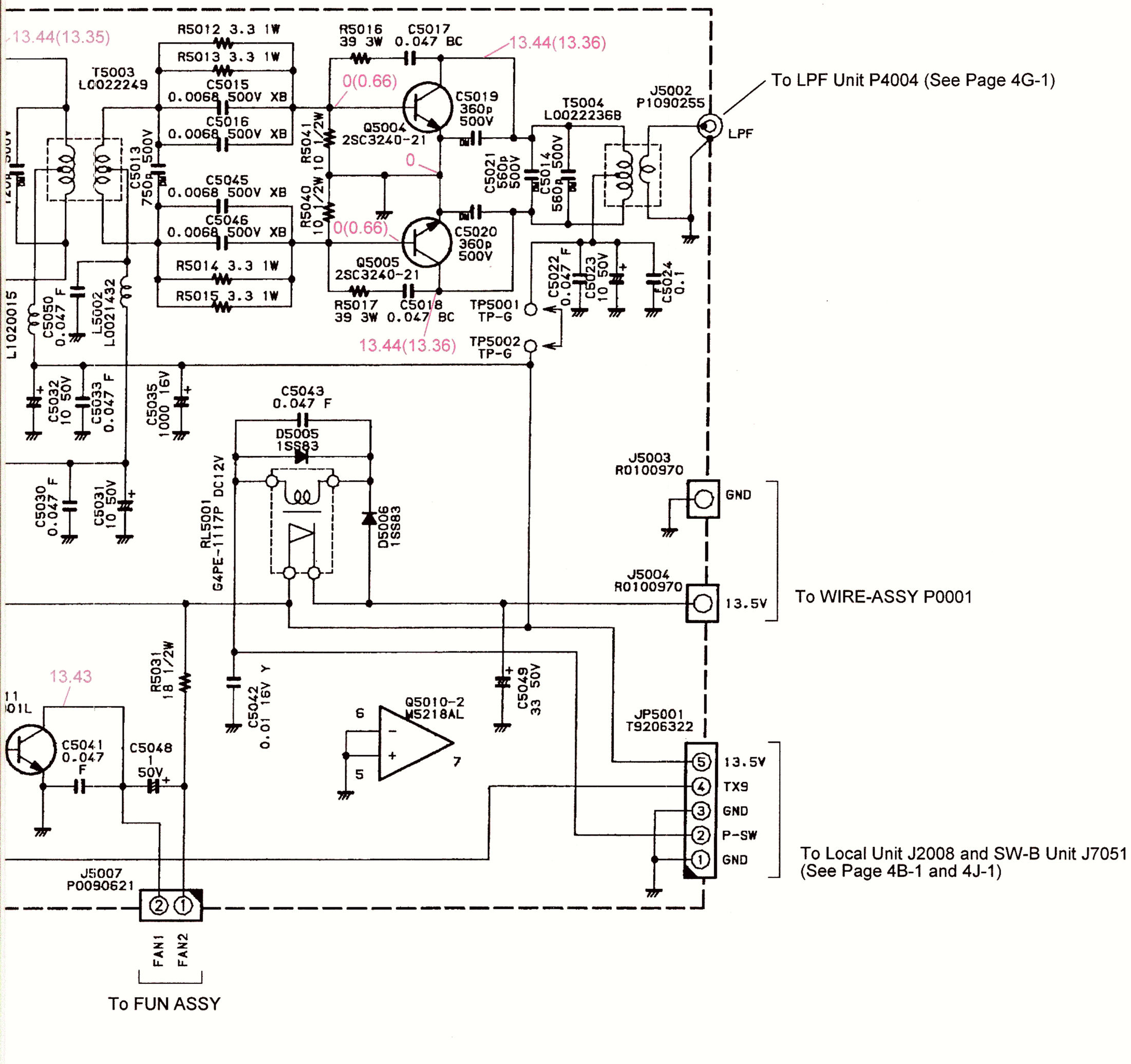


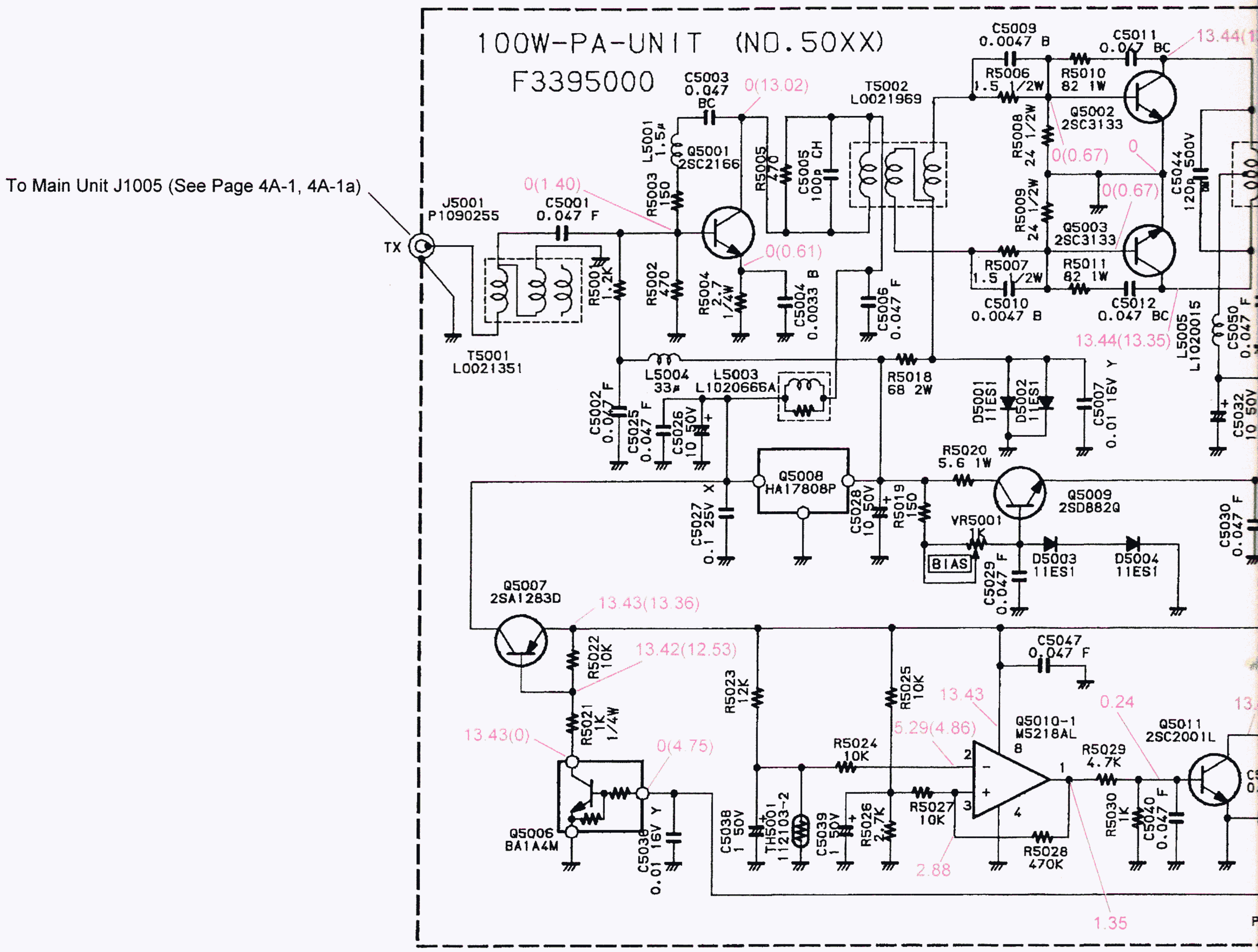
M5218AL
(Q5010)



Parts Layout




13.44(13.35)
R5012 3.3 1W
R5013 3.3 1W
T5003
L0022249
C5015
0.0068 500V XB
C5016
0.0068 500V XB
C5013
750p 500V
C5045
0.0068 500V XB
C5046
0.0068 500V XB
R5014 3.3 1W
R5015 3.3 1W
R5016
39 3W
C5017
0.047 BC
13.44(13.36)
0(0.66)
Q5004
2SC3240-21
C5019
360p
500V
R5041
10 1/2W
0
R5040
10 1/2W
0(0.66)
Q5005
2SC3240-21
C5020
360p
500V
R5017
39 3W
C5018
0.047 BC
13.44(13.36)
T5004
L0022236B
C5021
560p
500V
C5014
560p 500V
J5002
P1090255
LPF
To LPF Unit P4004 (See Page 4G-1)
TP5001
TP-G
TP5002
TP-G
C5022
0.047 F
C5023
10 50V
C5024
0.1
L1020015
C5050
0.047 F
L5002
L0021432
C5032
10 50V
C5033
0.047 F
C5035
1000 16V
C5043
0.047 F
D5005
1SS83
RL5001
G4PE-1117P DC12V
D5006
1SS83
C5030
0.047 F
C5031
10 50V
J5003
R0100970
GND
J5004
R0100970
13.5V
To WIRE-ASSY P0001
13.43
R5031
18 1/2W
C5042
0.01 16V Y
Q5010-2
M5218AL
C5049
33 50V
JP5001
T9206322
C5041
0.047 F
C5048
1 50V
13.5V
TX9
GND
P-SW
GND
To Local Unit J2008 and SW-B Unit J7051
(See Page 4B-1 and 4J-1)
J5007
P0090621
FAN1
FAN2
To FUN ASSY

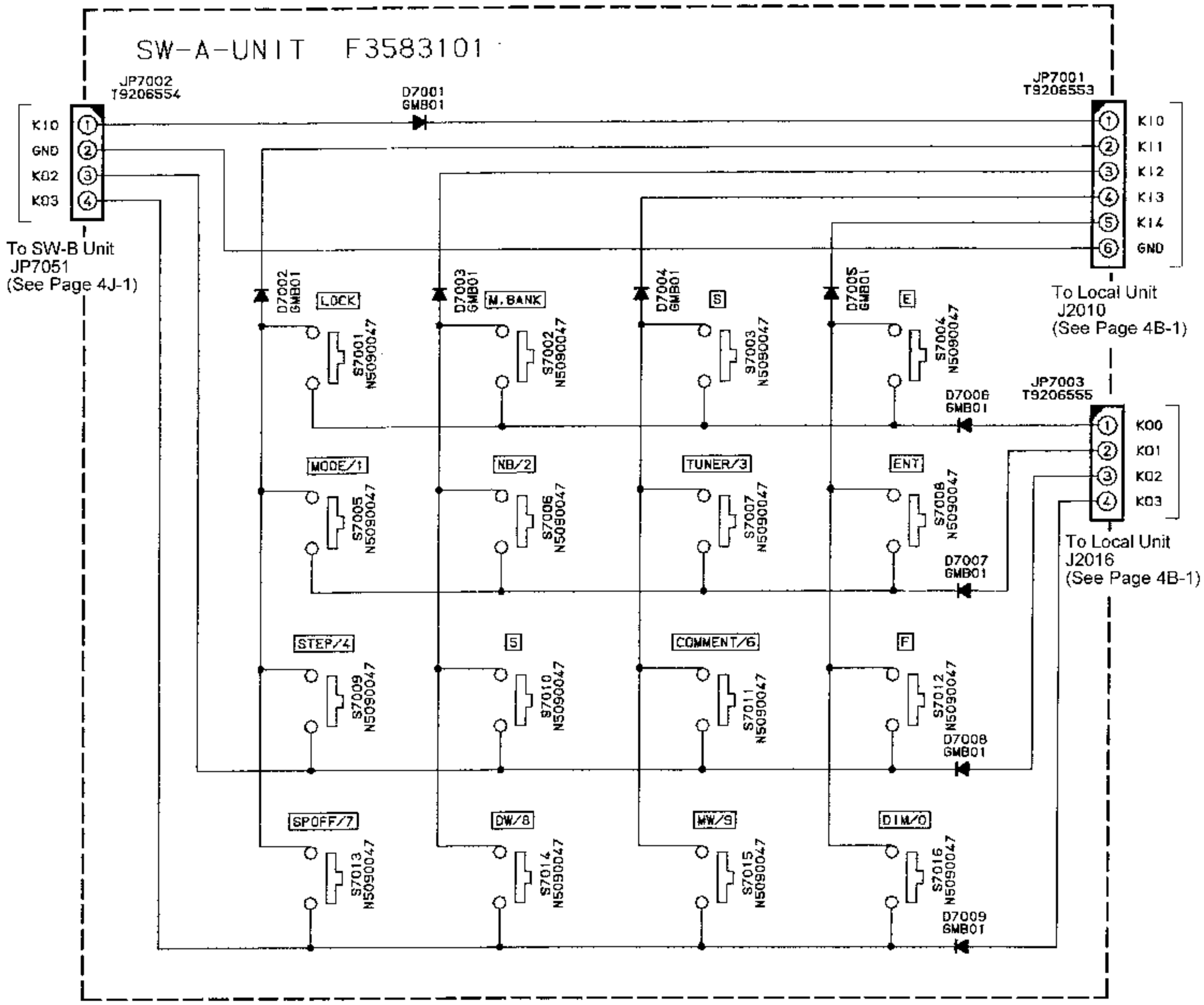


NOTE:
RESISTER VALUES ARE IN Ω.1/6W :
CAPACITOR VALUES ARE IN μF. 50V :
INDUCTOR VALUES ARE IN H
UNLESS OTHERWISE NOTED.

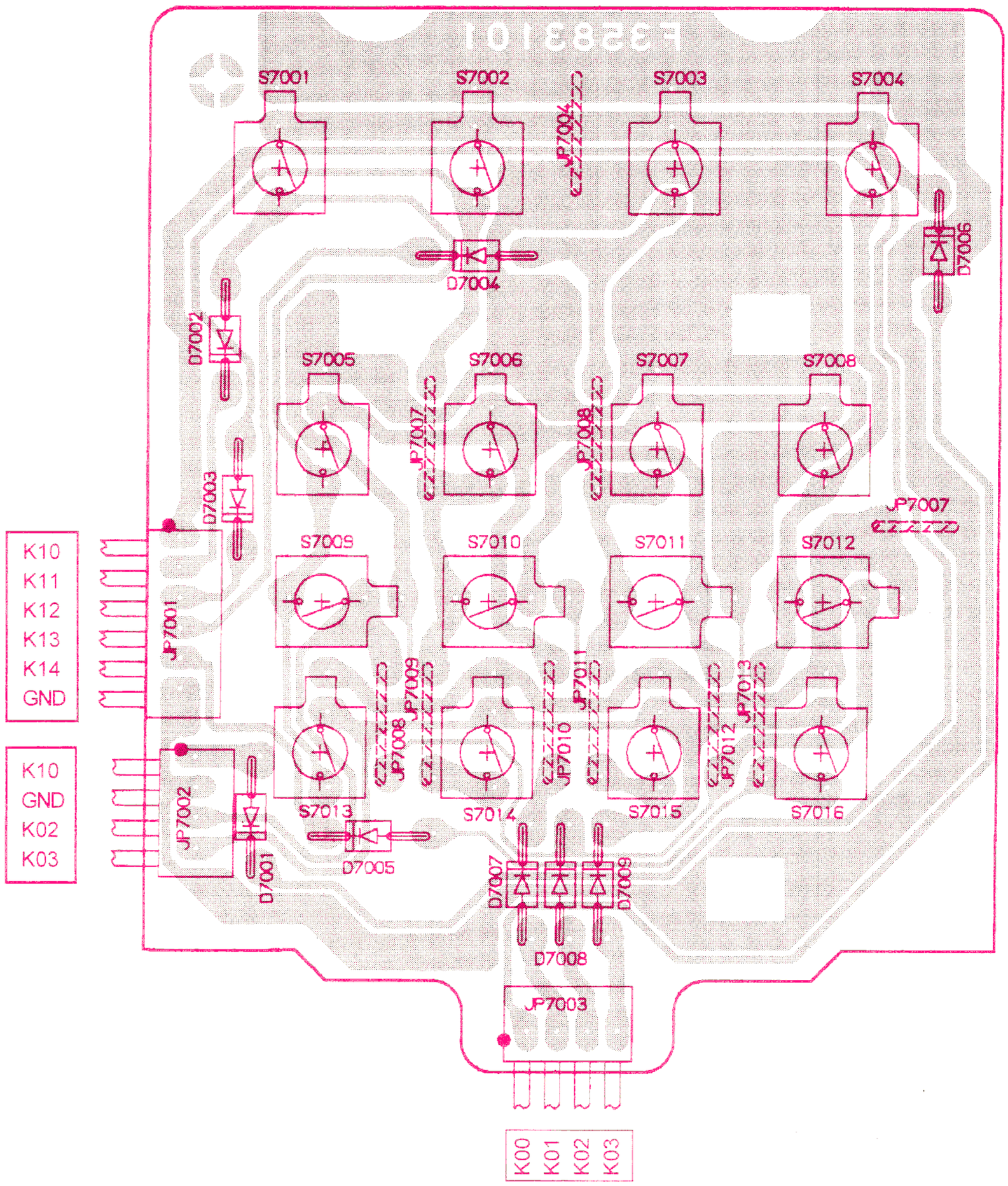
RX(TX)

SW-A Unit

Circuit Diagram

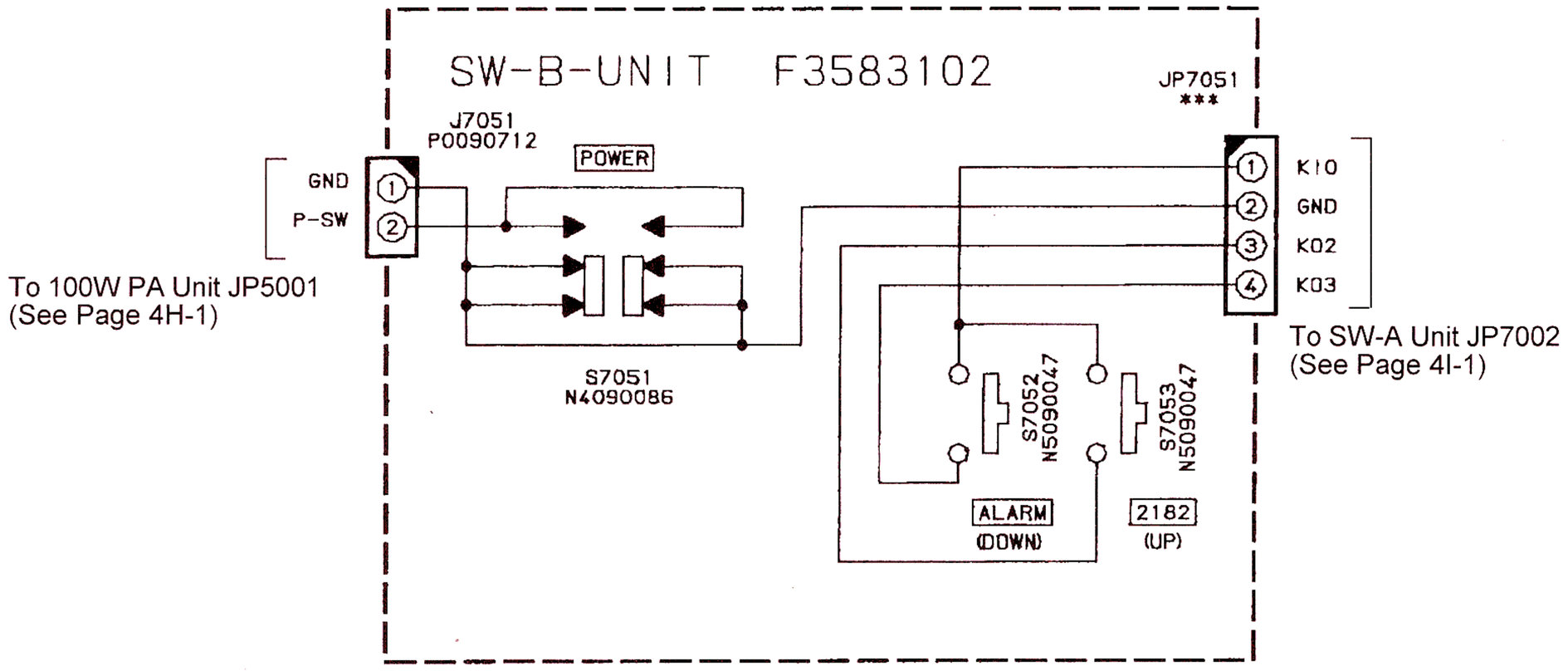


Parts Layout

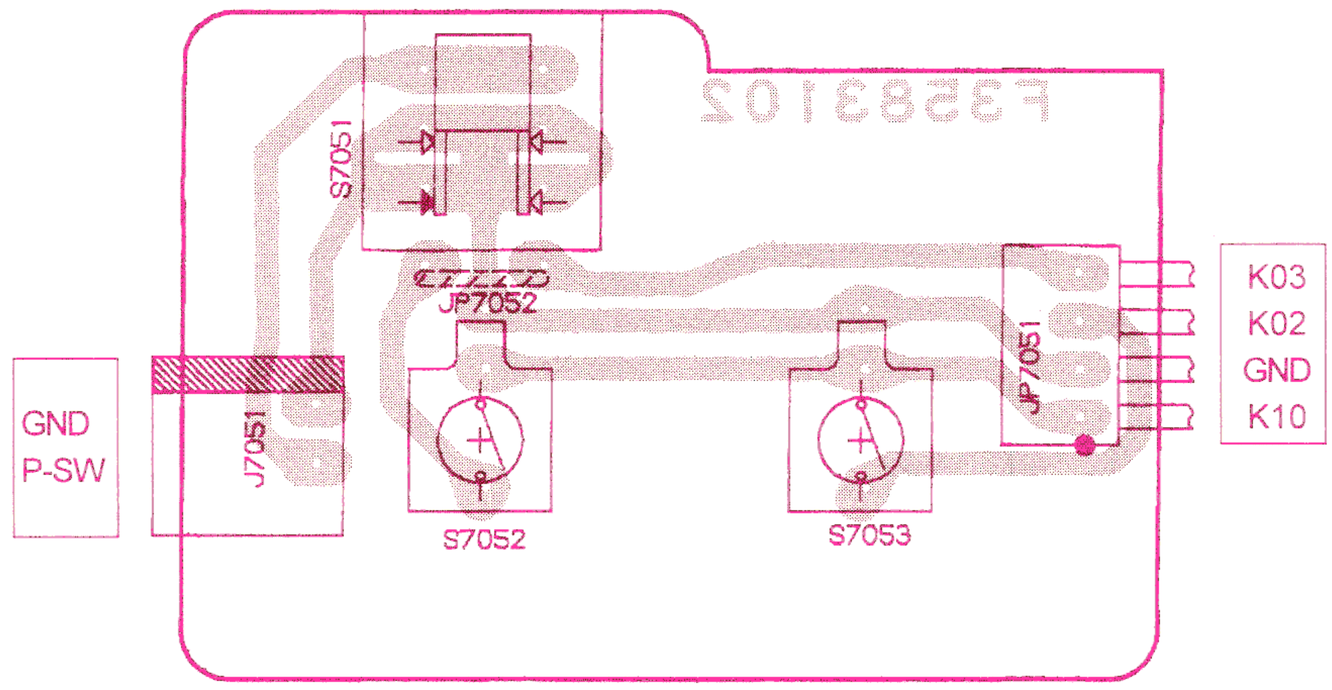


Component Side

Circuit Diagram



Parts Layout

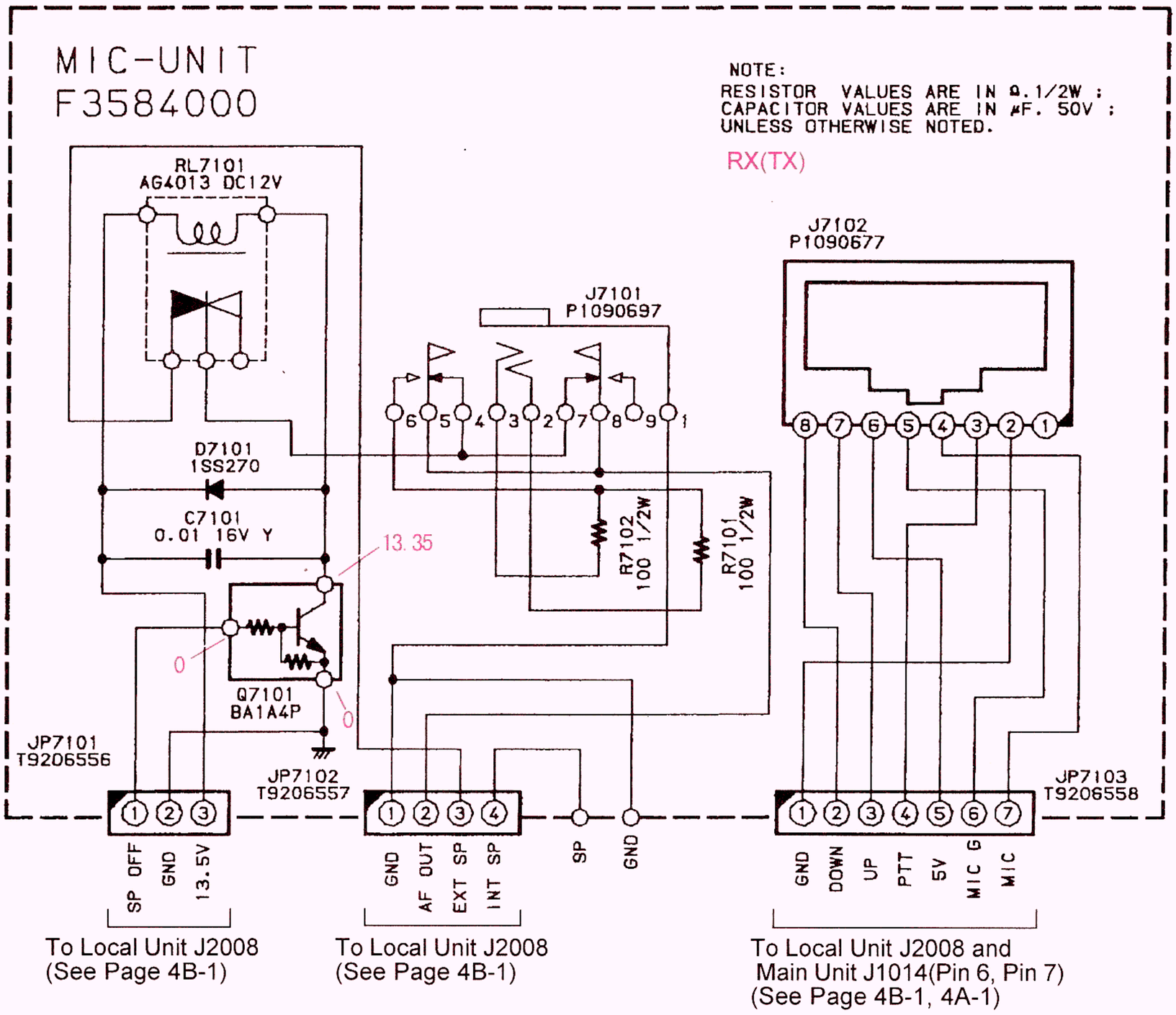


Component Side

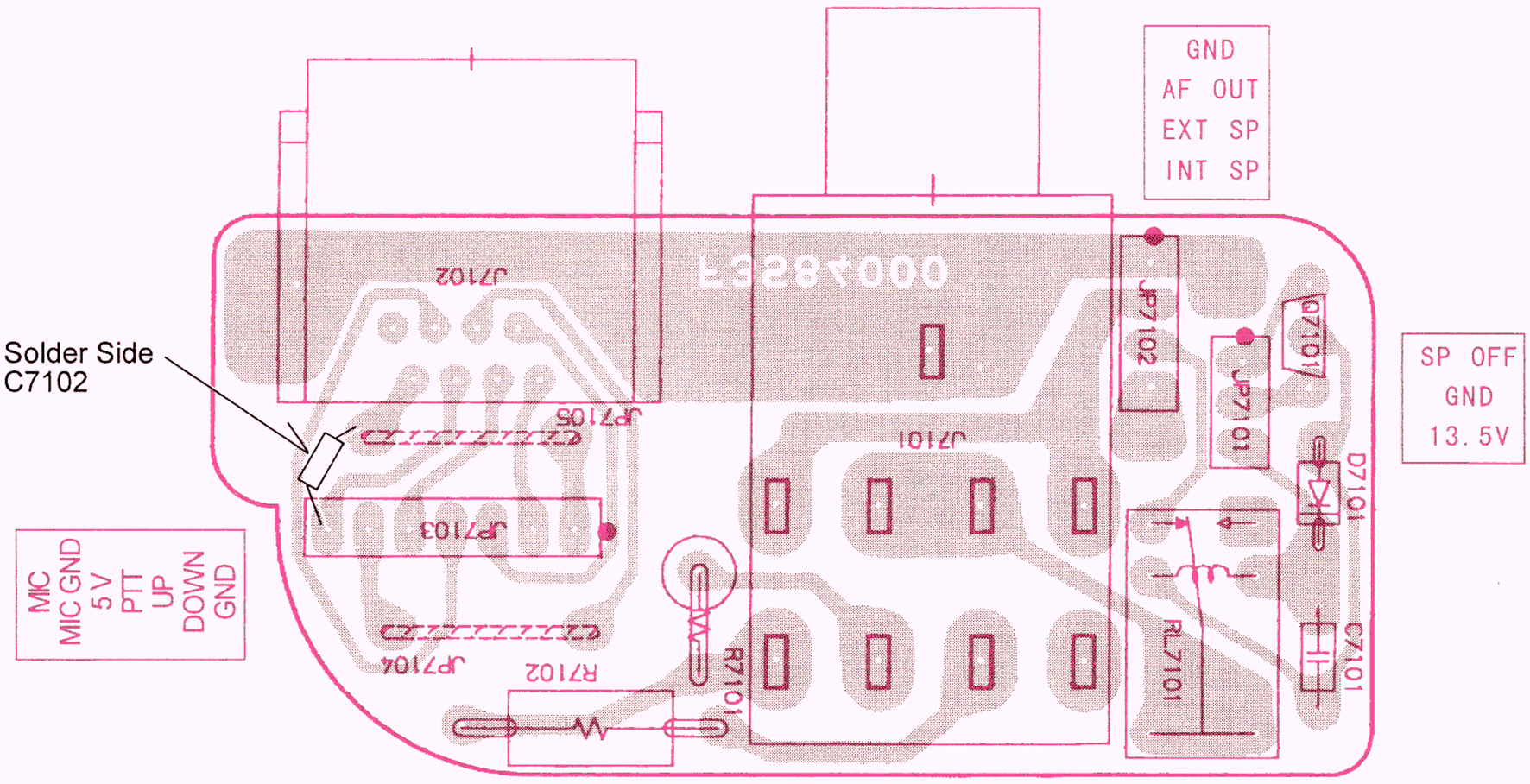
Parts List

REF.	DESCRIPTION	VALUE	WV	TOL.	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
	*** SW-B UNIT ***								
	PCB with Components					CA1530001			
	Printed Circuit Board					F3583102			
J 7051	CONNECTOR				SC25-02WL	P0090712			
S 7051	PUSH SWITCH				SPH121A94	N4090086			
S 7052	TACT SWITCH				EVQ-333 H=9.5	N5090047			
S 7053	TACT SWITCH				EVQ-333 H=9.5	N5090047			

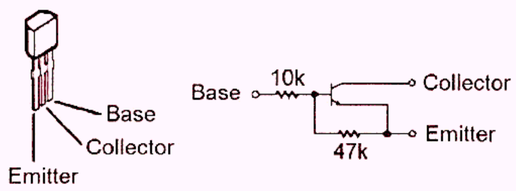
Circuit Diagram



Parts Layout

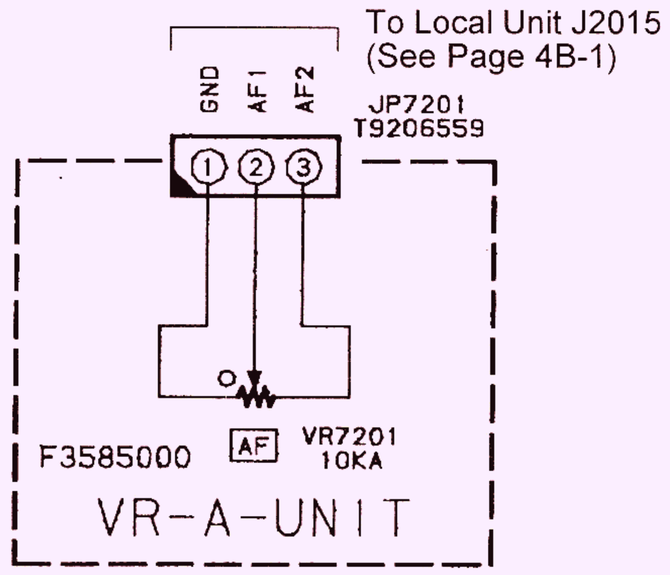


Component Side

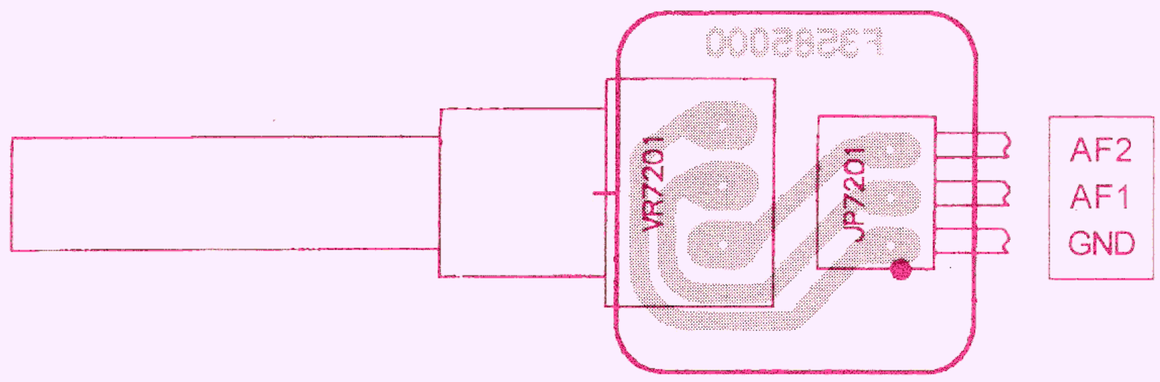


BA1A4P (Q7101)

Circuit Diagram



Parts Layout

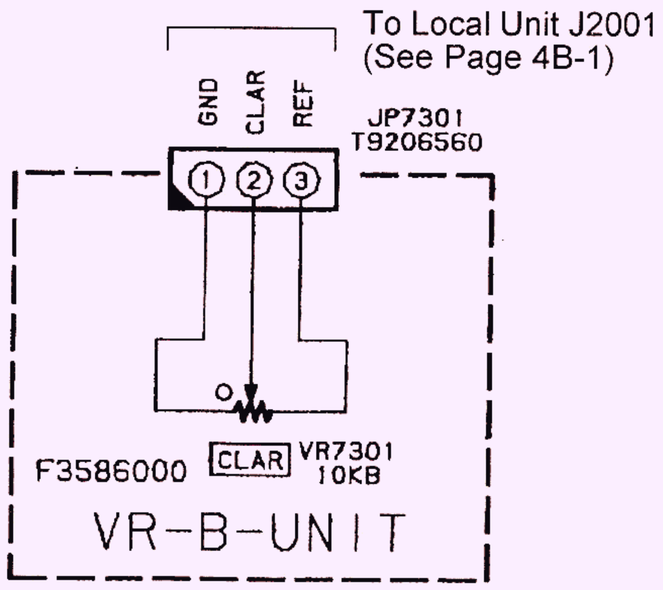


Component Side

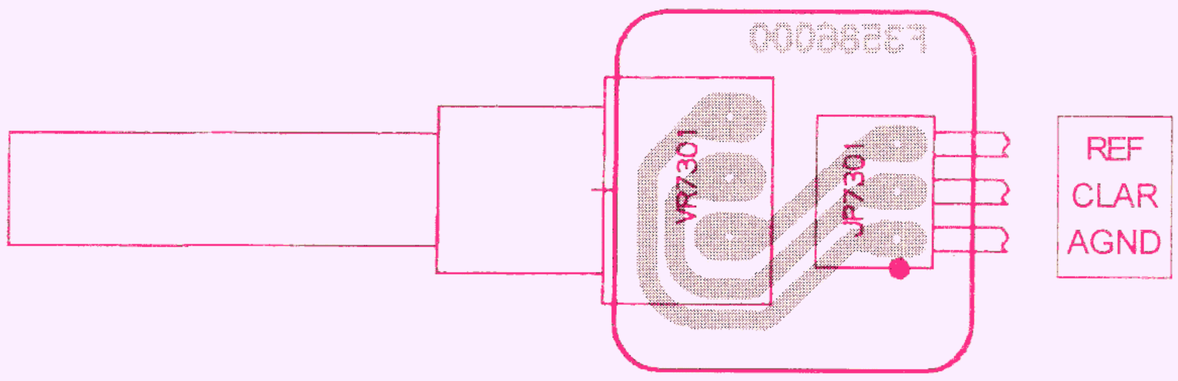
Parts List

REF.	DESCRIPTION	VALUE	WV	TOL.	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
	*** VR-A UNIT ***								
	PCB with Components					CA1494001			
	Printed Circuit Board					F3585000			
JP7201	WIRE ASSY					T9206559			
VR7201	POT.	10KA			RK09711100TGA 10KA	J60800205			

Circuit Diagram



Parts Layout

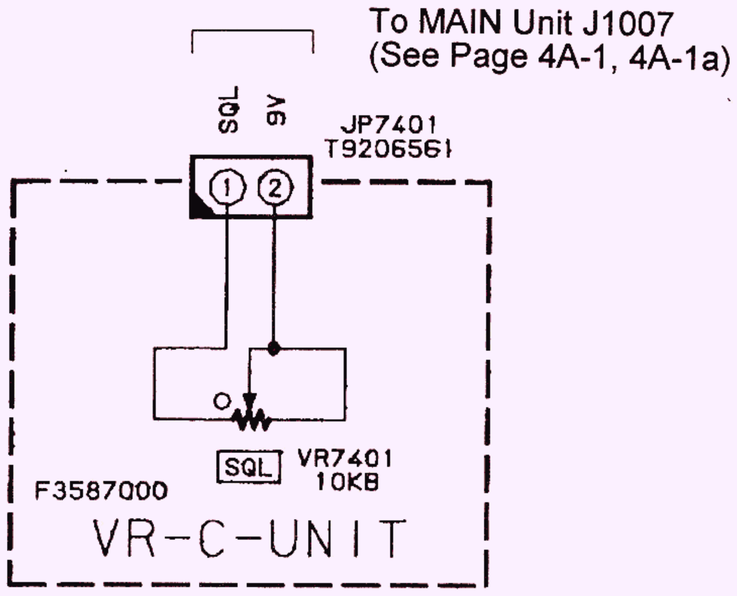


Component Side

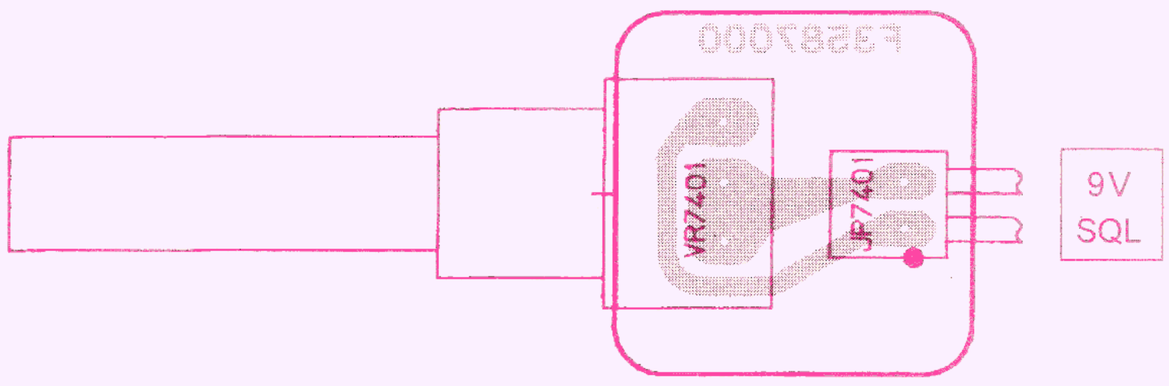
Parts List

REF.	DESCRIPTION	VALUE	WV	TOL.	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
	*** VR -B UNIT ***								
	PCB with Components					CA1495001			
	Printed Circuit Board					F3586000			
JP7301	WIRE ASSY					T9206560			
VR7301	POT.	10KB			RK0971110D62A 10KB	J60800195			

Circuit Diagram



Parts Layout

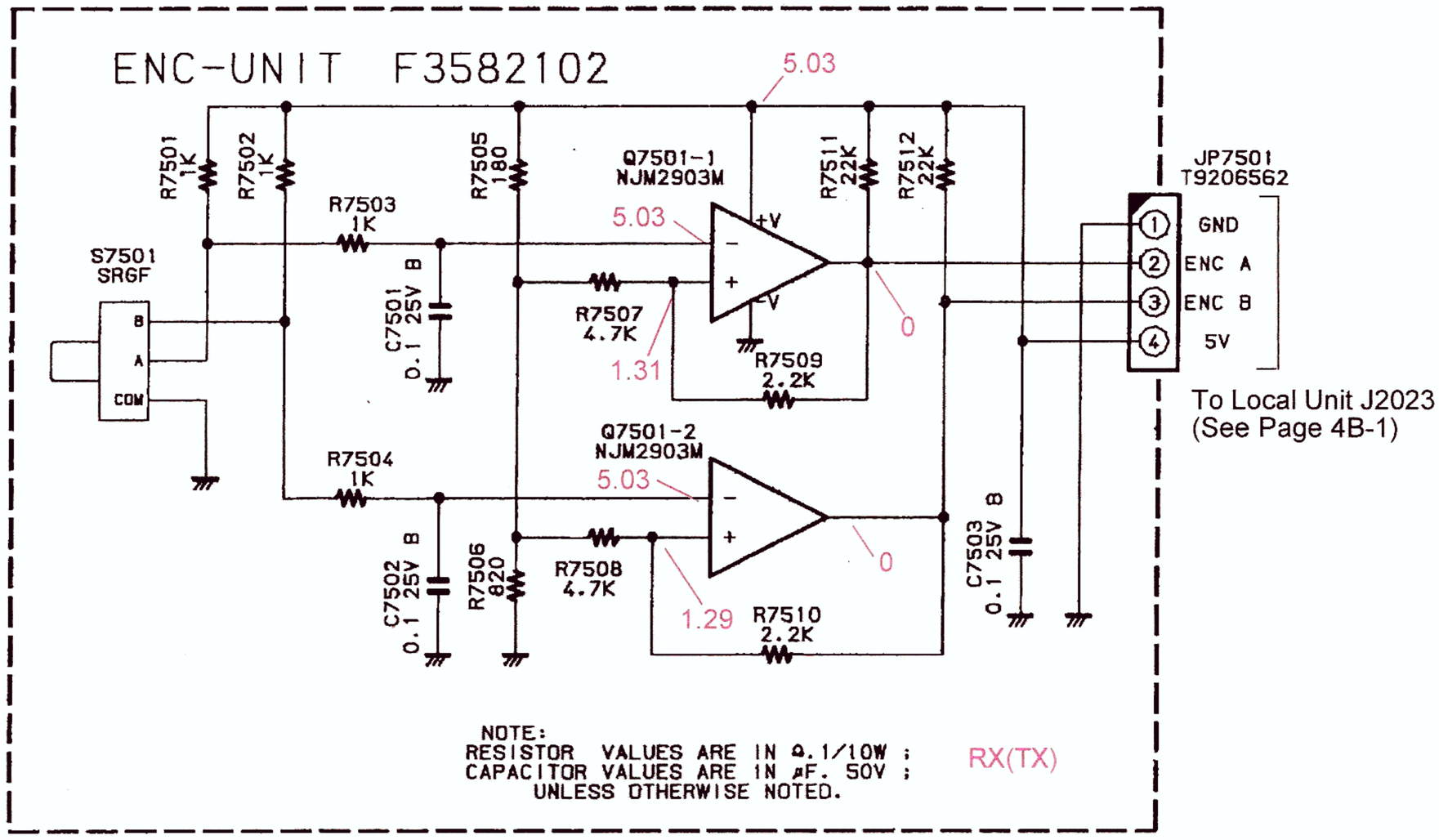


Component Side

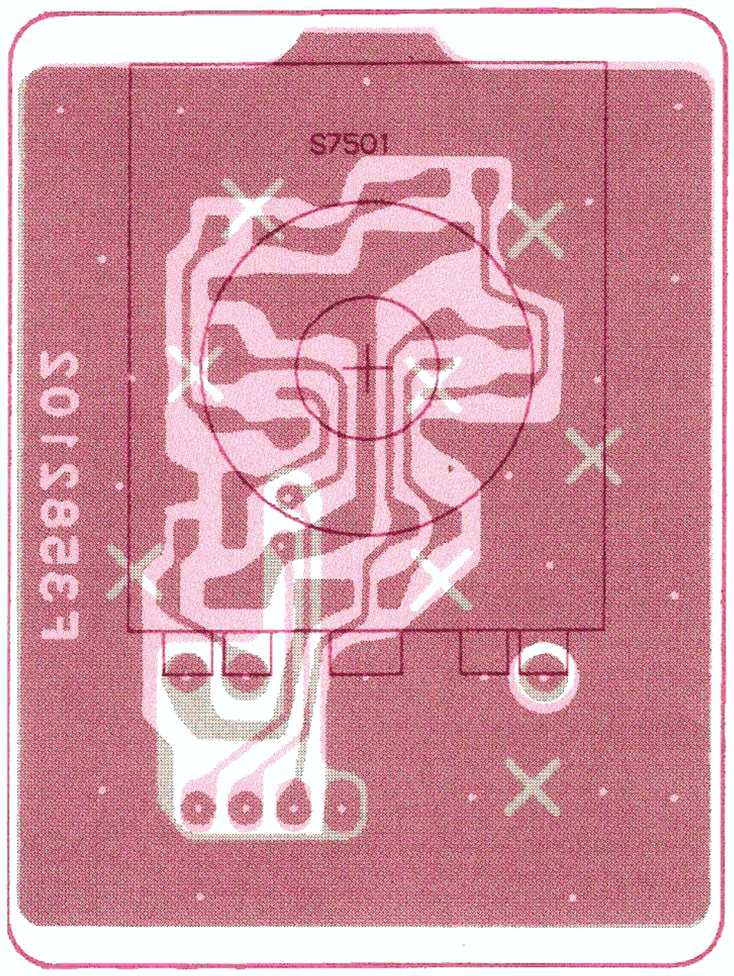
Parts List

REF.	DESCRIPTION	VALUE	WV	TOL.	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
			*** VR-C UNIT ***						
	PCB with Components					CA1496001			
	Printed Circuit Board					F3587000			
JP7401	WIRE ASSY					T9206561			
VR7401	POT.	10KB			RK09711100THA 10KB	J60800196			

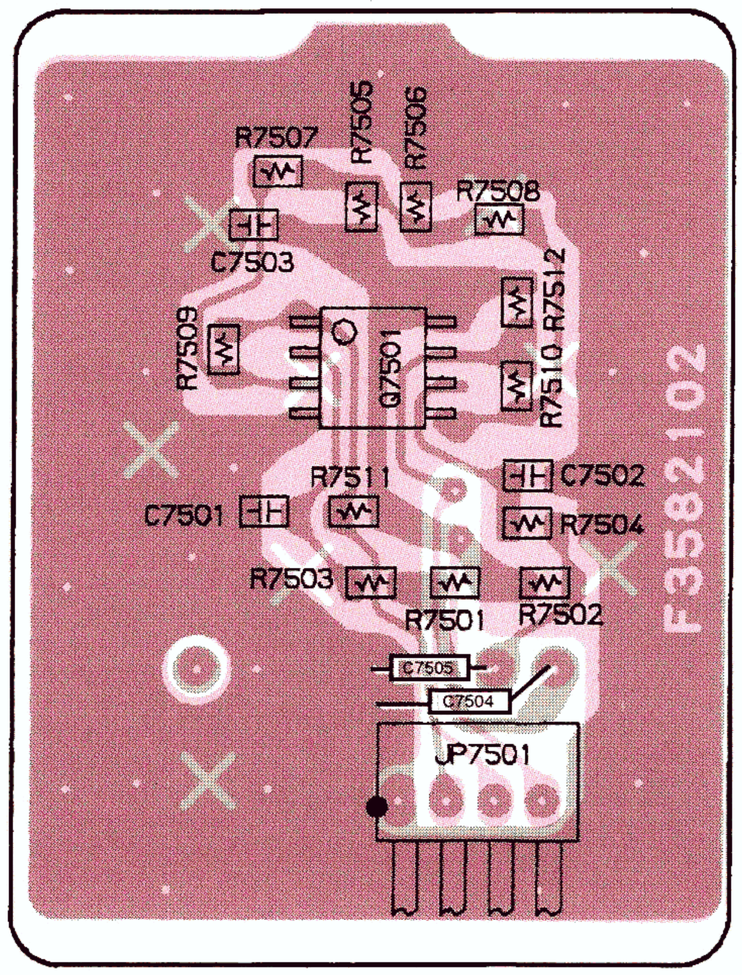
Circuit Diagram



Parts Layout



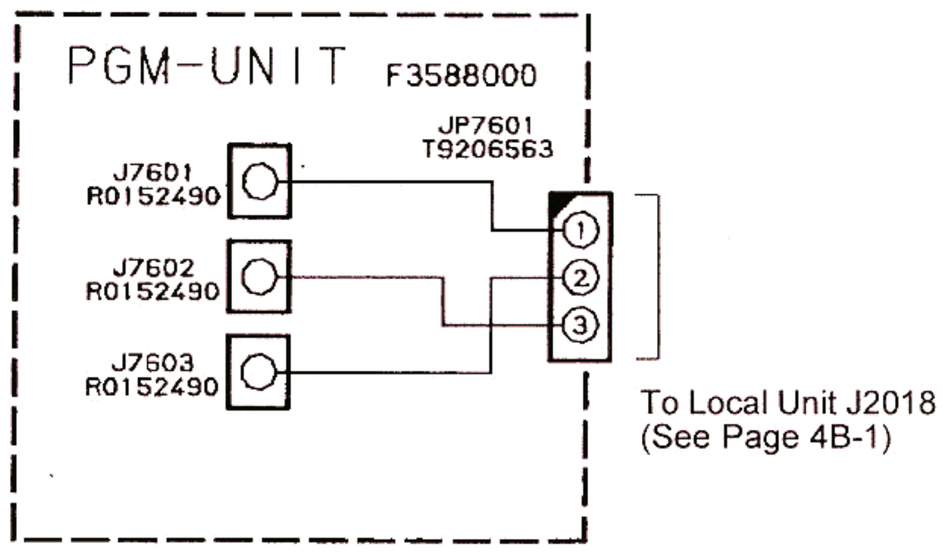
Component Side



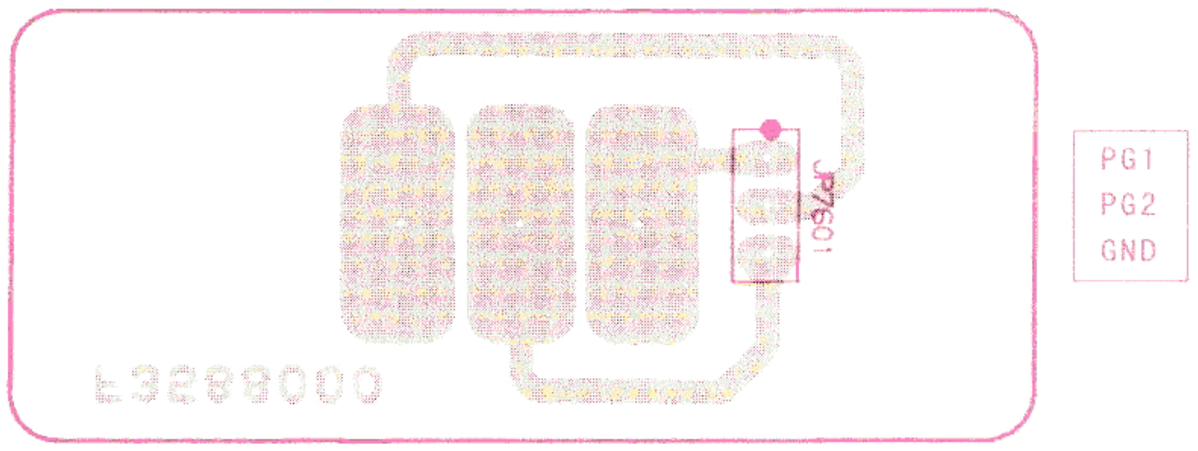
GND
ENC A
ENC B
5V

Chip Side

Circuit Diagram



Parts Layout

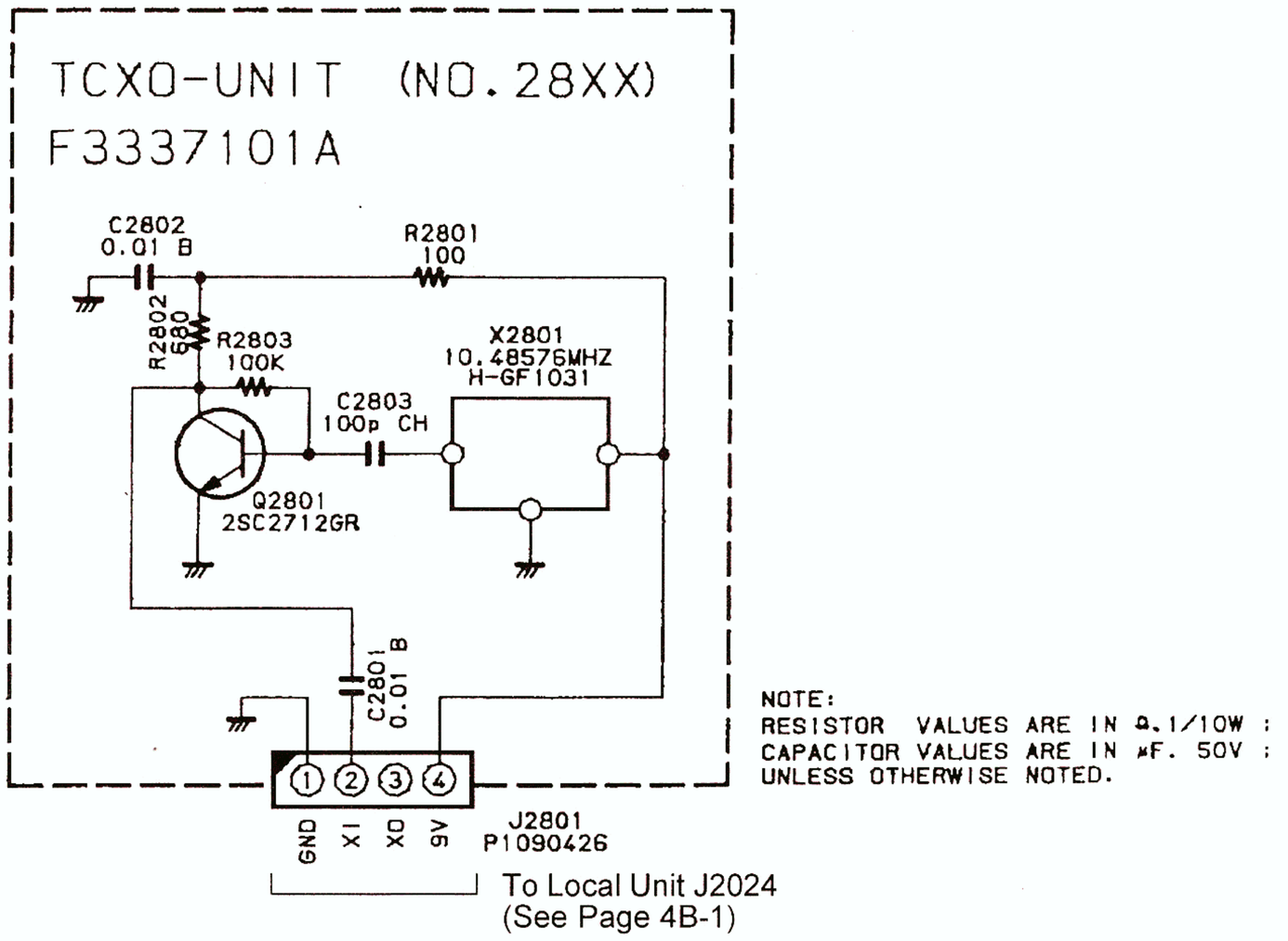


Component Side

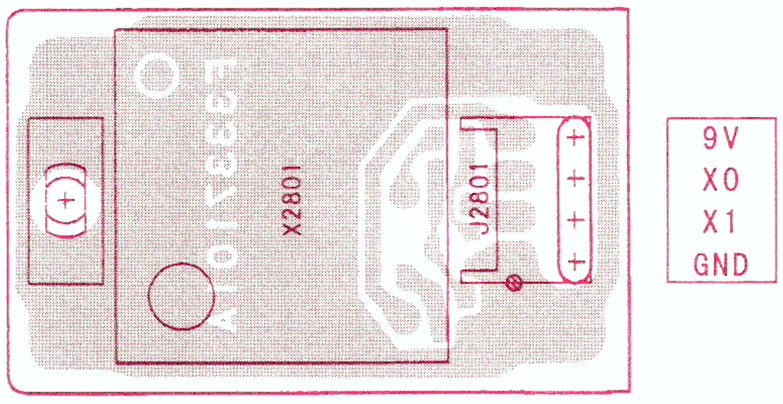
Parts List

REF.	DESCRIPTION	VALUE	WV	TOL.	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
	*** PGM UNIT ***								
	PCB with Components					CA1528001			
	Printed Circuit Board					F3588000			
J 7601	SPRING CONNECTOR					R0152490			
J 7602	SPRING CONNECTOR					R0152490			
J 7603	SPRING CONNECTOR					R0152490			
JP7601	WIRE ASSY A0604					T9206563			

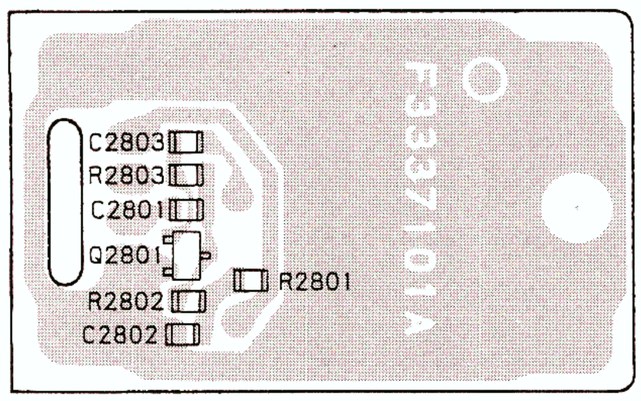
Circuit Diagram



Parts Layout



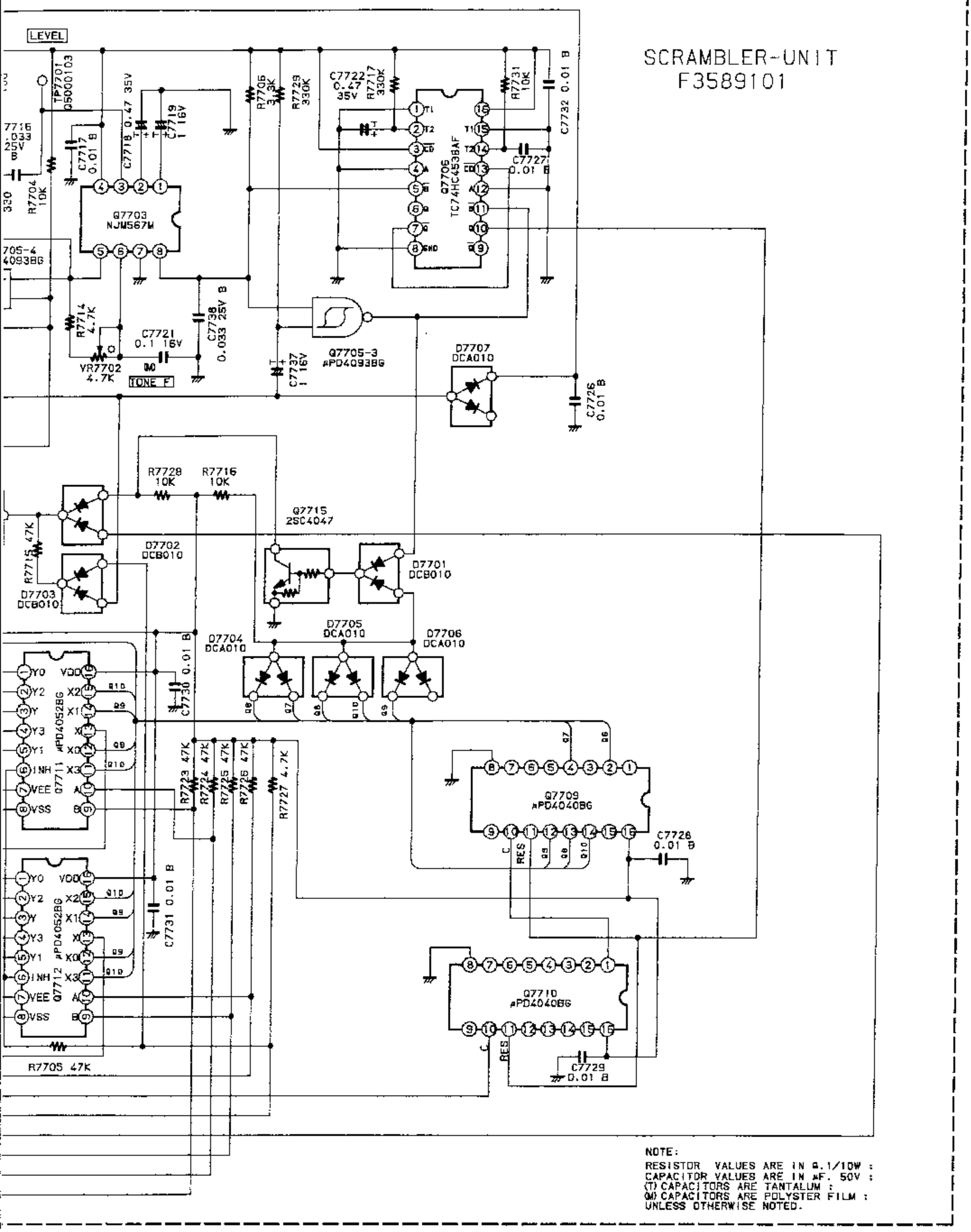
Component Side



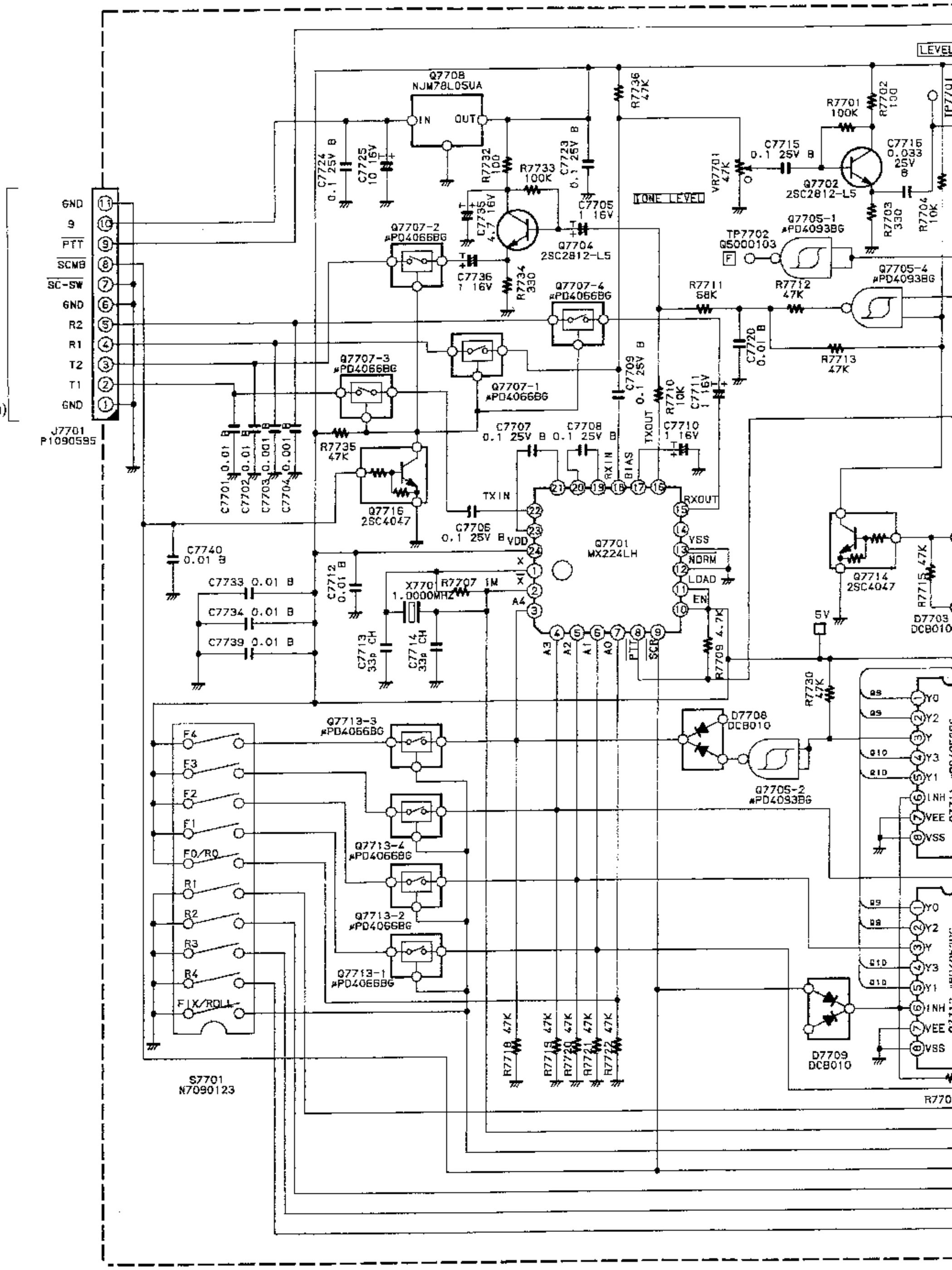
Chip Side

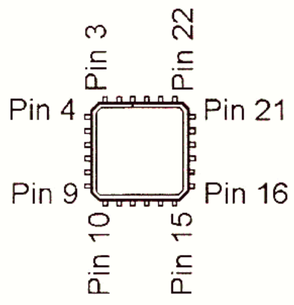
Parts List

REF.	DESCRIPTION	VALUE	WV	TOL.	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
		*** TCX-4 ***							
	Printed Circuit Board					F3337101A			
C 2801	CHIP CAP.	0.01uF	50V	B	GRM40B103M50PT	K22170817			
C 2802	CHIP CAP.	0.01uF	50V	B	GRM40B103M50PT	K22170817			
C 2803	CHIP CAP.	33pF	50V	CH	GRM40CH330J50PT	K22170223			
J 2801	CONNECTOR				5124-04BHPB	P1090426			
Q 2801	TRANSISTOR				2SC2712GR	G3327127G			
R 2801	CHIP RES.	100	1/10W	5%	RMC1/10T 101J	J24205101			
R 2802	CHIP RES.	1K	1/10W	5%	RMC1/10T 102J	J24205102			
R 2803	CHIP RES.	100K	1/10W	5%	RMC1/10T 104J	J24205104			
X 2801	XTAL	10.48576MHz				GF-1031	H9500140		

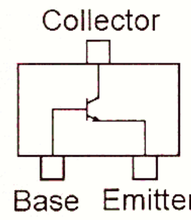

SCRAMBLER-UNIT
F3589101
LEVEL
TP7701
Q5000103
C7716
0.033
25V B
R7704
10K
C7717
0.01 B
C7718 0.47 35V T
C7719
1 16V T
R7706
3.3K
R7729
330K
C7722
0.47
35V T
R7717
330K
C7732 0.01 B
R7731
10K
C7727
0.01 B
Q7706
TC74HC4538AF
Q7703
NJM567M
Q7705-4
μPD4093BG
R7714
4.7K
C7721
0.1 16V
C7738
0.033 25V B
YR7702
4.7K
TONE F
Q7705-3
μPD4093BG
C7737
1 16V T
D7707
DCA010
C7726
0.01 B
R7728
10K
R7716
10K
Q7715
2SC4047
R7715 47K
D7702
DCB010
D7703
DCB010
D7701
DCB010
D7705
DCA010
D7704
DCA010
D7706
DCA010
C7730 0.01 B
Q7711 μPD4052BG
Q7712 μPD4052BG
R7723 47K
R7724 47K
R7725 47K
R7726 47K
R7727 4.7K
C7731 0.01 B
R7705 47K
Q7709
μPD4040BG
C7728
0.01 B
Q7710
μPD4040BG
C7729
0.01 B
NOTE:
RESISTOR VALUES ARE IN Ω.1/10W :
CAPACITOR VALUES ARE IN μF. 50V :
(T) CAPACITORS ARE TANTALUM :
(M) CAPACITORS ARE POLYSTER FILM :
UNLESS OTHERWISE NOTED.

Circuit Diagram

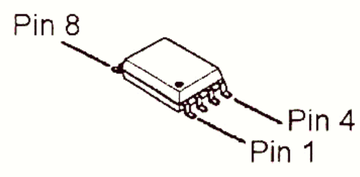




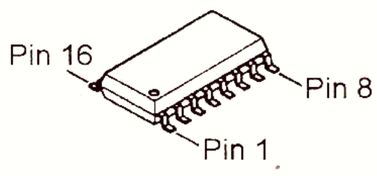
MX224LH
(Q7701)



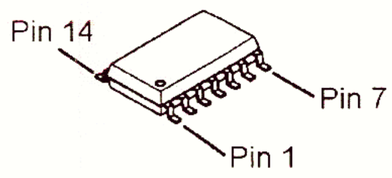
2SC2812 (L5)
(Q7702, 7704)



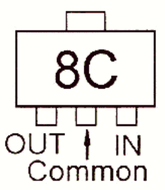
NJM567M
(Q7703)



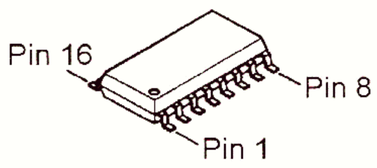
TC74HC4538AF
(Q7706)
µPD4040BG
(Q7709, 7710)



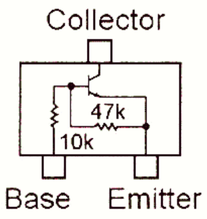
µPD4093BG
(Q7705)
µPD4066BG
(Q7707, 7713)



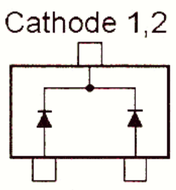
NJM78L05UA (8C)
(Q7708)



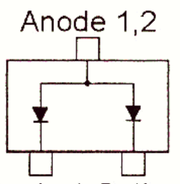
µPD4052BG
(Q7711, 7712)



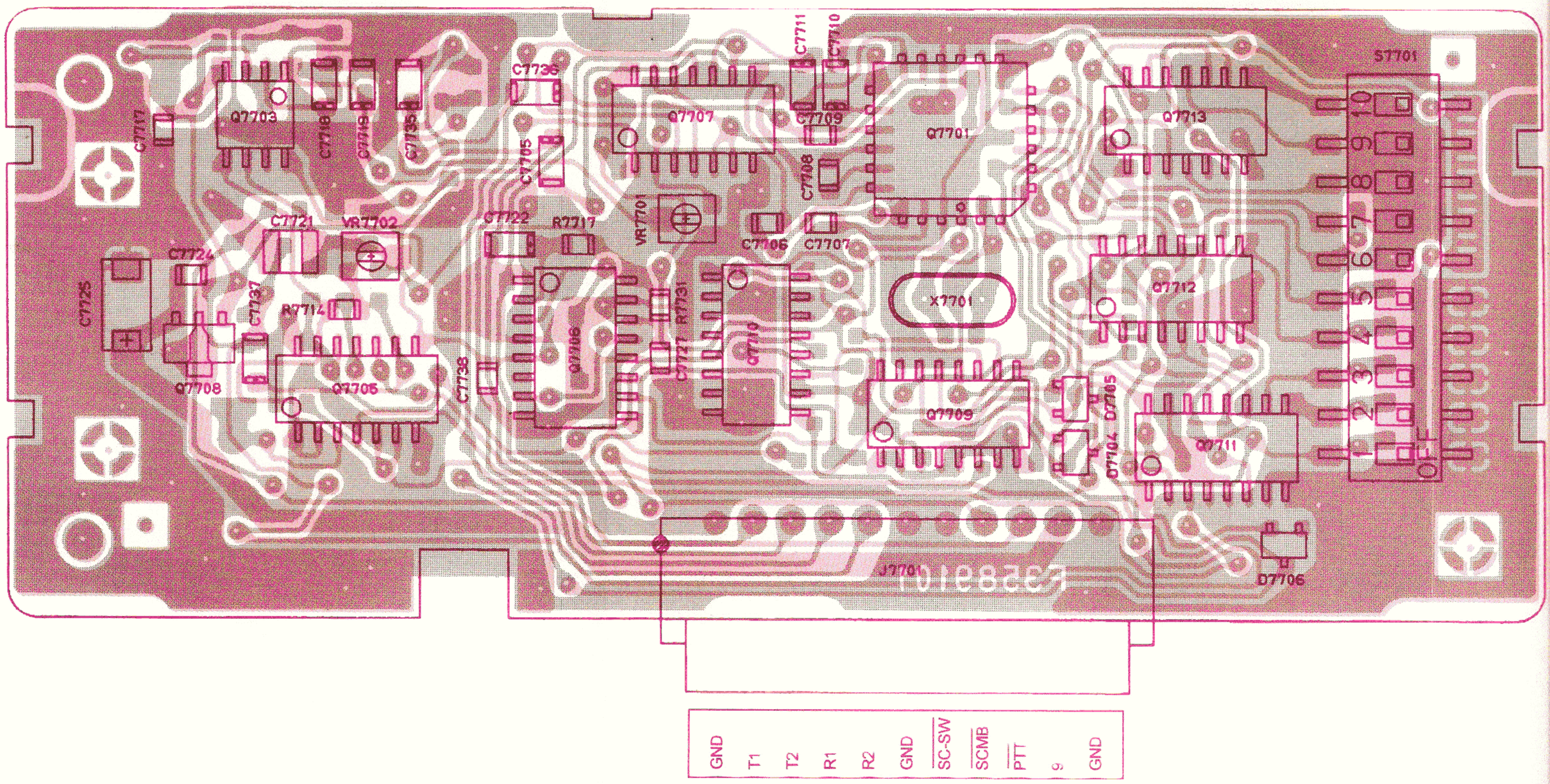
2SC4047 (ZY)
(Q7714, 7715, 7716)



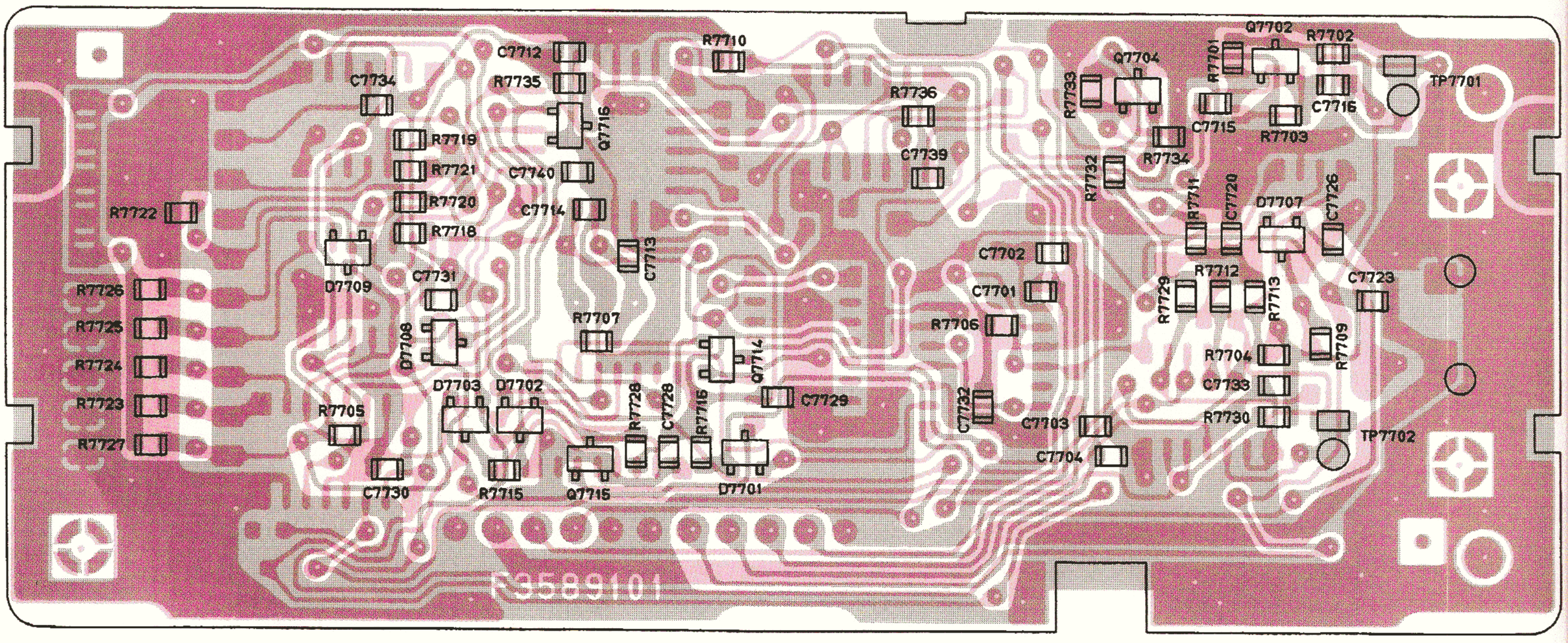
DCB010 (W6)
(D7701, 7702, 7703, 7708, 7709)



DCA010 (W5)
(D7704, 7705, 7706, 7707)



Component Side



Chip Side