Low Voltage, 2.4Ω Quad SPST Switch

FEATURES

- ±1.08V to ±2.75V dual supply
- +1.08V to +5.5V single supply
- Low on resistance 2.4Ω
- 16-lead, 2mm × 2mm LGA
- 1.8 V and 3 V JEDEC compliant logic
- Fully specified at ±5V,+3.3V, +1.8V, and ±2.5V
- Rail-to-rail signal range
- −40 °C to +125 °C operating temperature range

APPLICATIONS

- Automated test equipment
- Data acquisition systems
- Medical equipment
- FPGA and microcontroller systems
- Audio and video signal routing
- Communications systems
- Relay replacement

GENERAL DESCRIPTION

The ADG1712 contains four independent single-pole/single-throw (SPST) switches and operates with a low-voltage single supply range from +1.08V to + 5.5V or a low-voltage dual supply range from ±1.08V to ±2.75V.

The ADG1712 is designed for small size without compromising on performance. The 2mm × 2mm land grid array (LGA) package is ideal for a broad range of applications where area is a concern.

The ADG1712 has a low on resistance of just 2.4Ω and a rail-to-rail input signal range. Each switch conducts equally well in both directions when on. The switches are turned on with a Logic 1 input on the corresponding digital control line, and the digital control inputs are 1.8V and 3V JEDEC compliant for ease of use with microcontrollers and field programmable gate arrays (FPGAs).

FUNCTIONAL BLOCK DIAGRAM

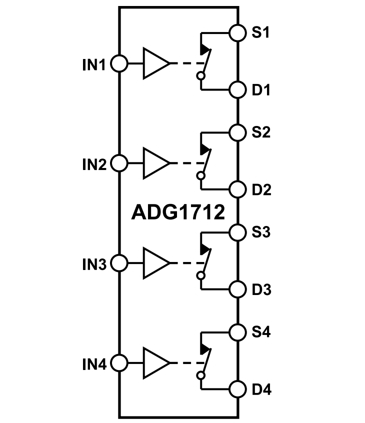

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

1. 1.08V to 5.5V wide supply range
2. Low on-resistance of 2.4Ω
3. JEDEC standard compliant for both 1.8V and 3V logic levels.
4. 16-lead, 2mm × 2mm LGA.

Rev. 0

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REVISION HISTORY

7/2025—Revision 0: Initial Version

SPECIFICATIONS

OPERATING SUPPLY VOLTAGES

Table 1. Operating Voltage Range

Supply Voltage	Min	Max	Unit
Dual Supply	±1.08	±2.75	V
Single Supply	+1.08	+5.5	V

5V SINGLE SUPPLY

V_{DD} = 5V ± 10%, V_{SS} = 0V, GND = 0V, V_L = 1.65V to 3.6V, unless otherwise noted.

Table 2. +5 V Single-Supply Specifications

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +4.5V, V_{SS} = 0V
Analog Signal Range	V_{SS} to V_{DD}			V	
On Resistance, R_{ON}	2.4			Ω typ	Source voltage (V_S) = 0 to V_{DD}, source current (I_S) = −10mA, see Figure 49
	3.2	3.8	4.2	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.01			Ω typ	V_S = 0 to V_{DD}, I_S = −10mA
	0.1	0.11	0.3	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.56			Ω typ	V_S = 0 to V_{DD}, I_S = −10mA
	1.0	1.0	1.0	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 4.5V/1V, drain voltage (V_D) = 1V/4.5V, see Figure 50
	±0.54	±2.1	±5.7	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 4.5V/1V, V_D = 1 V/4.5V, see Figure 50
	±0.54	±2.1	±5.7	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1V or 4.5V, see Figure 51
	±0.04	±0.06	±0.3	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	V_L = 1.65V to 1.95V
Input Low Voltage, V_{INL}			0.35 × V_L	V max	V_L = 1.65V to 1.95V
Input High Voltage, V_{INH}			2.0	V min	V_L = 2.7V to 3.6V
Input Low Voltage, V_{INL}			0.8	V max	V_L = 2.7V to 3.6V
Input Current, I_{INH} or I_{INL}	0.02			μA typ	V_{INx} = 0V or V_L
			0.8	μA max	
Digital-Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	21			ns typ	Load resistance (R_L) = 300Ω, load capacitance (C_L) = 35pF , V_S = 3V, V_L = 1.8V, see Figure 56
	26	27	27	ns max	
Off Time, t_{OFF}	52			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 3V V_L = 1.8V, see Figure 56
	64	65	65	ns max	
Charge Injection, Q_{INJ}	3			pC typ	V_S = 2.5V, R_S = 0Ω, C_L = 1nF, V_L = 1.8V, see Figure 57
Off Isolation	−68			dB typ	R_L = 50Ω, C_L = 5pF, frequency (f) = 1MHz, see Figure 52
	−48			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz
Channel-to-Channel Crosstalk	−118			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 53
	−103			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz
Total Harmonic Distortion, THD	−93			dB typ	R_L = 10kΩ, 3V p-p, f = 20kHz, see Figure 55

SPECIFICATIONS

Table 2. +5 V Single-Supply Specifications (Continued)

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
	−91			dB typ	R_L = 10kΩ, 3V p-p, f = 100kHz, see Figure 55
	−87			dB typ	R_L = 10kΩ, 3V p-p, f = 200kHz, see Figure 55
Total Harmonic Distortion + Noise, THD + N	0.0026			% typ	R_L = 10kΩ, 3V p-p, f = 20Hz to 20kHz, see Figure 55
−3dB Bandwidth	410			MHz typ	R_L = 50Ω, C_L = 5pF, see Figure 54
Insertion Loss	−0.1			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 54
Source Off Capacitance, C_S (Off)	6			pF typ	V_S = 2.5V, f = 1MHz
Drain Off Capacitance, C_D (Off)	6			pF typ	V_S = 2.5V, f = 1MHz
Drain On Capacitance, C_D (On), Source On Capacitance, C_S (On)	12			pF typ	V_S = 2.5V, f = 1MHz
POWER REQUIREMENTS					V_{DD} = +5.5V, V_{SS} = 0V, V_L = 1.8V
Positive Supply Current, I_{DD}	1.0			µA typ	Digital inputs = 0V or V_L V
	1.4	1.62	1.62	µA max	
Negative Supply Current, I_{SS}	0.64			nA typ	Digital inputs = 0V or V_L V
	1.8	11	91	nA max	
Digital Supply Current, I_L	0.05			nA typ	Digital inputs = 0V or V_L V
	1.5	3.0	20	nA max	

+3V SINGLE SUPPLY

V_{DD} = +2.7V to 3.6V, V_{SS} = 0V, GND = 0V, V_L = 1.65V to 3.6V, unless otherwise noted.

Table 3. +3V Single-Supply Specifications

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 2.7V, V_{SS} = 0V
Analog Signal Range	V_{SS} to V_{DD}			V	
On Resistance, R_{ON}	3.9			Ω typ	V_S = 0 to V_{DD}, I_S = −10mA, see Figure 49
	6.8	7.6	8.0	max	
On-Resistance Match Between Channels, ΔR_{ON}	0.02			Ω typ	V_S = 0 to V_{DD} = −10mA
	0.12	0.14	0.3	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.1			Ω typ	V_S = 0 to V_{DD} = −10mA
	2.1	2.3	2.4	Ω max	
LEAKAGE CURRENTS					V_{DD} = 3.6V, V_{SS} = 0V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 3.3V/1 V, V_D = 1V/3.3V, see Figure 50
	±0.032	±0.08	±0.5	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 3.3V/1V, V_D = 1V/3.3V, see Figure 50
	±0.032	±0.08	±0.5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 3.3V or 1V, see Figure 51
	±0.04	±0.05	±0.27	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	V_L = 1.65V to 1.95V
Input Low Voltage, V_{INL}			0.35 × V_L	V max	V_L = 1.65V to 1.95V
Input High Voltage, V_{INH}			2.0	V min	V_L = 2.7V to 3.6V
Input Low Voltage, V_{INL}			0.8	V max	V_L = 2.7V to 3.6V
Input High Current, I_{INH} or $_{INL}$	0.02			µA typ	V_{INx} = 0V or V_L
			0.8	µA max	
Digital-Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					

SPECIFICATIONS

Table 3. +3V Single-Supply Specifications (Continued)

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
On Time, t_{ON}	23			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V, V_L = 1.8V, see Figure 56
	28	30	30	ns max	
Off Time, t_{OFF}	51			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V, V_L = 1.8V, see Figure 56
	63	65	65	ns max	
Charge Injection, Q_{INJ}	1.5			pC typ	V_S = 1.5V, R_S = 0 Ω, C_L = 1nF, V_L = 1.8V, see Figure 57
Off Isolation	−68			dB typ	R_L = 50Ω, C_L = 5pF, frequency (f) = 1MHz, see Figure 52
	−48				R_L = 50Ω, C_L = 5pF, f = 10MHz
Channel-to-Channel Crosstalk	−118			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 53
	−103			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz
Total Harmonic Distortion, THD	−87			dB typ	R_L = 10kΩ, 1.5V p-p, f = 20kHz, see Figure 55
	−86			dB typ	R_L = 10kΩ, 1.5V p-p, f = 100kHz, see Figure 55
	−83			dB typ	R_L = 10kΩ, 1.5V p-p, f = 200kHz, see Figure 55
Total Harmonic Distortion + Noise, THD + N	0.005			% typ	R_L = 10kΩ, 1.5V p-p, f = 20Hz to 20kHz, see Figure 55
−3dB Bandwidth	535			MHz typ	R_L = 50Ω, C_L = 5pF, see Figure 54
Insertion Loss	−0.3			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 54
Source Off Capacitance, C_S (Off)	6			pF typ	V_S = 1.5V, f = 1MHz
Drain Off Capacitance, C_D (Off)	6			pF typ	V_S = 1.5V, f = 1MHz
Drain On Capacitance, C_D (On), Source On Capacitance, C_S (On)	12			pF typ	V_S = 1.5V, f = 1MHz
POWER REQUIREMENTS					V_{DD} = 3.6V, V_{SS} = 0V, V_L = 1.8V
Positive Supply Current, I_{DD}	0.17			μA typ	Digital inputs = 0V or V_L V
	0.26	0.31	0.31	μA max	
Negative Supply Current, I_{SS}	0.64			nA typ	Digital inputs = 0V or V_L V
	1.8	11	91	nA max	
Digital Supply Current, I_L	0.05			nA typ	Digital inputs = 0V or V_L V
	1.5	3.0	20	nA max	

+1.8V SINGLE SUPPLY

V_{DD} = 1.71V to 1.95V, V_{SS} = 0V, GND = 0V, V_L = 1.65V to 3.6V, unless otherwise noted.

Table 4. +1.8V Single-Supply Specifications

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 1.71V, V_{SS} = 0V
Analog Signal Range	V_{SS} to V_{DD}			V	
On Resistance, R_{ON}	19.2			Ω typ	V_S = 0 to V_{DD}, I_S = −10mA, see Figure 49
	63	77	77	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.16			Ω typ	V_S = 0 to V_{DD} = −10mA
	0.8	0.95	0.95	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	14.5			Ω typ	V_S = 0 to V_{DD} = −10mA
	56	72	72	Ω max	
LEAKAGE CURRENTS					V_{DD} = 1.95V, V_{SS} = 0V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 0.6V/1.65V, V_D = 1.65V/0.6 V, see Figure 50
	±0.032	±0.08	±0.5	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 1.65V/0.6V, V_D = 0.6V/1.65 V, see Figure 50
	±0.032	±0.08	±0.5	nA max	

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Table 4. +1.8V Single-Supply Specifications (Continued)

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	$V_S = V_D$ = 0.6V or 1.65V, see Figure 51
	±0.04	±0.05	±0.27	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	V_L = 1.65V to 1.95V
Input Low Voltage, V_{INL}			0.35 × V_L	V max	V_L = 1.65V to 1.95V
Input High Voltage, V_{INH}			2.0	V min	V_L = 2.7V to 3.6V
Input Low Voltage, V_{INL}			0.8	V max	V_L = 2.7V to 3.6V
Input High Current, I_{INH} or $_{INL}$	0.02			μA typ	V_{INx} = 0V or V_L
			0.8	μA max	
Digital-Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	38			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1V, V_L = 1.8V, see Figure 56
	47	48	48	ns max	
Off Time, t_{OFF}	53			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1V, V_L = 1.8V, see Figure 56
	64	67	67	ns max	
Charge Injection, Q_{INJ}	0.7			pC typ	V_S = 0.9V, R_S = 0Ω, C_L = 1nF, V_L = 1.8V, see Figure 57
Off Isolation	−68			dB typ	R_L = 50Ω, C_L = 5pF, frequency (f) = 1MHz, see Figure 52
	−48				R_L = 50Ω, C_L = 5 pF, f = 10MHz
Channel-to-Channel Crosstalk	−118			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 53
	−103			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz
Total Harmonic Distortion, THD	−66			dB typ	R_L = 10kΩ, 1.5V p-p, f = 20kHz, see Figure 55
	−62			dB typ	R_L = 10kΩ, 1.5V p-p, f = 100kHz, see Figure 55
	−58			dB typ	R_L = 10kΩ, 1.5V p-p, f = 200kHz, see Figure 55
Total Harmonic Distortion + Noise, THD + N	0.05			% typ	R_L = 10kΩ, 1.5V p-p, f = 20Hz to 20kHz, see Figure 55
−3dB Bandwidth	450			MHz typ	R_L = 50Ω, C_L = 5pF, see Figure 54
Insertion Loss	−1.1			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 54
Source Off Capacitance, C_S (Off)	6			pF typ	V_S = 0.9V, f = 1MHz
Drain Off Capacitance, C_D (Off)	6			pF typ	V_S = 0.9V, f = 1MHz
Drain On Capacitance, C_D (On), Source On Capacitance, C_S (On)	12			pF typ	V_S = 0.9V, f = 1MHz
POWER REQUIREMENTS					V_{DD} = 1.95V, V_{SS} = 0V, V_L = 1.8V
Positive Supply Current, I_{DD}	0.01			nA typ	Digital inputs = 0V or V_L V
	0.26	0.31	0.31	μA max	
Negative Supply Current, I_{SS}	0.64			nA typ	Digital inputs = 0V or V_L V
	1.8	11	91	nA max	
Digital Supply Current, I_L	0.05			nA typ	Digital inputs = 0V or V_L V
	1.5	3.0	20	nA max	

±2.5V DUAL SUPPLY

V_{DD} = +2.5V ± 10%, V_{SS} = −2.5V ± 10%, GND = 0V, V_L = 1.65V to 1.95VV, unless otherwise noted.

Table 5. ±2.5 V Dual-Supply Specifications

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +2.25V, V_{SS} = −2.25V
Analog Signal Range	V_{SS} to V_{DD}			V	
On Resistance, R_{ON}	2.4			Ω typ	$V_S = V_{SS}$ to V_{DD}, I_S = −10mA, see Figure 49
	3.2	3.8	4.2	Ω max	

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Table 5. ±2.5 V Dual-Supply Specifications (Continued)

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
On-Resistance Match Between Channels, ΔR_{ON}	0.01			Ω typ	V_S = V_{SS} to V_{DD} = −10mA
	0.1	0.11	0.3	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.56			Ω typ	V_S = V_{SS} to V_{DD} = −10mA
	1.0	1.0	1.0	Ω max	
LEAKAGE CURRENTS					V_{DD} = +2.75V, V_{SS} = −2.75V
Source Off Leakage, I_S (Off)	±0.3			nA typ	V_S = +2.25V/−2.25V, V_D = −2.25V/+2.25V, see Figure 50
	±0.54	±2.1	±5.7	nA max	
Drain Off Leakage, I_D (Off)	±0.3			nA typ	V_S = +2.25 V/−2.25 V, V_D = −2.25V/+2.25V, see Figure 50
	±0.54	±2.1	±5.7	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = −2.25V or +1.25V, see Figure 51
	±0.04	±0.06	±0.3	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	V_L = 1.65V to 1.95V
Input Low Voltage, V_{INL}			0.35 × V_L	V max	V_L = 1.65V to 1.95V
Input High Current, I_{INH} or I_{INL}	0.02			µA typ	V_{INx} = 0V or V_L
			0.8	µA max	
Digital-Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	22			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V,V_L = 1.8V, see Figure 56
	26	27	27	ns max	
Off Time, t_{OFF}	51			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V, V_L = 1.8V, see Figure 56
	63	64	64	ns max	
Charge Injection, Q_{INJ}	3			pC typ	V_S = 0V, R_S = 0Ω, C_L = 1nF, V_L = 1.8V, see Figure 57
Off Isolation	−68			dB typ	R_L = 50Ω, C_L = 5pF, frequency (f) = 1MHz, see Figure 52
	−48				R_L = 50Ω, C_L = 5pF, f = 10MHz
Channel-to-Channel Crosstalk	−118			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 53
	−103			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz
Total Harmonic Distortion, THD	−99			dB typ	R_L = 10kΩ, 3V p-p, f = 20kHz, see Figure 55
	−95			dB typ	R_L = 10kΩ, 3V p-p, f = 100kHz, see Figure 55
	−90			dB typ	R_L = 10kΩ, 3V p-p, f = 200kHz, see Figure 55
Total Harmonic Distortion + Noise, THD + N	0.002			% typ	R_L = 10kΩ, 3V p-p, f = 20Hz to 20kHz, see Figure 55
−3dB Bandwidth	405			MHz typ	R_L = 50Ω, C_L = 5pF, see Figure 54
Insertion Loss	−0.1			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 54
Source Off Capacitance, C_S (Off)	6			pF typ	V_S = 0V, f = 1MHz
Source Off Capacitance, C_D (Off)	6			pF typ	V_S = 0V, f = 1MHz
Drain On Capacitance, C_D (On), Source On Capacitance, C_S (On)	12			pF typ	V_S = 0V, f = 1MHz
POWER REQUIREMENTS					V_{DD} = +2.75V, V_{SS} = −2.75V, V_L = 1.8V
Positive Supply Current, I_{DD}	0.013			µA typ	Digital inputs = 0V or V_L
	0.26	0.31	0.31	µA max	
Negative Supply Current, I_{SS}	0.06			nA typ	Digital inputs = 0V or V_L
	1.9	13	105	nA max	
Digital Supply Current, I_L	0.05			µA typ	Digital inputs = 0V or V_L
	1.5	3.0	20	nA max	

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CONTINUOUS CURRENT PER CHANNEL, SX OR DX

Table 6. One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx[1] (θ_{JA} = 150 °C/W.)				
V_{DD} = +5 V, V_{SS} = 0 V	254	111	44	mA maximum
V_{DD} = +3 V, V_{SS} = 0 V	196	97	43	mA maximum
V_{DD} = 1.8 V, V_{SS} = 0 V	123	73	39	mA maximum
V_{DD} = 2.5 V, V_{SS} = −2.5 V	239	108	44	mA maximum

[1] Sx refer to S1 to S4 pins, and Dx refers to the D1 to D4 pins.

Table 7. Four Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx[1] (θ_{JA} = 150 °C/W.)				
V_{DD} = +5 V, V_{SS} = 0 V	146	81	40	mA maximum
V_{DD} = +3 V, V_{SS} = 0 V	112	68	37	mA maximum
V_{DD} = 1.8 V, V_{SS} = 0 V	70	47	31	mA maximum
V_{DD} = 2.5 V, V_{SS} = −2.5 V	137	78	40	mA maximum

[1] Sx refer to S1 to S4 pins, and Dx refers to the D1 to D4 pins.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to V_{SS}	6V
V_{DD} to GND	–0.3V to +6V
V_{SS} to GND	+0.3V to −6V
V_L to GND	–0.3V to +6V
V_L to V_{SS}	6V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3V or 30mA, whichever occurs first
Digital Inputs[2]	GND − 0.3V to 6V or 30mA, whichever occurs first
Peak Current, Sx or Dx Pins[3]	682mA (pulsed at 1ms, 10% duty-cycle maximum)
Continuous Current, Sx or Dx Pins[3]	Data Table 6 and Table 7 + 15%
Temperature	
Operating Range	–40°C to +125°C
Storage Range	–65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-Free	As per JEDEC J-STD-020

1 Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Current must be limited to the maximum ratings given.

2 Overvoltages at the INx digital-input pins are clamped by internal diodes.

3 Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JCB} is the junction to the bottom of case thermal resistance.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JCB}	Unit
CC-16-10[1]	150	74.8	°C/W

1 Thermal impedance simulated values are based on JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADG1712

Table 10. ADG1712, 16-Lead LGA

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±4000	3A
FICDM	±1250	C3

1 For the input and output port to the supplies, the input and output port to the input and output port, and all other inputs.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

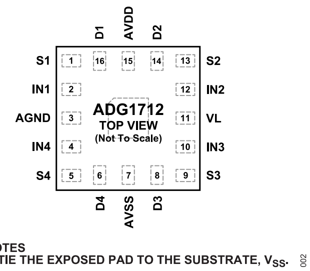

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1	Source Terminal 1. This pin can be an input or output.
2	IN1	Digital Control Input. Logic state controls the status of the switch S1 to D1.
3	AGND	Ground (0V) Reference.
4	IN4	Digital Control Input. Logic state controls the status of the switch S4 to D4.
5	S4	Source Terminal 4. This pin can be an input or output.
6	D4	Drain Terminal 4. This pin can be an input or output.
7	V_{SS}	Most Negative Power-Supply Potential. Decouple the V_{SS} pin using a 0.1µF capacitor to GND.
8	D3	Drain Terminal 3. This pin can be an input or output.
9	S3	Source Terminal 3. This pin can be an input or output.
10	IN3	Digital Control Input. Logic state controls the status of the switch S3 to D3.
11	V_L	Digital Logic Power Supply.
12	IN2	Digital Control Input. Logic state controls the status of the switch S2 to D2.
13	S2	Source Terminal 2. This pin can be an input or output.
14	D2	Drain Terminal 2. This pin can be an input or output.
15	V_{DD}	Most Positive Power-Supply Potential. Decouple the V_{DD} pin using a 0.1µF capacitor to GND.
16	D1	Drain Terminal 1. This pin can be an input or output.
EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, VSS.

Table 12. ADG1712 Truth Table

INx	Switch Condition
0	Off
1	On

TYPICAL PERFORMANCE CHARACTERISTICS

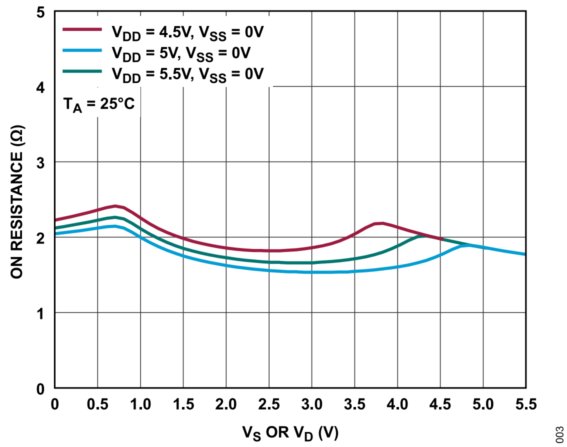

Figure 3. On Resistance vs. V_S or V_D, 5V Single Supply

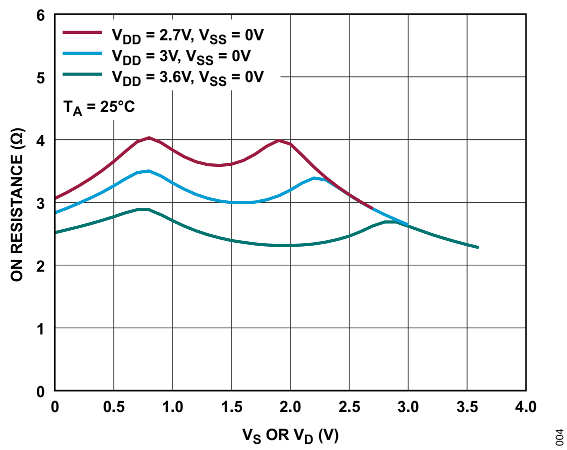

Figure 4. On Resistance vs. V_S or V_D, 3V Single Supply

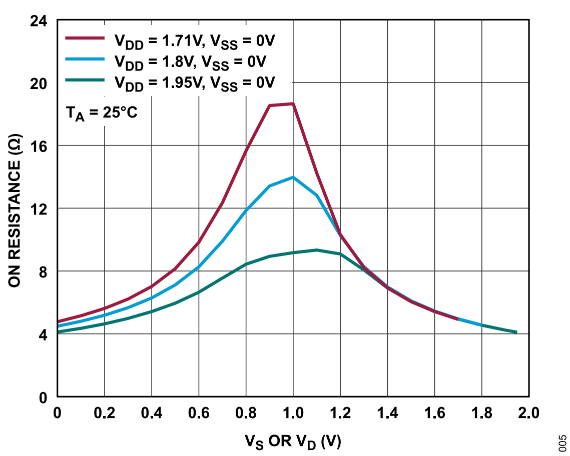

Figure 5. On Resistance vs. V_S or V_D, 1.8V Single Supply

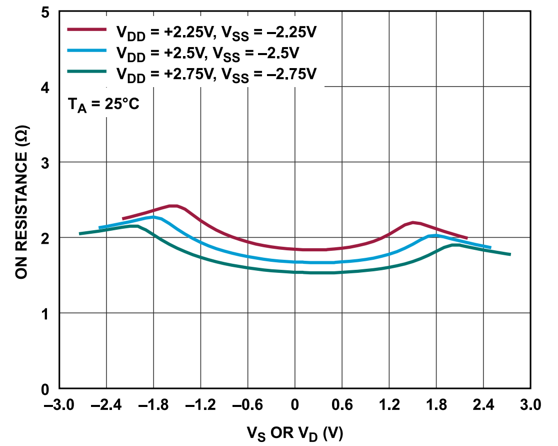

Figure 6. On Resistance vs. V_S or V_D, 2.5V Dual Supply

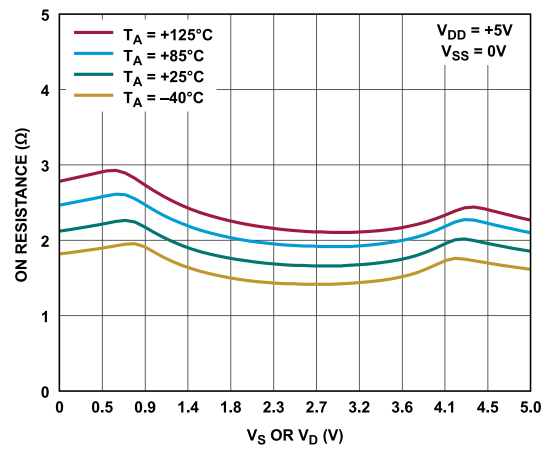

Figure 7. On Resistance vs. V_S or V_D for Different Temperatures, +5V Single Supply

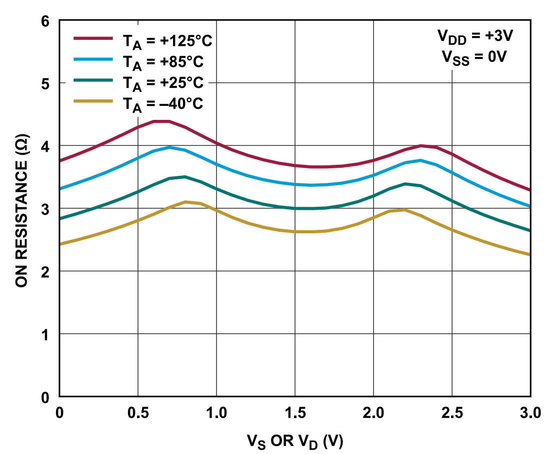

Figure 8. On Resistance vs. V_S or V_D for Different Temperatures, +3V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

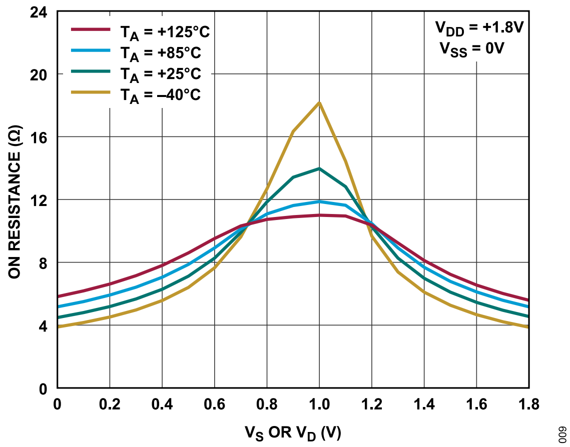

Figure 9. On Resistance vs. V_S or V_D for Different Temperatures, +1.8V Single Supply

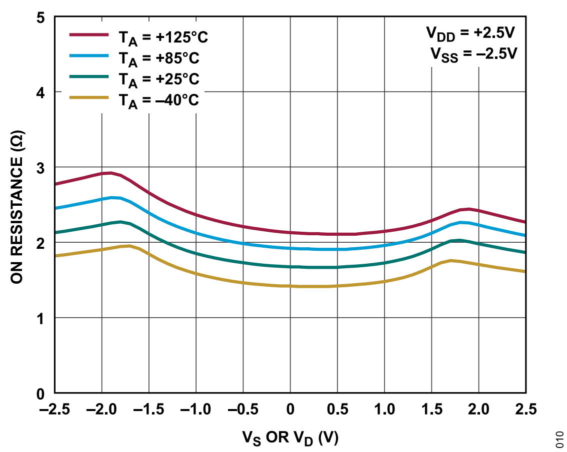

Figure 10. On Resistance vs. V_S or V_D for Different Temperatures, ±2.5V Dual Supply

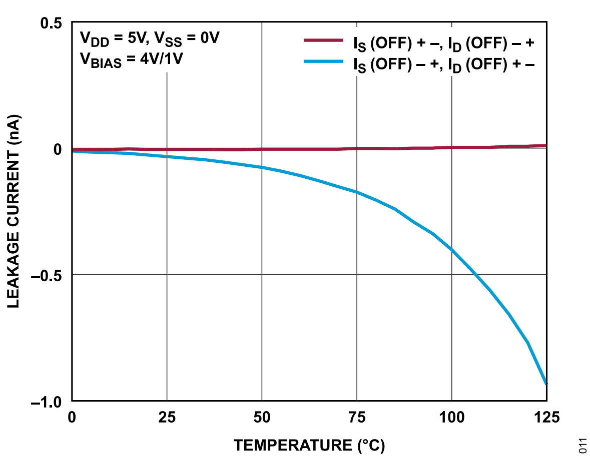

Figure 11. Off Leakage Currents vs. Temperature, +5V Single Supply

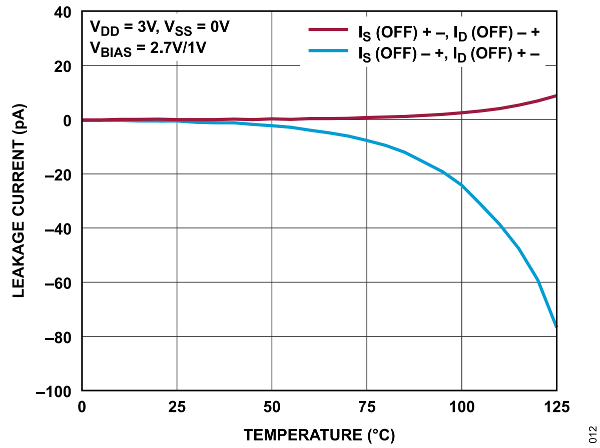

Figure 12. Off Leakage Currents vs. Temperature, +3V Single Supply

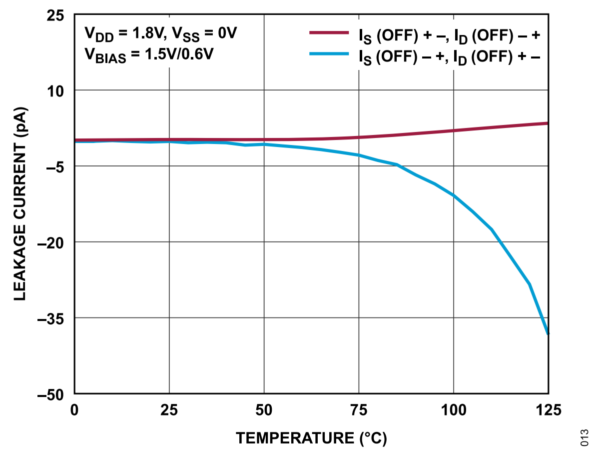

Figure 13. Off Leakage Currents vs. Temperature, +1.8V Single Supply

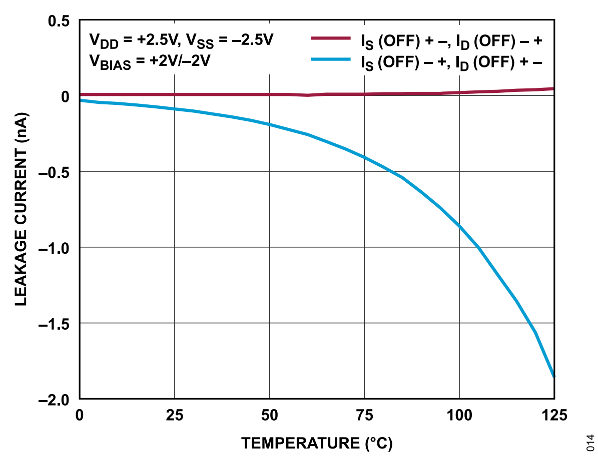

Figure 14. Off Leakage Currents vs. Temperature, ±2.5V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

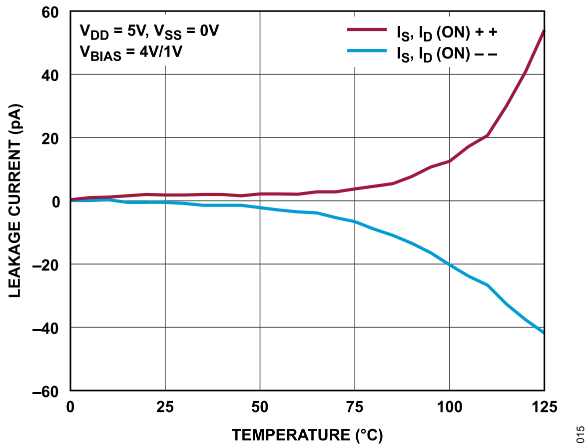

Figure 15. On Leakage Currents vs. Temperature, +5V Single Supply

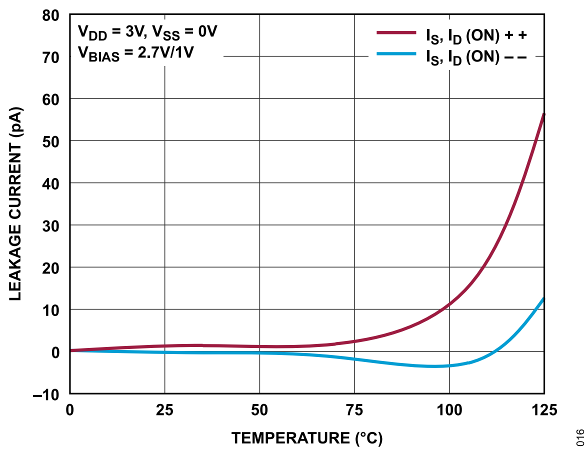

Figure 16. On Leakage Currents vs. Temperature, +3V Single Supply

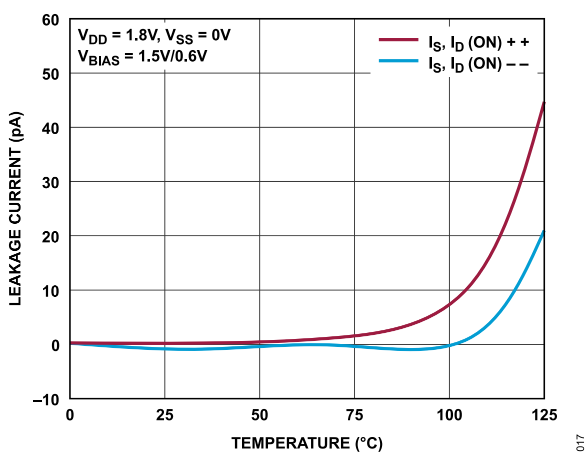

Figure 17. On Leakage Currents vs. Temperature, +1.8V Single Supply

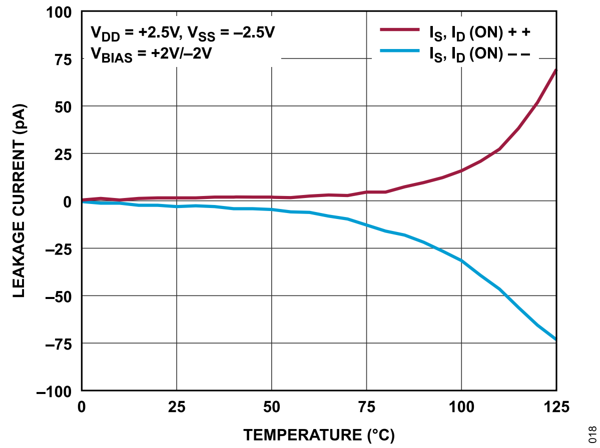

Figure 18. On Leakage Currents vs. Temperature, ±2.5V Dual Supply

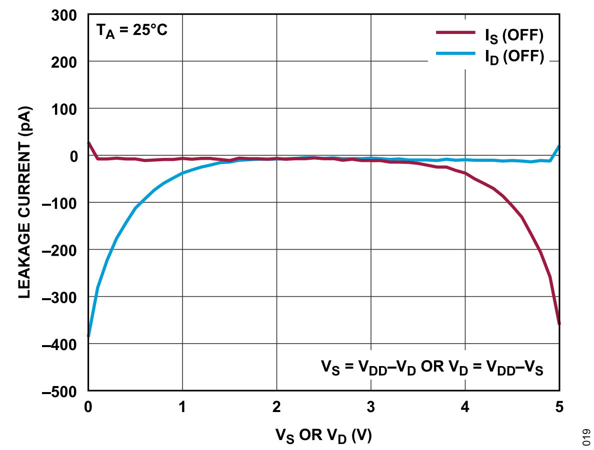

Figure 19. Off Leakage Currents as a Function of V_S, (V_D), 25°C, 5V Single Supply

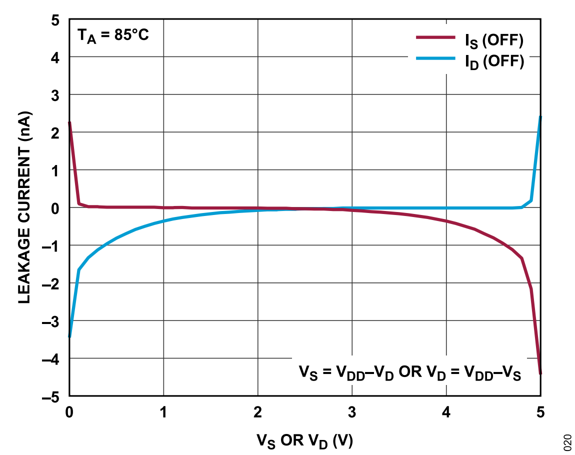

Figure 20. Off Leakage Currents as a Function of V_S, (V_D), 85°C, 5V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

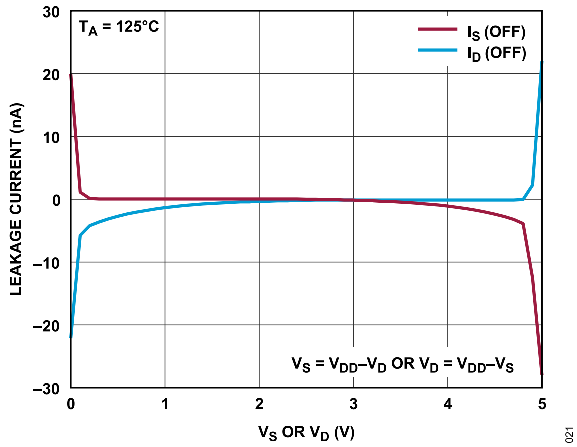

Figure 21. Off Leakage Currents as a Function of V_S, (V_D), 125°C, 5V Single Supply

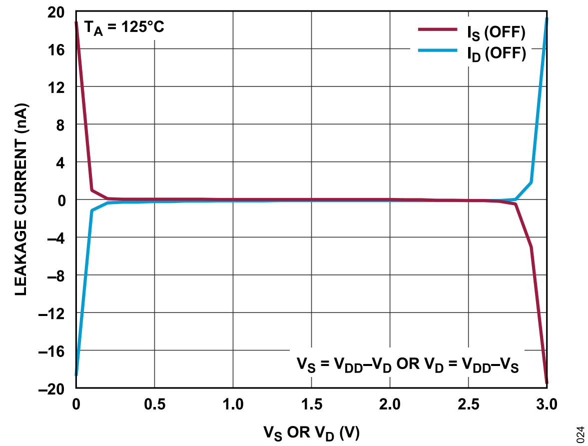

Figure 24. Off Leakage Currents as a Function of V_S, (V_D), 125°C, 3V Single Supply

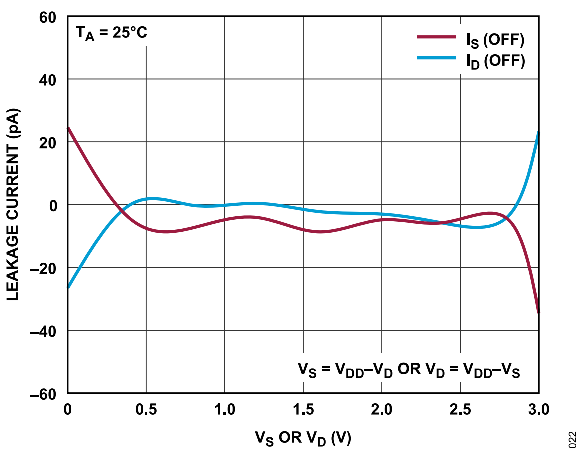

Figure 22. Off Leakage Currents as a Function of V_S, (V_D), 25°C, 3V Single Supply

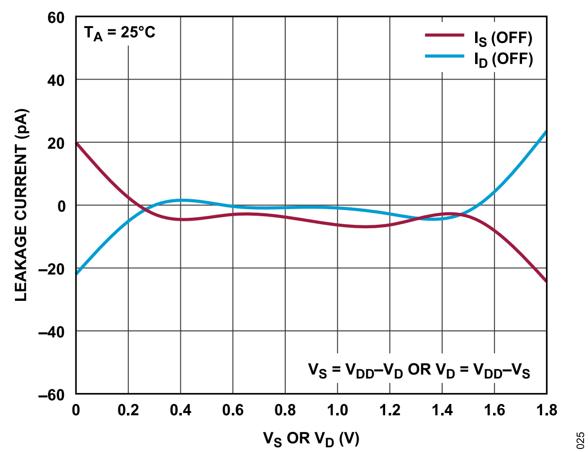

Figure 25. Off Leakage Currents as a Function of V_S, (V_D), 25°C, 1.8V Single Supply

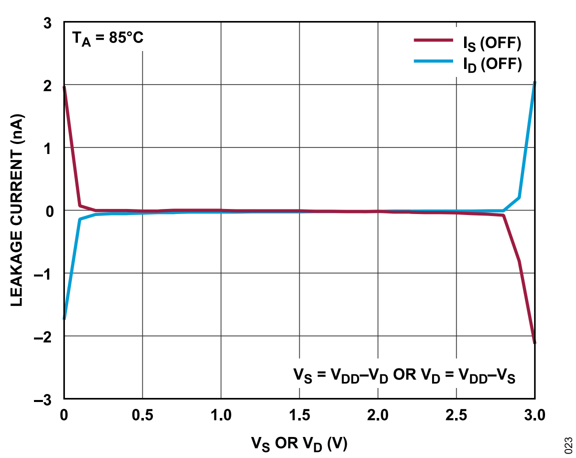

Figure 23. Off Leakage Currents as a Function of V_S, (V_D), 85°C, 3V Single Supply

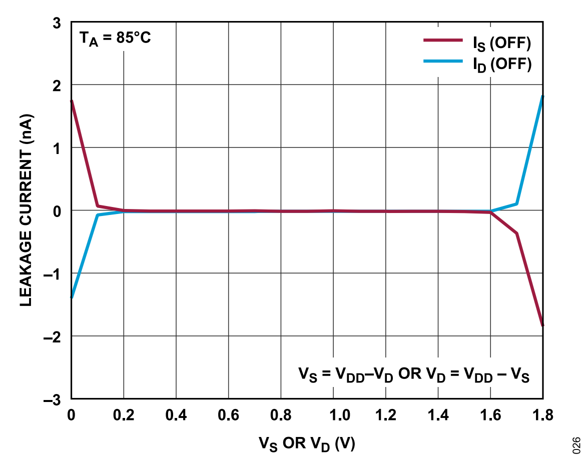

Figure 26. Off Leakage Currents as a Function of V_S, (V_D), 85°C, 1.8V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

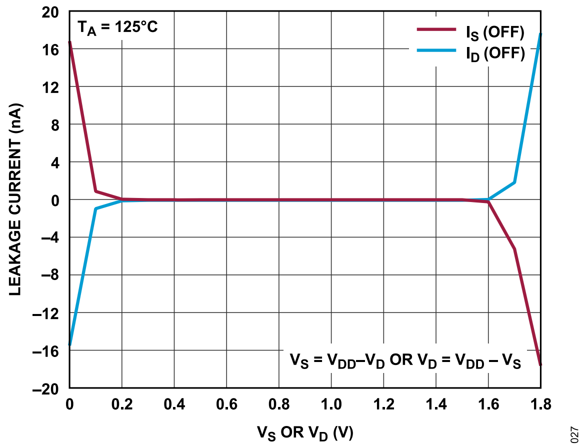

Figure 27. Off Leakage Currents as a Function of V_S, (V_D), 125°C, 1.8V Single Supply

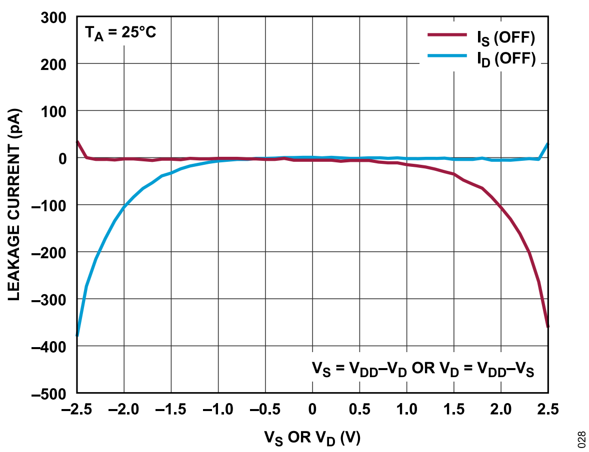

Figure 28. Off Leakage Currents as a Function of V_S, (V_D), 25°C, 2.5V Dual Supply

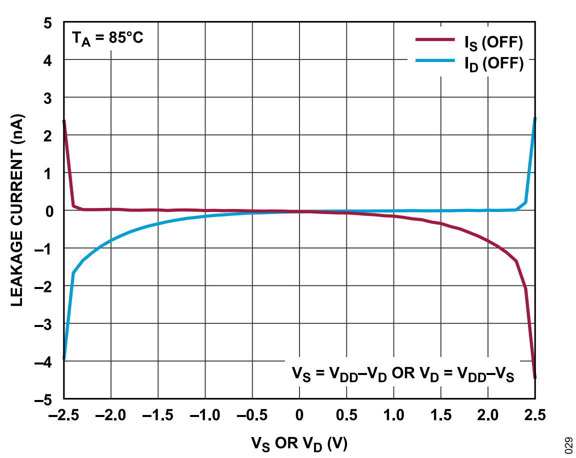

Figure 29. Off Leakage Currents as a Function of V_S, (V_D), 85°C, 2.5V Dual Supply

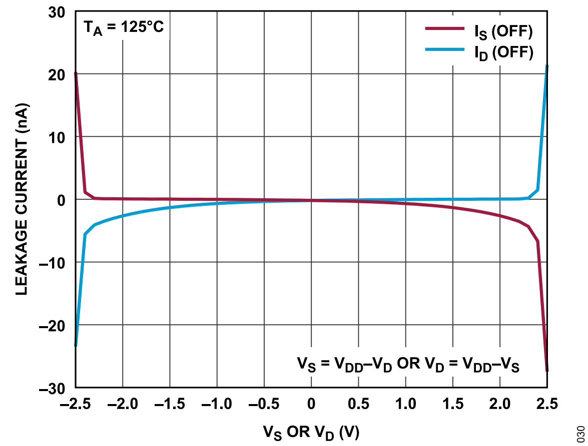

Figure 30. Off Leakage Currents as a Function of V_S, (V_D), 125°C, 2.5V Dual Supply

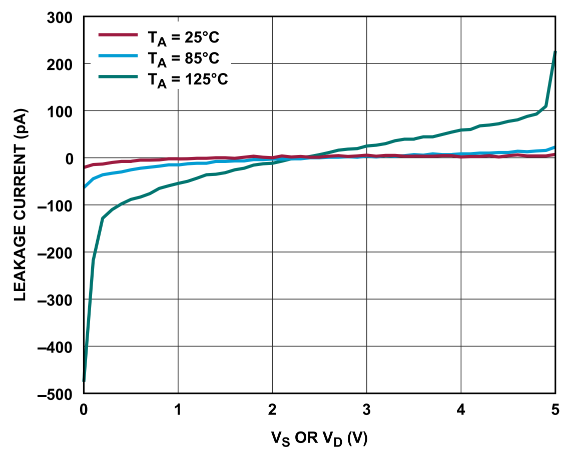

Figure 31. On Leakage Currents as a Function of V_S, (V_D), 5V Single Supply

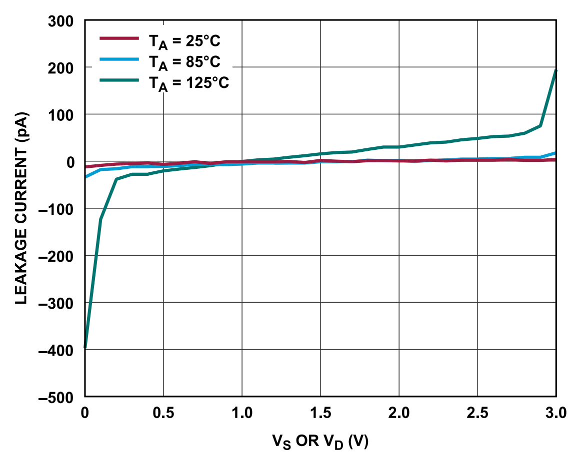

Figure 32. On Leakage Currents as a Function of V_S, (V_D), 3V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

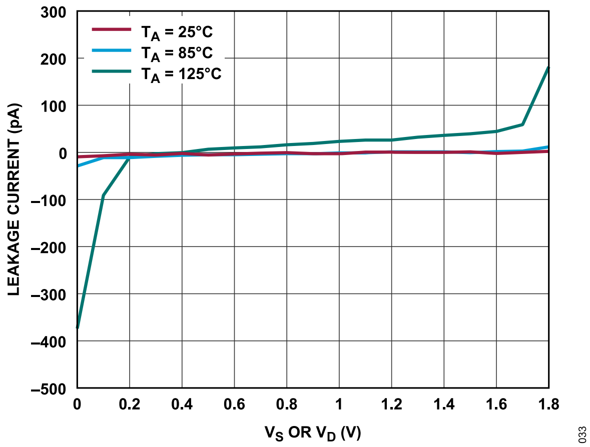

Figure 33. On Leakage Currents as a Function of V_S, (V_D), 1.8V Single Supply

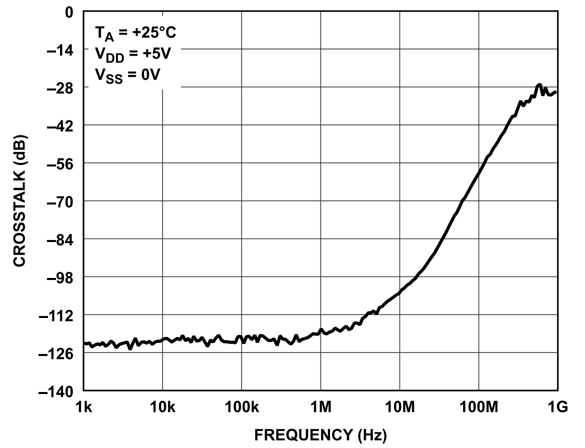

Figure 36. Crosstalk vs. Frequency, 5V Single Supply

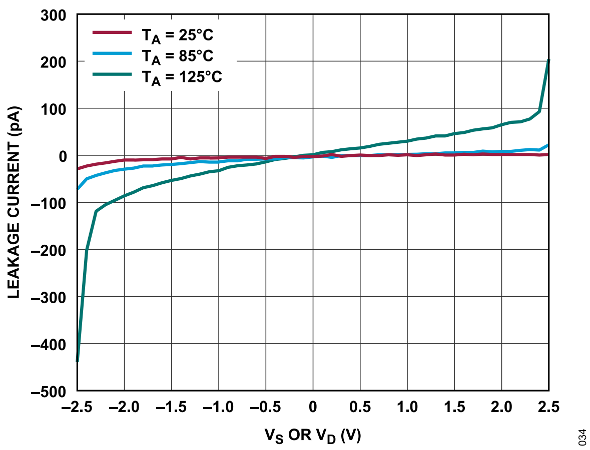

Figure 34. On Leakage Currents as a Function of V_S, (V_D), 2.5V Dual Supply

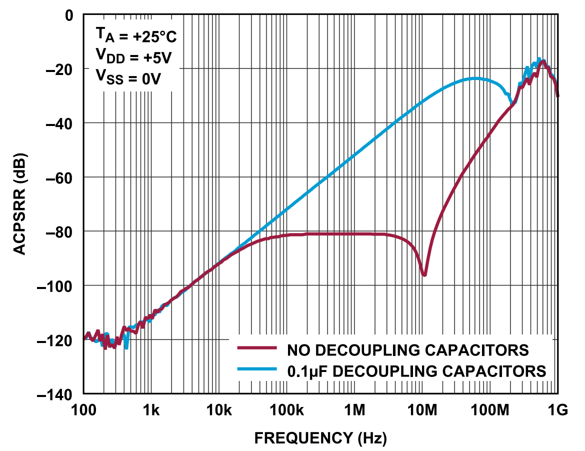

Figure 37. AC PSRR vs. Frequency, 5V Single Supply

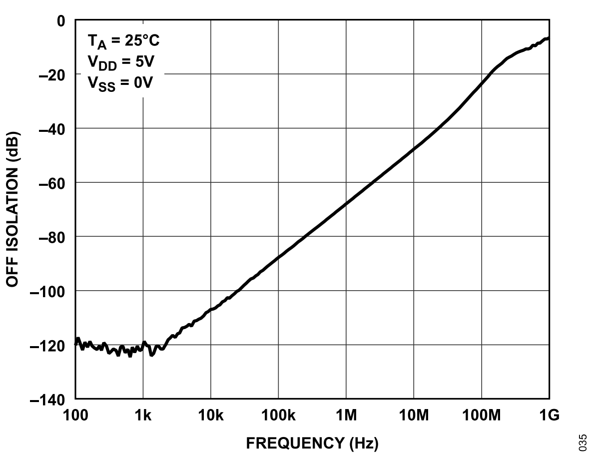

Figure 35. Off Isolation vs. Frequency, 5V Single Supply

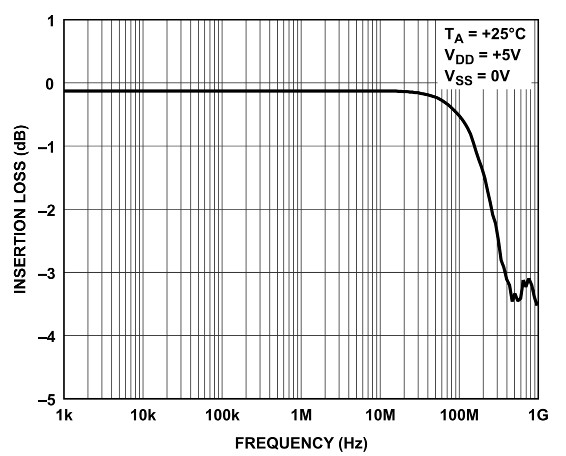

Figure 38. Insertion Loss vs. Frequency, 5V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

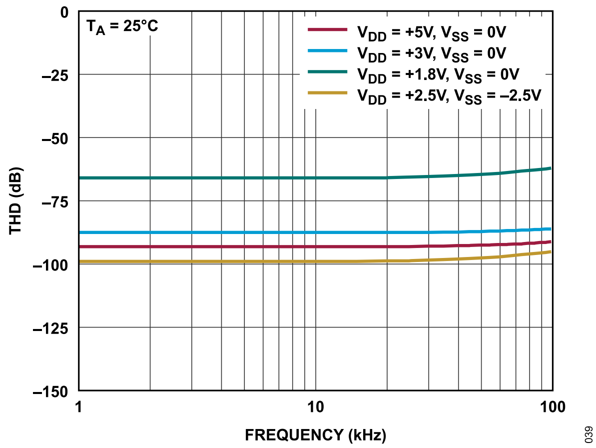

Figure 39. THD vs. Frequency

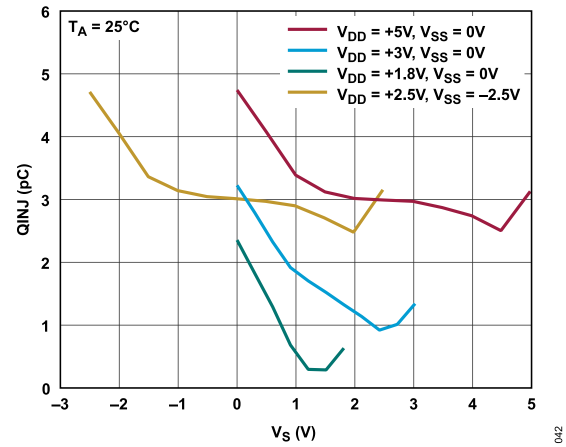

Figure 42. Charge Injection (QINJ) vs. V_S

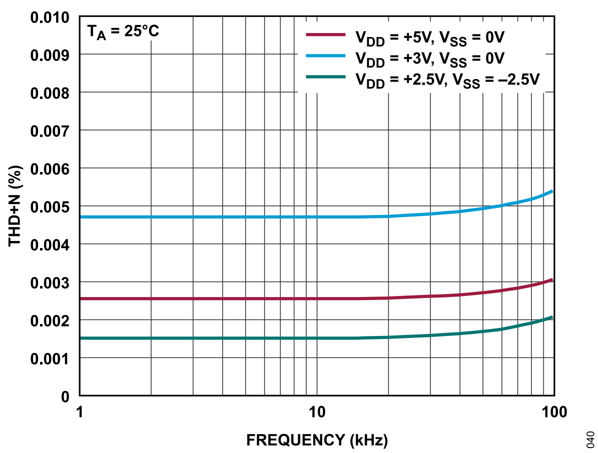

Figure 40. THD + N vs. Frequency

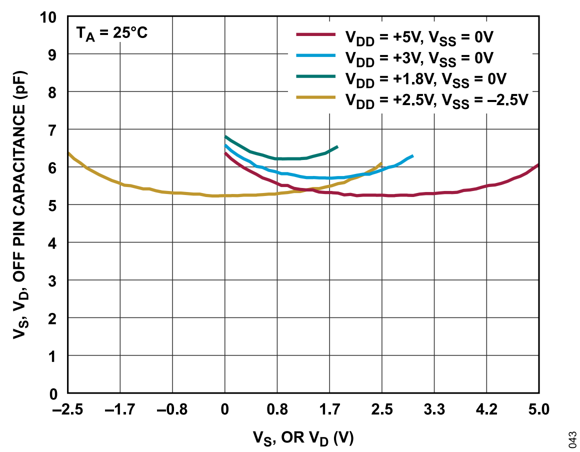

Figure 43. Off Pin Capacitance vs. V_S

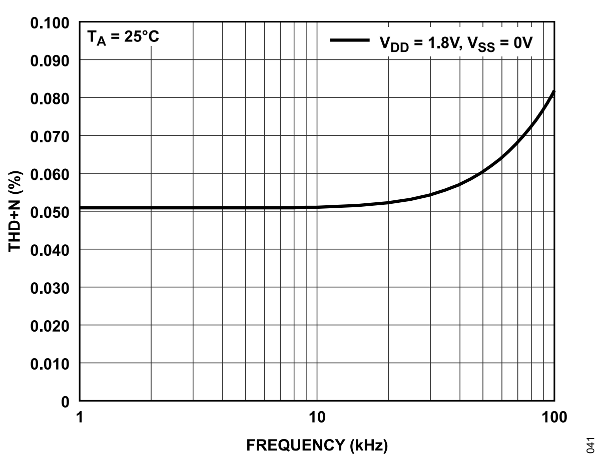

Figure 41. THD + N vs. Frequency, 1.8V Single Supply

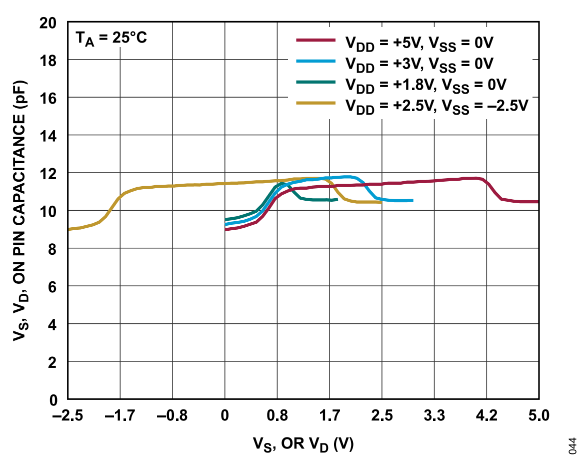

Figure 44. On Pin Capacitance vs. V_S

TYPICAL PERFORMANCE CHARACTERISTICS

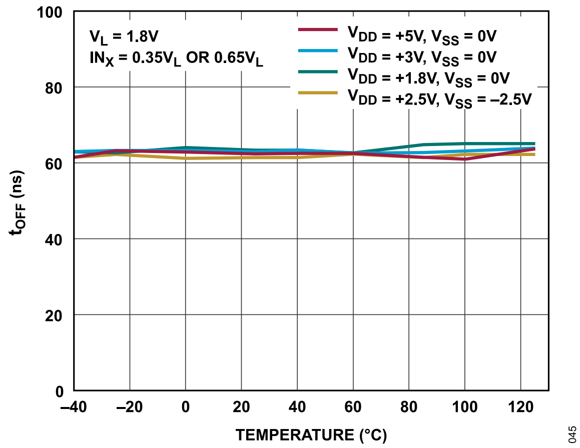

Figure 45. T_{OFF} Times vs. Temperature

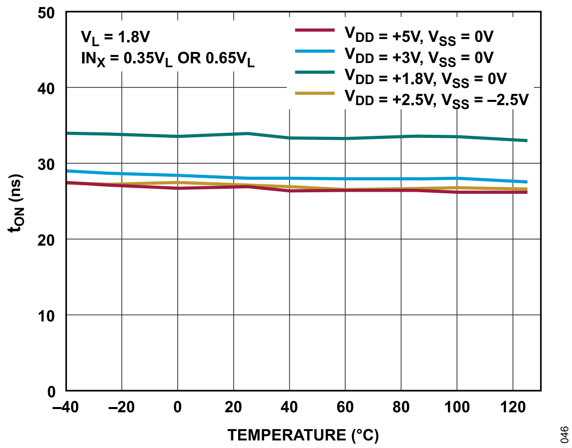

Figure 46. T_{ON} Times vs. Temperature

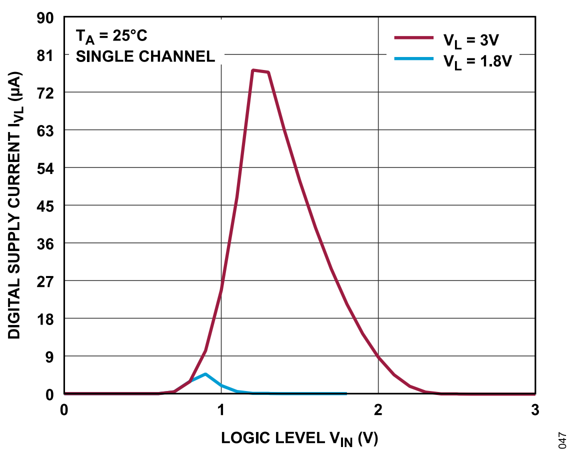

Figure 47. Digital Supply Current vs. Logic Level

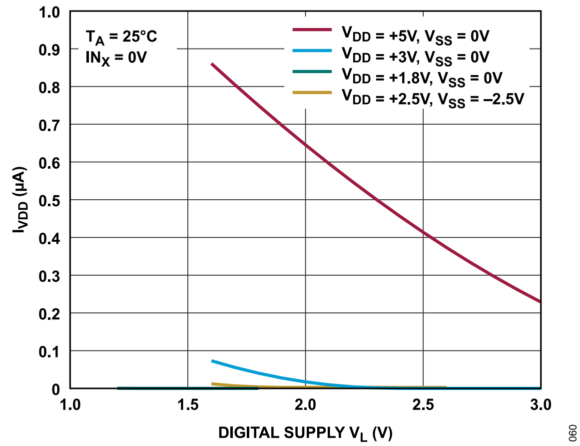

Figure 48. Positive Supply Current (IVDD) vs. Digital Supply (VL)

TEST CIRCUITS

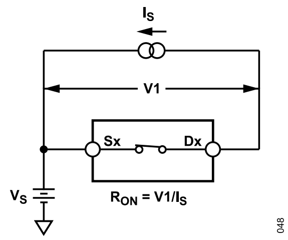

Figure 49. On Resistance

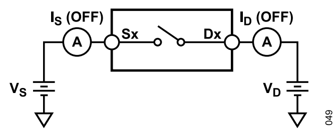

Figure 50. Off Leakage

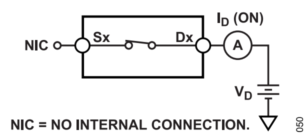

Figure 51. On Leakage

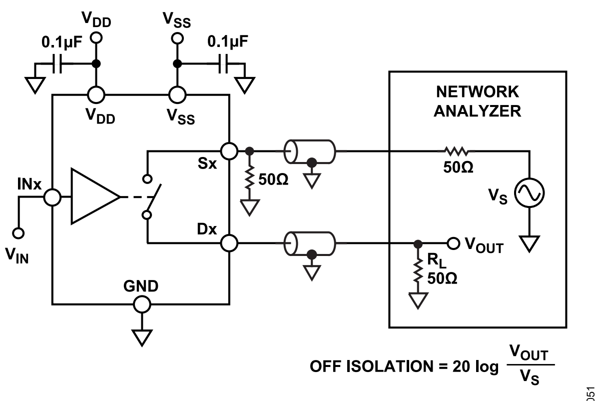

Figure 52. Off Isolation

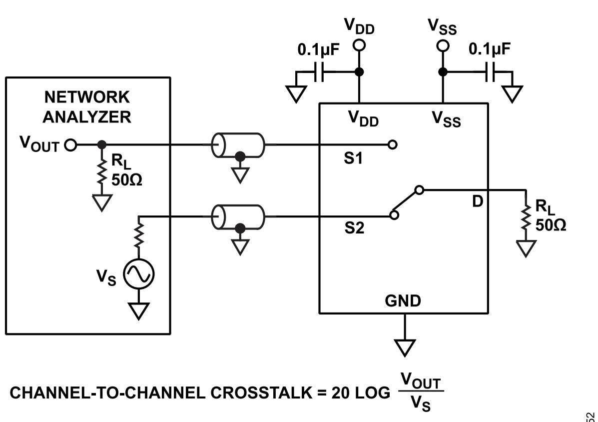

Figure 53. Channel-to-Channel Crosstalk

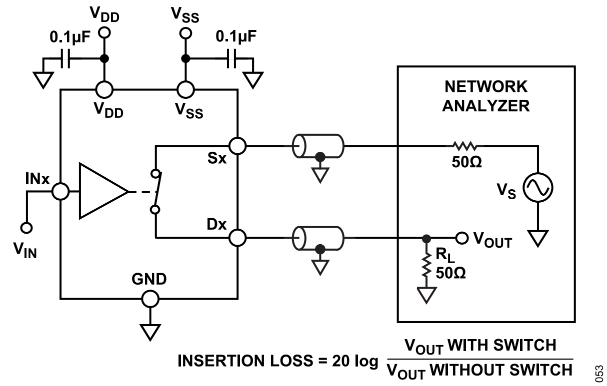

Figure 54. Bandwidth

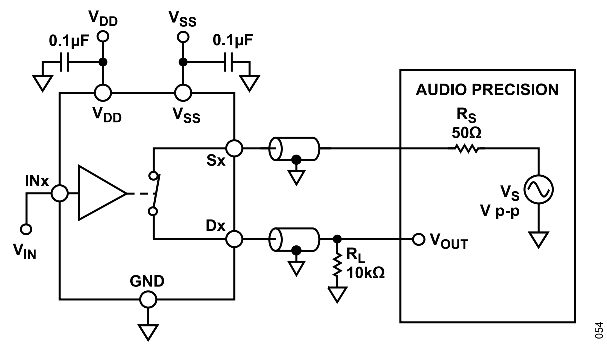

Figure 55. THD + Noise

TEST CIRCUITS

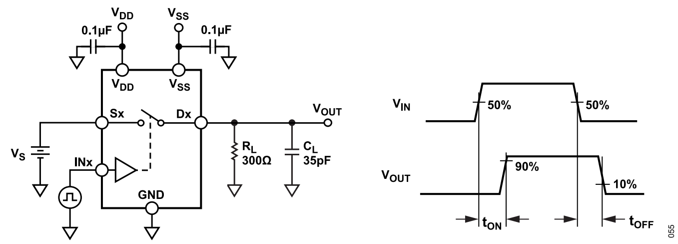

Figure 56. Switching Times

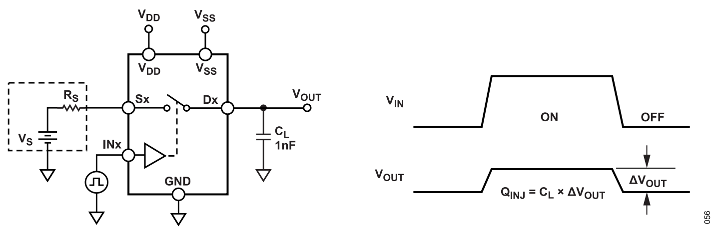

Figure 57. Charge Injection

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

I_{VL}

The digital supply current.

V_D and V_S

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

ΔR_{ON}

The difference between the R_{ON} of any two channels.

I_S Off

The source leakage current with the switch off.

I_D Off

The drain leakage current with the switch off.

I_D I_S On

The channel leakage current with the switch on.

V_D AND V_S

Analog voltages on Terminal D and Terminal S.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL}, I_{INH}

The input current of the digital input when high or when low.

C_S (Off) and C_D (Off)

The off switch source and drain capacitance for the off condition, which is measured with reference to ground.

C_D (On) and C_S (On)

The on switch drain and source capacitance for the on condition, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON}

The delay between the 50% and 90% points of the digital control input and the output switching on.

t_{OFF}

The delay between the 50% and 10% points of the digital control input and the output switching off.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Channel-to-Channel Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

Insertion Loss

The loss due to the on resistance of the switch.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)

A measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The DC voltage on the device is modulated by a sine wave of 0.62V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the AC PSRR.

THEORY OF OPERATION

SWITCH ARCHITECTURE

The ADG1712 is a set of low voltage CMOS quad SPST switches that are compatible with a wide range of power supply voltages.

The ADG1712 is designed for precision applications where size and channel density are a priority. The ADG1712 gives an optimal balance of low on resistance (2.4Ω typical), and low leakage currents (0.01nA, typical) in a very small 2mm × 2mm LGA package, to suit a very broad range of user applications.

3V AND 1.8V JEDEC COMPLIANCE

An external V_L supply provides flexibility for lower logic levels. The following V_L conditions must be satisfied for the switch to operate in either 3V or 1.8V logic operation:

- V_L = 2.7V to 3.6V for 3V logic
- V_L = 1.65V to 1.95V for 1.8V logic

V_L FLEXIBILITY

The absolute maximum voltage rating for the digital control input pins (INx) is −0.3V to 6V. The digital control inputs are not limited to the external V_L supply or V_{DD}. This allows the digital input voltages to be present without the V_L supply and gives the ability to use the V_L pin as an enable pin for all four switch channels in the ADG1712. Regardless of the input voltage on the digital input pins, if V_L = 0 V, all of the switch channels will be off. This flexibility also allows V_L voltages higher than V_{DD} if required, just ensure not to violate the 6V maximum voltage rating between V_L and V_{SS}.

APPLICATIONS INFORMATION

DATA ACQUISITION SYSTEM CALIBRATION

ADG1712 can be used in a broad variety of applications to add flexibility and configurations to systems that require low voltage switching of precision analog signals, digital signals, and low voltage power supplies. Figure 58 shows a typical application where the ADG1712 is used in a differential analog input to a data acquisition system. In this typical system, to preform a system calibration, it is required to short the differential inputs together. The small package size of the ADG1712 provides advantages in applications that are area constrained, and the flexible supply voltage allows the ADG1712 to adapt to the existing system power supply ranges.

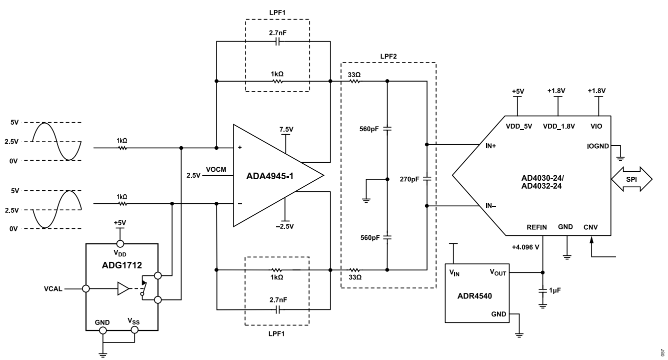

Figure 58. Typical Application

OUTPUT LOAD FOR REDUCED OVERSHOOT

The each channel of the ADG1712 can toggle at a very high speed. Typically 21ns for T_{ON} and 52ns for T_{OFF}. These very high switching speeds are an advantage in systems such as high speed digital circuits or communications systems. However, depending on the load at the output of the switch circuit, the very fast switching action can cause voltage overshoots to occur. Depending on the switch supply voltage and the level of the signal voltage through the switch, an overshoot can cause the voltage at the output of the switch to go beyond the supply voltage and exceed the absolute ratings for the ADG1712. Adding extra load capacitance is a practical solution to mitigate these overshoots, ensuring the output voltage remains within safe limits.

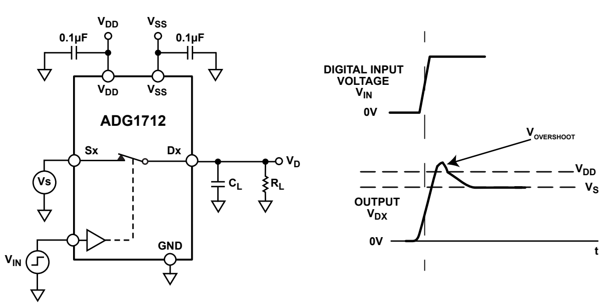

Figure 59. ADG1712 Overshoot

POWER-SUPPLY RAILS

To guarantee correct operation of the ADG1712, 0.1µF decoupling capacitors are required on the V_{DD}, V_{SS}, and V_L supply pins.

The ADG1712 can operate with single supplies from +1.08V to +5.5V and dual supplies between ±1.08V to ±2.75V. The supplies on V_{DD} and V_{SS} do not have to be asymmetrical. However, the V_{DD} to V_{SS} range must not exceed 5.5V as stated in Table 1.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a 3V unipolar power solution is shown in Figure 60. The ADP162 ultra-low quiescent current, 150mA, CMOS linear regulator generates a positive supply rail for the ADG1712 along with other components such as amplifiers and/or a precision converter in a typical signal chain.

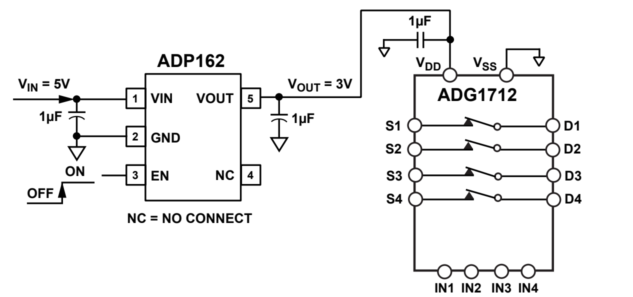

Figure 60. Power Supply Recommendation

OUTLINE DIMENSIONS

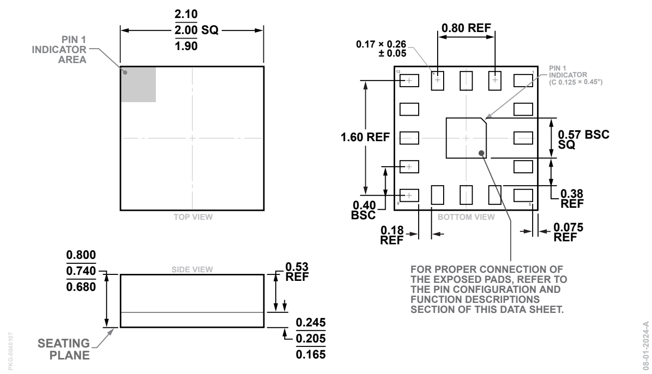

Figure 61. 16-Lead Land Grid Array [LGA]
2mm × 2mm Body and 0.74mm Package Height
(CC-16-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature	Package Description	Package Option	Package Quantity
ADG1712BCCZ-RL7	−40°C to +125°C	16-Terminal Land Grid Array [LGA]	CC-16-10	Reel, 1500

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADG1712ARDZ	Evaluation Board

[1] Z = RoHS Compliant Part.