

LTM4710-1 Low V_{IN}, Quad 8A Silent Switcher µModule Regulator

DESCRIPTION

Demonstration circuit 3164A-B features the LTM®4710-1, a quad DC/DC step-down µModule® regulator with 8A per output, packaged in a compact (6mm × 12mm × 3.54mm) land grid array (LGA) with pre-made solder balls. DC3164A-B has an operating input range of 2.5V to 5.5V. The outputs of the four channels are 0.8V, 1.0V, 1.2V, and 1.5V with 8A per output, respectively. All outputs voltages are programmable from 0.5V up to 3.6V (step-down only). DC3164A-B operates by default at 1.5MHz and can be adjusted by an external resistor from 1MHz to 5MHz or by being synchronized to an external clock from 1.2MHz to 2.6MHz. DC3164A-B also allows for the channels to be paralleled up to 32A load current.

LTM4710-1 integrates four separate constant-frequency peak current mode control regulators, power MOSFETs, inductors, and other supporting discrete components. It employs the second-generation Silent Switcher® technologyin which it allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI performance. Refer to the LTM4710-1 data sheet for more detailed information.

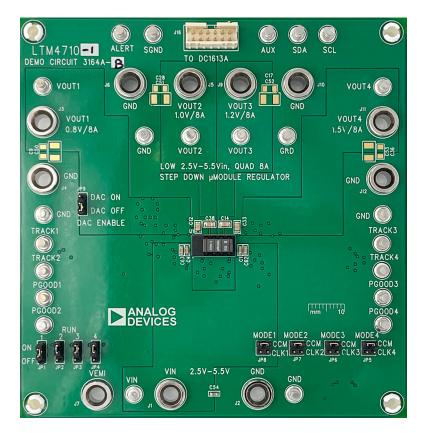
It is recommended to read the data sheet of the LTM4710-1 prior to making any changes to the DC3164A-B board.

Design files for this circuit board are available.

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BOARD PHOTO

Part marking is either ink mark or laser mark



PERFORMANCE SUMMARY Specifications are at $T_A = 25^{\circ}C$, no forced-air cooling

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range V _{IN}		2.5		5.5	V
Default Switching Frequency			1.5		MHz
Maximum Output Current	For Each Channel		8		А
Output Voltage of Channel 1, V _{OUT1}			0.8		V
Output Voltage of Channel 2, V _{OUT2}			1.0		V
Output Voltage of Channel 3, V _{OUT3}			1.2		V
Output Voltage of Channel 4, V _{OUT4}			1.5		V
Efficiency of Channel 1	$V_{IN} = 3.3V$, $f_{SW} = 1.5MHz$, $V_{OUT1} = 0.8V$, $I_{OUT1} = 8A$		85.1		%
Efficiency of Channel 2	V _{IN} = 3.3V, f _{SW} = 1.5MHz, V _{OUT2} = 1.0V, I _{OUT2} = 8A		85.8		%
Efficiency of Channel 3	$V_{IN} = 3.3V$, $f_{SW} = 1.5MHz$, $V_{OUT3} = 1.2V$, $I_{OUT3} = 8A$		87.8		%
Efficiency of Channel 4	$V_{IN} = 3.3V$, $f_{SW} = 1.5MHz$, $V_{OUT4} = 1.5V$, $I_{OUT4} = 8A$		89.2		%

QUICK START PROCEDURE

Demonstration circuit 3164A-B is easy to set up to evaluate the performance of the LTM4710-1. See Figure 1 for the proper measurement equipment setup and follow the procedure below.

1. With power off, place the jumpers as shown in the following positions.

NAME	POSITION
RUN1	ON
RUN2	ON
RUN3	ON
RUN4	ON
DAC ENABLE	OFF

NAME	POSITION
MODE1	CCM
MODE2	CCM
MODE3	CCM
MODE4	CCM

- 2. With power off, (see Figure 1), connect the input power supply between VIN and GND. Connect the output loads between VOUT1 and GND, VOUT2 and GND, VOUT3 and GND, and VOUT4 and GND, respectively.
- 3. Connect the DMMs to the input and outputs.
- 4. Turn on the input power supply.

NOTE: The input voltage should be between 2.5V and 5.5V.

- 5. Check for the proper output voltages. The output voltage meters for each channel should display the programmed output voltages ($V_{OUT1} = 0.8V$, $V_{OUT2} = 1.0V$, $V_{OUT3} = 1.2V$, $V_{OUT4} = 1.5V$) within $\pm 1.5\%$.
- 6. Once the input and output voltages are properly established, adjust the load current within the operating range of OA to 8A max for each channel. Observe the output voltage regulation, output voltage ripples, load transient response and other parameters.
- 7. Vary the input voltage from 2.5V to 5.5V. Observe the output voltage regulation.

NOTE: When measuring the output or input voltage ripple, do not use the long ground lead on the oscilloscope probe. See Figure 2 for the proper scope probe technique. Short, stiff leads need to be soldered to the (+) and (-) terminals of an output capacitor. The probe's ground ring needs to touch the (-) lead and the probe tip needs to touch the (+) lead.

OPTIONAL: An input EMI filter is included on the board. To include this filter, connect the input supply positive terminal to VEMI. Connect the input positive supply to VIN to exclude the input EMI filter.

QUICK START PROCEDURE

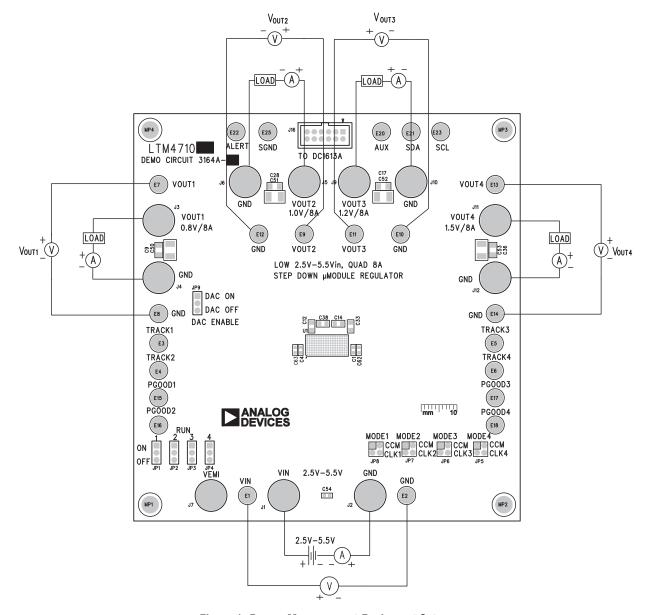


Figure 1. Proper Measurement Equipment Setup

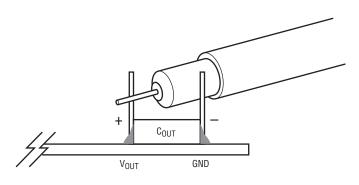


Figure 2. Measuring Output Voltage Ripple

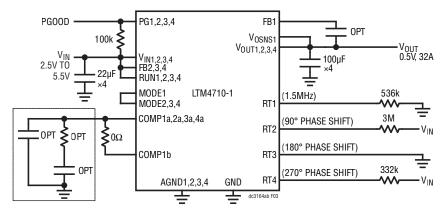
MULTIPHASE CONFIGURATION

For output loads that demand more than 8A of current, multiple LTM4710-1 channels can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. Figure 3 shows the typical paralleled application where channel 1 is used as the main channel and the rest of LTM4710-1 channels are programmed as the subordinary channels to achieve the same switching frequency, interleaved phase shift and current sharing among different channels.

The RT pin of the main phase is connected to a resistor to AGND, programming the frequency and configuring

the MODE pin to become clock output used to drive the MODE pin of the subordinary phase(s).

Connecting the FB pin to V_{IN} configures a phase as a subordinary phase. The MODE becomes an input, and the voltage control loop is disabled. The subordinary phase current control loop is still active, and the peak current is controlled via the shared COMP node. The phase shift of a subordinary phase relative to the main phase is programmed with a resistor divider on the RT pin. Refer to the LTM4710-1 data sheet for more detailed information.



PINS NOT SHOWN IN THIS CIRCUIT: SSTT, SW; COMP2b, COMP3b, COMP4b NO CONNECTION.

Figure 3. Paralleled Single Output, 0.5V, 32A DC/DC μModule Regulator

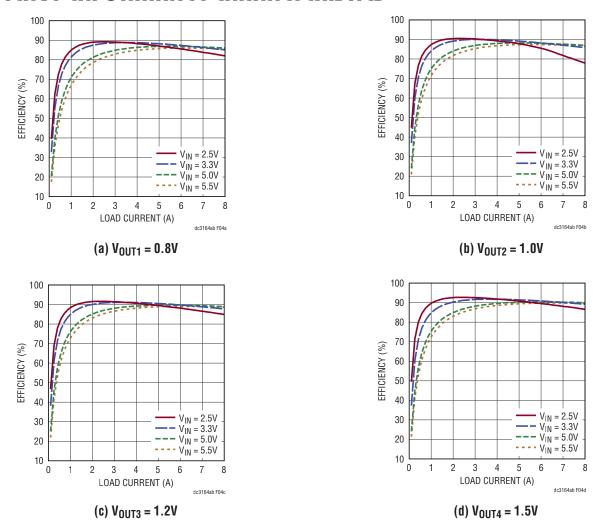


Figure 4. Measured Efficiency of Each Channel ($f_{SW} = 1.5$ MHz), No Forced Air Cooling with $T_A = 25$ °C

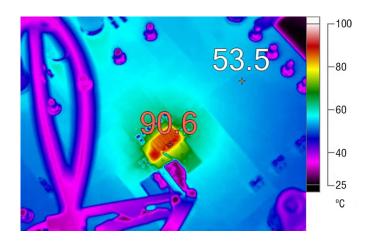


Figure 5. Thermal Performance of 0.8V, 1.0V, 1.2V, and 1.5V with 8A per Output ($V_{IN}=3.3V$, $f_{SW}=1.5$ MHz), $T_A=25$ °C, No Forced Air Cooling

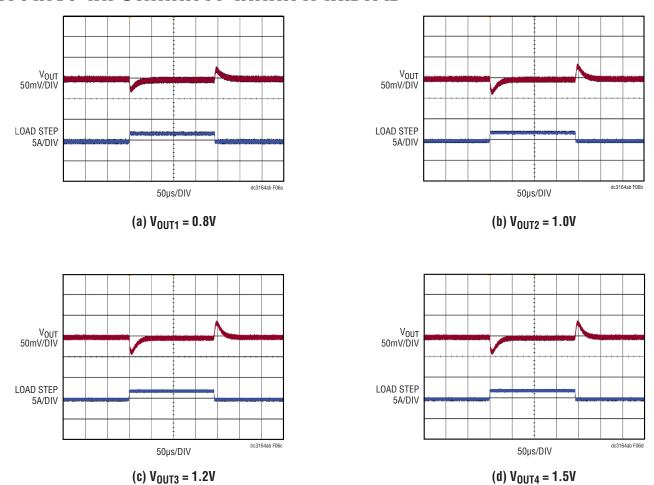


Figure 6. Load Transient Responses with Load Steps OA to 2A to OA, $dI/dt = 2A/\mu s$ ($V_{IN} = 3.3V$, $f_{SW} = 1.5 MHz$)

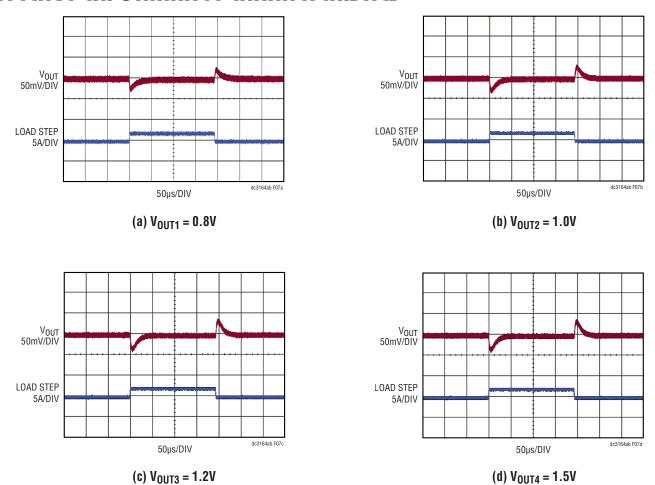
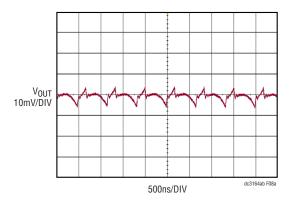
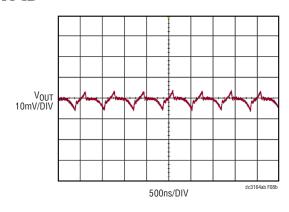


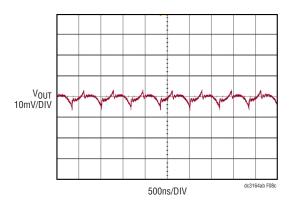
Figure 7. Load Transient Responses with Load Steps 6A to 8A to 6A, $dI/dt = 2A/\mu s$ ($V_{IN} = 3.3V$, $f_{SW} = 1.5 MHz$)



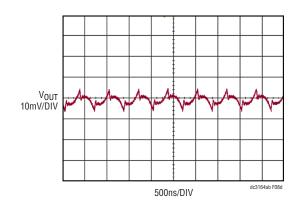
(a)
$$V_{OUT1} = 0.8V$$
, $I_{OUT1} = 8A$



(b) $V_{OUT2} = 1.0V$, $I_{OUT2} = 8A$



(c) $V_{OUT3} = 1.2V$, $I_{OUT3} = 8A$



(d) $V_{OUT4} = 1.5V$, $I_{OUT4} = 8A$

Figure 8. Output Voltage Ripple ($V_{IN} = 3.3V$, $f_{SW} = 1.5MHz$, 350MHz BW)

PARTS LIST

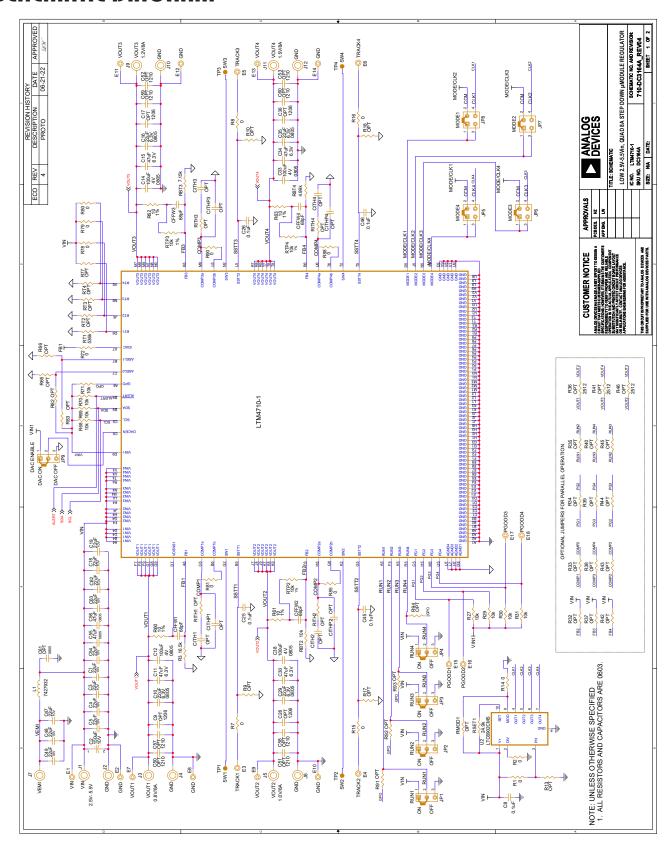
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Require	d Circuit	t Components		1
1	12	C1, C3-C5, C18-C19, C47-C49, C54, C62-C63	CAP., 22µF, X5R, 10V, 20%, 0603	SAMSUNG, CL10A226MP8NUNE
2	1	C2	CAP, 150µF, ALUM POLY, OS-CON, 10V, 20%, 8mm × 6.9mm, E7, SMD, RADIAL, SVP	PANASONIC, 10SVP150MX
3	5	C8, C25-C26, C45-C46	CAP., 0.1µF, X7R, 50V, 10%, 0603	TDK, C1608X7R1H104K080AA
4	4	C10, C16, C29, C35	CAP., 22µF, X5R, 6.3V, 20%, 0805	TDK, C2012X5R0J226M125AC
5	4	C11, C15, C30, C34	CAP,47µF, X5R, 6.3V, 20%, 0603, NO SUBS. ALLOWED	MURATA, GRM188R60J476ME15D
6	4	C12, C14, C33, C38	CAP., 100μF, X6S, 4V, 20%, 0805	MURATA, GRM21BC80G107ME15L
7	2	C55, C56	CAP, 47µF, X5R, 10V, 20%, 0805	TDK, C2012X5R1A476M125AC
8	4	CFFW1, CFFW2, CFFW3, CFFW4	CAP, 68pF, C0G, 25V, 10%, 0603	KEMET, C0603C680K3GACTU
9	15	R1-R2, R7-R8, R14-R16, R72, R78-R81, R85, R88, R90	RES., 0Ω, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ3GEY0R00V
10	1	R3	RES., 16.5k, 1%, 1/10W, 0603, AEC-Q200	VISHAY, CRCW060316K5FKEA
11	8	R27, R29-R31, R68, R69-R71	RES., 10k, 5%, 1/10W, 0603	YAGEO, RC0603JR-0710KL
12	4	R60-R63	RES., 10Ω, 1%, 1/10W, 0603	YAGEO, RC0603FR-0710RL
13	4	RBT2, RTP2, RTP3, RTP4	RES., 10k, 1%, 1/10W, 0603	YAGEO, RC0603FR-0710KL
14	1	RBT3	RES., 7.15k, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ3EKF7151V
15	1	RBT4	RES., 4.99k, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ3EKF4991V
16	1	RSET1	RES., 24.9k, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ3EKF2492V
17	1	RT1	RES., 536k, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ3EKF5363V
18	1	L1	IND., 98Ω AT100MHz, FERRITE BEAD, 25%, 18A, 0.9m Ω , 1LN, 7847	WURTH ELEKTRONIK, 7427932
19	1	U1	IC, LOW V _{IN} QUAD 8A Silent Switcher μModule, BGA	ANALOG DEVICES, LTM4710EV-1#PBF
20	1	U2	IC, MULTIPHASE OSC WITH FREQ MOD, MSOP-10	ANALOG DEVICES, LTC6902CMS#PBF
Addition	al Dem	o Board Circuit Components		
1	0	C9, C17, C28, C36	CAP., OPTION, 1206	
2	0	C50-C53, C57-C60	CAP., OPTION, 1210	
3	0	C61	CAP., OPTION, 0805	
4	0	CITH1-CITH4, CITHP1-CITHP4	CAP., OPTION, 0603	
5	0	R9-R10, R13, R17-R18, R32-R35, R37-R40, R42- R45, R65-R66, R77, R82-R83, R91-R94, RITH1-RITH4, RMOD1, RT2-RT4	RES., OPTION, 0603	
6	0	R36, R41, R46	RES., OPTION, 2512	
7	0	R95-R98	RES., OPTION, 2010	

DEMO MANUAL DC3164A-B

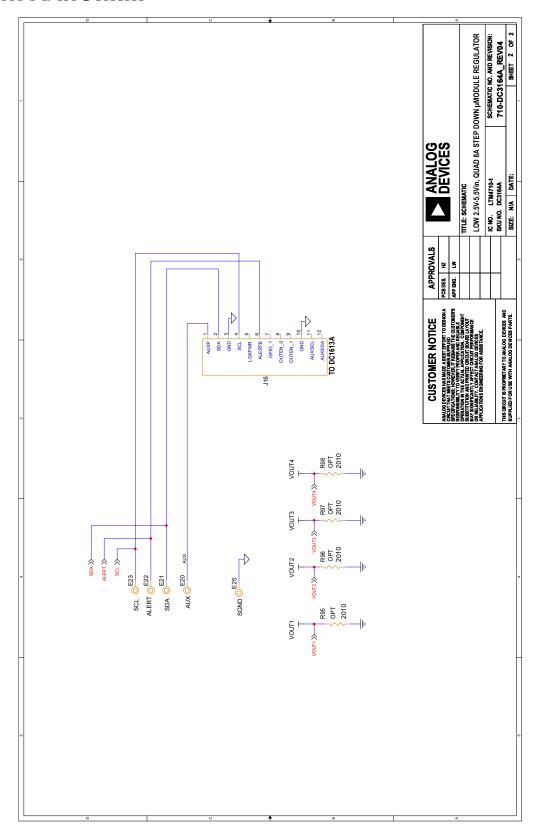
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER		
Hardwar	Hardware for Demo Board Only					
1	23	E1-E18, E20-E23, E25	TEST POINT, TURRET, 0.094" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0		
2	11	J1-J7, J9-J12	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4		
3	1	J16	CONN., HDR, SHROUDED, MALE, 2×6, 2mm, VERT, ST, THT	AMPHENOL, 98414-G06-12ULF		
4	5	JP1-JP4, JP9	CONN., HDR, MALE, 1×3, 2mm, VERT, ST, THT, NO SUBS. ALLOWED	WURTH ELEKTRONIK, 62000311121		
5	4	JP5-JP8	CONN., HDR, MALE, 2×2, 2mm, VERT, ST, THT, 10µ Au	SAMTEC, TMM-102-02-L-D		
6	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.25" (6.4mm)	KEYSTONE, 8831		
7	1	PCB1	PCB, DC3164A	ANALOG DEVICES APPROVED SUPPLIER, 600-DC3164A		
8	9	XJP1-XJP9	CONN., SHUNT, FEMALE, 2-POS, 2mm	WURTH ELEKTRONIK, 60800213421		

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	07/23	Initial Release.	_

DEMO MANUAL DC3164A-B



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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