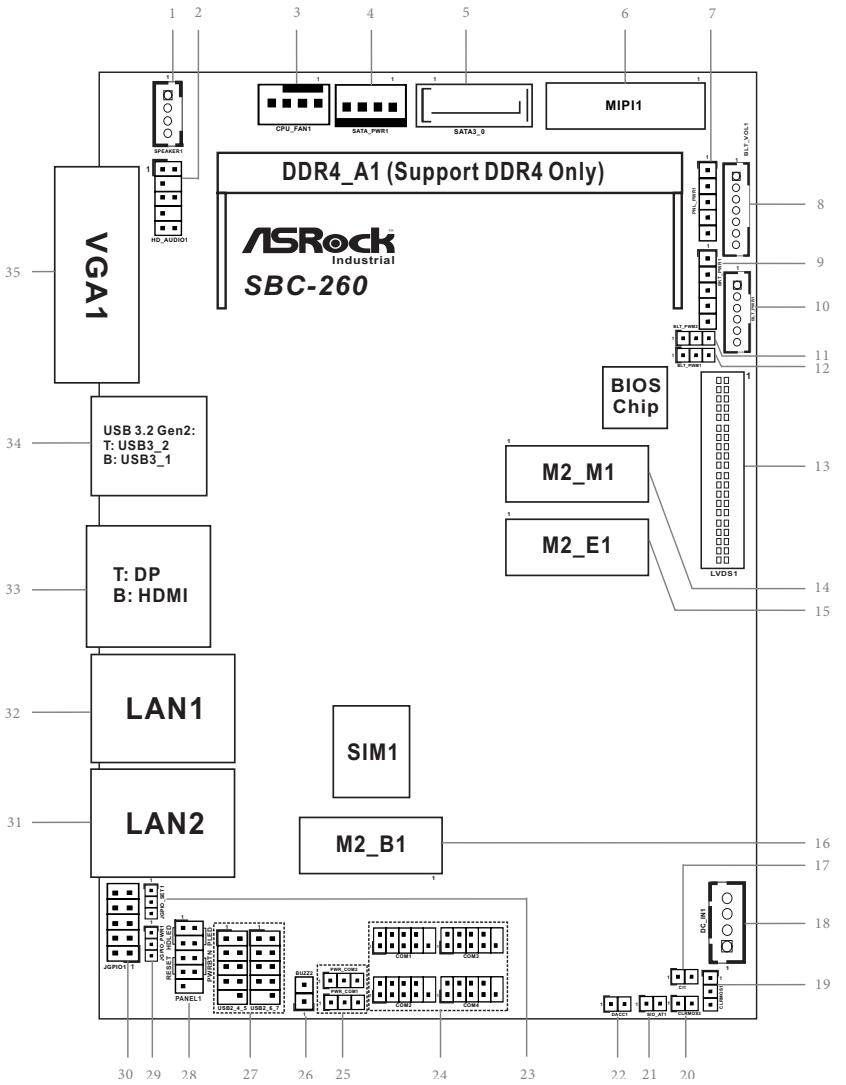
Jumpers and Headers Setting Guide

SBC-260

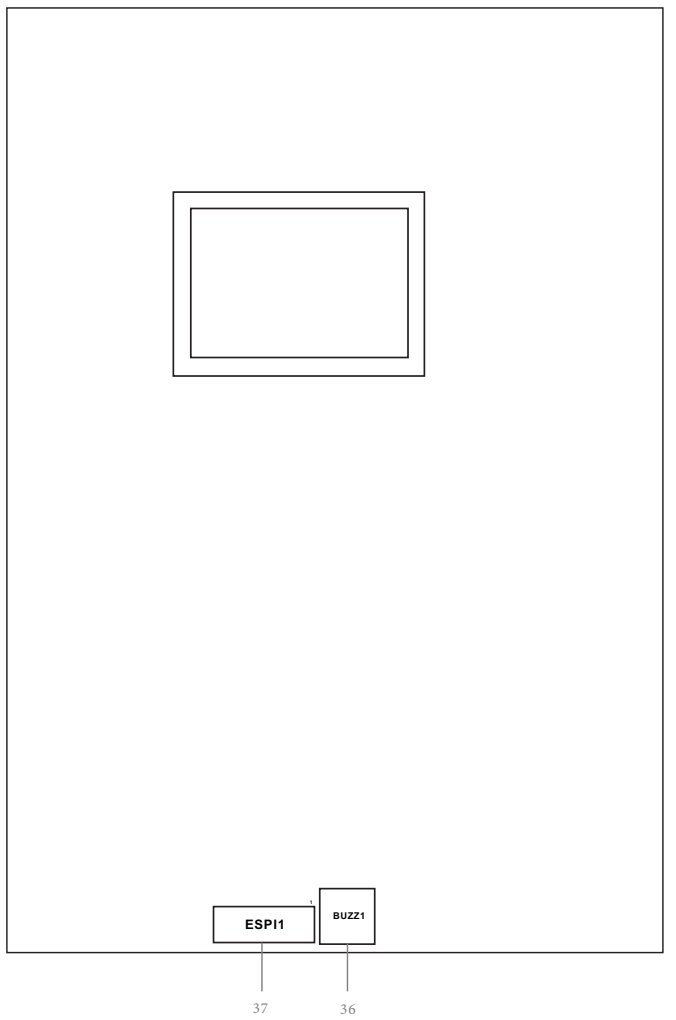
Revision History

Date	Description
February 17, 2023	First Release
July 13, 2023	Second Release

Top:



Bottom:

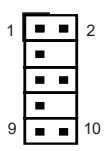


1 : 3W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	SPK L-
2	SPK L+
3	SPK R+
4	SPK R-

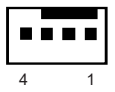
2 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	MIC1_L	GND	2
3	MIC1_R		4
5	OUT2_R	MIC1_RET	6
7	J_SENSE		8
9	OUT2_L	OUT_RET	10



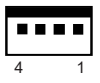
3 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL



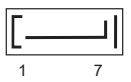
4 : SATA Power Output Connector (SATA_PWR1)

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V

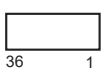


5 : SATA3 Connector (SATA3_0)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B-
6	SATA-B+
7	GND



6 : MIPI Connector (MIPI1)



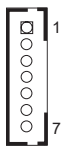
Pin	Signal Name
1	GND
2	CSI_B_DN2
3	CSI_B_DP2
4	GND
5	CSI_B_DN1
6	CSI_B_DP1
7	GND
8	CSI_B_CLK_N
9	CSI_B_CLK_P
10	GND
11	CSI_B_DN0
12	CSI_B_DP0
13	CSI_B_DN3
14	CSI_B_DP3
15	GND
16	GND
17	+2.8V
18	GND
19	+2.8V
20	+1.8V
21	+1.2V
22	GND
23	IMBCLKOUT0
24	GND
25	I2C1_SCL
26	I2C1_SDA
27	N/C
28	BUF_PLT_RST_1.8_R_N
29	N/C
30	GND
31	N/C
32	+1.2V
33	GND
34	GPP_S1
35	GPP_S2
36	GPP_S3

7 : Panel Power Select (LCD_VCC) (PNL_PWR1)

1-2 : +3V (Default)
2-3 : +5V
3-4 : +5V
4-5 : +12V

8 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	GPIO_VOL_UP
2	GPIO_VOL_DW
3	PWRDN
4	BRIGHTNESS_UP
5	BRIGHTNESS_DW
6	GND
7	GND

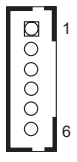


9 : Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2 : LCD_BLT_VCC: +5V (Default)
2-3 : LCD_BLT_VCC: +12V
4-5 : LCD_BLT_VCC: DC_IN

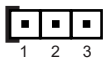
10 : Inverter Power Control Wafer (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	BL CTL
4	BL EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC



11 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)

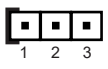
1-2 : 3V Level (Default)
2-3 : 5V Level



12 : Brightness Control Mode (BLT_PWM1)

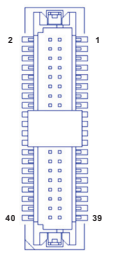
1-2 : From eDP PWM to CON_LBKLT_CTL
2-3 : From LVDS PWM to CON_LBKLT_CTL (Default)

• Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.
• Please set to 2-3 when adjusting brightness by BLT_VOL1.



13 : LVDS Panel Connector (LVDS1)

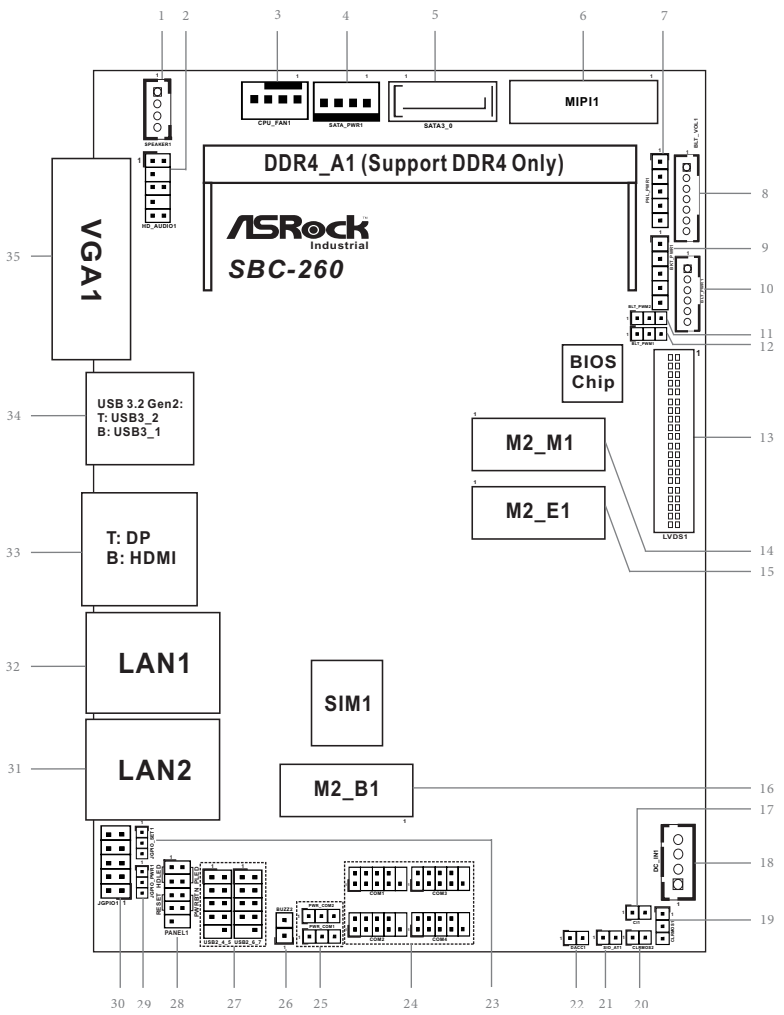
Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	N/A	4
5	N/A	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	GND	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	NC	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40



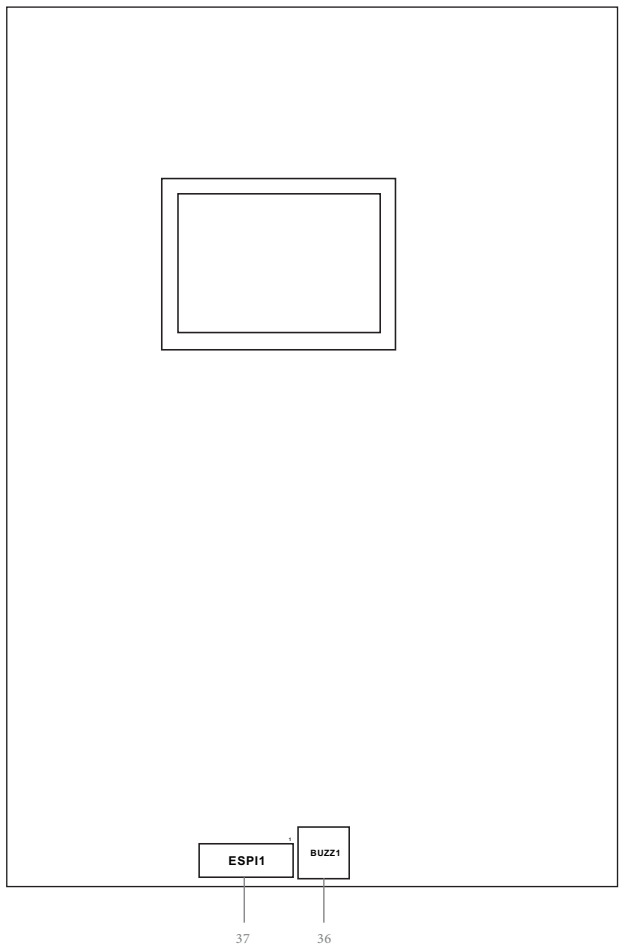
* eDP by pass mode pin definition:

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	N/A	N/A	4
5	N/A	N/A	6
7	N/A	GND	8
9	EDP_TX1#	EDP_TX1	10
11	GND	EDP_TX0#	12
13	EDP_TX0	GND	14
15	N/A	N/A	16
17	GND	EDP_AUXN	18
19	EDP_AUXP	GND	20
21	N/A	N/A	22
23	GND	N/A	24
25	N/A	GND	26
27	N/A	N/A	28
29	DPLVDD_EN	N/A	30
31	N/A	GND	32
33	N/A	N/A	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

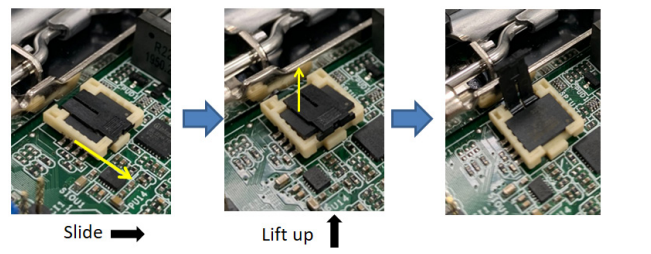
Top:



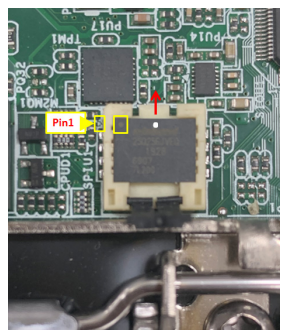
Bottom:



Installation of ROM Socket



- Do not apply force to the actuator cover after ic inserted.
- Do not apply force to actuator cover when it is opening over 120 degree, Otherwise, the actuator cover may be broken.



- The yellow dot (Pin1) on the ROM must be installed at pin1 position of the socket (white arrow area).
- Make sure the white dot on the ROM is installed outwards of the socket.
- For further details of how to install ROM, please refer to ASRI website.

Warning: If the installation does not follow as the picture, then it may cause severe damage to chipset & MB.

14 : M.2 Key-M Socket (M2_M1)

PIN	SIGNAL	SIGNAL	PIN
1	GND	+3.3V	2
3	GND	+3.3V	4
5	NA	NA	6
7	NA	NA	8
9	GND	SATA_LED	10
11	NA	+3.3V	12
13	NA	+3.3V	14
15	GND	+3.3V	16
17	NA	+3.3V	18
19	NA	NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	NA	26
27	GND	NA	28
29	NA	NA	30
31	NA	NA	32
33	GND	NA	34
35	NA	NA	36
37	NA	NA	38
39	GND	NA	40
41	PERn0/SATA-B+	NA	42
43	PERp0/SATA-B-	NA	44
45	GND	NA	46
47	PETn0/SATA-A-	NA	48
49	PETp0/SATA-A+	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

15 : M.2 Key-E Socket (M2_E1)

PIN	SIGNAL	SIGNAL	PIN
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
33	GND	CNV_BGI_DT	32
35	PETp	CNV_RGI_RSP	34
37	PETn	CNV_BRI_DT	36
39	GND	NA	38
41	PERp	NA	40
43	PERn	NA	42
45	GND	NA	44
47	PEFCLKp	NA	46
49	PEFCLKn	NA	48
51	GND	SUSCLK	50
53	CLKREQ#	PERST0#	52
55	NA	W_DISABLE1#	54
57	GND	W_DISABLE2#	56
59	CNV_WT_D1-	SMB_DATA	58
61	CNV_WT_D1+	SMB_CLK	60
63	GND	NA	62
65	CNV_WT_D0-	NA	64
67	CNV_WT_D0+	NA	66
69	GND	NA	68
71	CNV_WT_CLK-	NA	70
73	CNV_WT_CLK+	+3.3V	72
75	GND	+3.3V	74

16 : M.2 Key-B Socket (M2_B1)

PIN	SIGNAL	SIGNAL	PIN
1	NA	+3.3V	2
3	GND	+3.3V	4
5	GND	FuLL_Card_Power_off	6
7	USB_D+	W_DISABLE1#	8
9	USB_D-	WWAN_LED#	10
11	GND		
21	GND	NA	20
23	NA	NA	22
25	NA	NA	24
27	GND	W_DISABLE2#	26
29	USB3_RX-	NA	28
31	USB3_RX+	UIM_RESET	30
33	GND	UIM_CLK	32
35	USB3_TX-	UIM_DATA	34
37	USB3_TX+	UIM_PWR	36
39	GND	NA	38
41	PERn0	NA	40
43	PERP0	NA	42
45	GND	NA	44
47	PETn0	NA	46
49	PETP0	NA	48
51	GND	PERST#	50
53	PEFCLKn	CLKREQ#	52
55	PEFCLKp	NA	54
57	GND	NA	56
59	NA	NA	58
61	NA	NA	60
63	NA	NA	62
65	NA	NA	64
67	NA	NA	66
69	PEDET	NA	68
71	GND	+3.3V	70
73	GND	+3.3V	72
75	NA	+3.3V	74

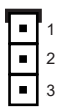
17 : Chassis Intrusion Header (CI1)

Open : Normal (Default)
Short : Active Case Open

18 : 4-pin DC-in PWR Connector

(Input +9V~+36V)
1-4 : GND
2-3 : DC Input

19 : Clear CMOS Header (CLRMOS1)



1-2 : Normal (Default)
2-3 : Clear CMOS

20 : Auto Clear CMOS Header (CLRMOS2)

Open : Normal (Default)
Short : Auto Clear CMOS When AC Powr On

21 : SIO_AT1

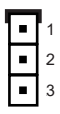
Open : ATX Mode (Default)
Short : AT Mode

22 : DACC1

Open : No ACC
Short : ACC (Default)

* Auto clear CMOS when system boot improperly.

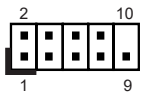
23 : GPIO Default Setting (JGPIO_SET1)



1-2 : Pull-High (Default)
2-3 : Pull-Low

24 : COM1, 2, 3, 4 Headers*

Pin	Signal Name	Signal Name	Pin
1	DDCD#1	RRXD1	2
3	TTXD1	DDTR#1	4
5	GND	DDSR#1	6
7	RRTS#1	CCTS#1	8
9	RRI#1		10

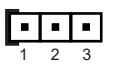


* This motherboard supports RS232/422/485 on COM1, 2 ports. Please refer to below table for the pin definition. In addition, COM1, 2 ports (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM1, 2 Port Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	N/A
4	DTR	RX-	N/A
5	GND	GND	GND
6	DSR	N/A	N/A
7	RTS	N/A	N/A
8	CTS	N/A	N/A
9	N/A	N/A	N/A

25 : COM Port Pin9 PWR Setting Jumpers



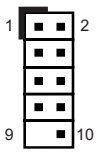
PWR_COM2 (For COM Port2)
PWR_COM1 (For COM Port1)
1-2 : +5V (Default)
2-3 : +12V

26 : 2-Pin Buzzer Header (BUZZ2)

Pin	Signal Name
1	BUZZ+
2	BUZZ-

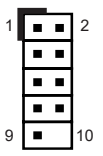
27 : USB2.0 Connectors (USB2_4_5, USB2_6_7)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	P-	P-	4
5	P+	P+	6
7	GND	GND	8
9		DUMMY	10

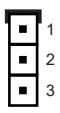


28 : System Panel Header

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	DUMMY		10



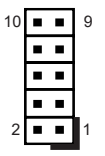
29 : Digital Input / Output Power Select (JGPIOPWR) (JGPIO_PWR1)



1-2 : +12V
2-3 : +5V (Default)

30 :Digital Input / Output Pin Header (JGPIO1)

Pin	Signal Name	Signal Name	Pin
1	SIO_GP34	TIME_SYNC0	2
3	SIO_GP35	GPP_E1	4
5	SIO_GP36	GPP_E2	6
7	SIO_GP37	GPP_E13	8
9	JGPIO_PWR	GND	10



- Time-Aware GPIO support at Pin 2

31 : LAN Port (LAN2)
32 : LAN Port (LAN1)
33 : Top : DisplayPort (DP)
Bottom : HDMI Port (HDMI)
34 : Top : USB3.2 Gen2 Port (USB3_2)
Bottom : USB3.2 Gen2 Port (USB3_1)
35 : VGA Port (VGA1)

<u>Backside :</u>

36 : Buzzer (BUZZ1)
37 : ESPI Connector (ESPI1) →

Pin	Signal Name
1	GND
2	C_ESPI_CLK
3	GND
4	C_ESPI_CS#
5	DEBUG_RESET
6	GND
7	+3V
8	GND
9	SMB_CLK_MAIN
10	SMB_DATA_MAIN
11	C_ESPI_IO0
12	C_ESPI_IO1
13	C_ESPI_IO2
14	C_ESPI_IO3
15	GND
16	+3VSB
17	N/A
18	N/A
19	C_ESPI_ALERT#
20	GND