Tektronix

PCIe 5.0/6.0 TRX Test Solution

Anritsu VIP Showcase

Tektronix Session-AE/Jacky Huang

PCI Express 5.0 Specification Status

Technology brief

- **The Design & Compliance problem**
  - Physical size of SoCs remain approximately constant, bandwidth increases are primarily achieved by increasing the speed (data rate) of data per pin. Issues related to higher speeds – such as **loss, cross talk and reflections** – all become more pronounced as data rates increase
  - For system designers, significant signal integrity experience is required to support the latest **networking protocols like 400GbE.**

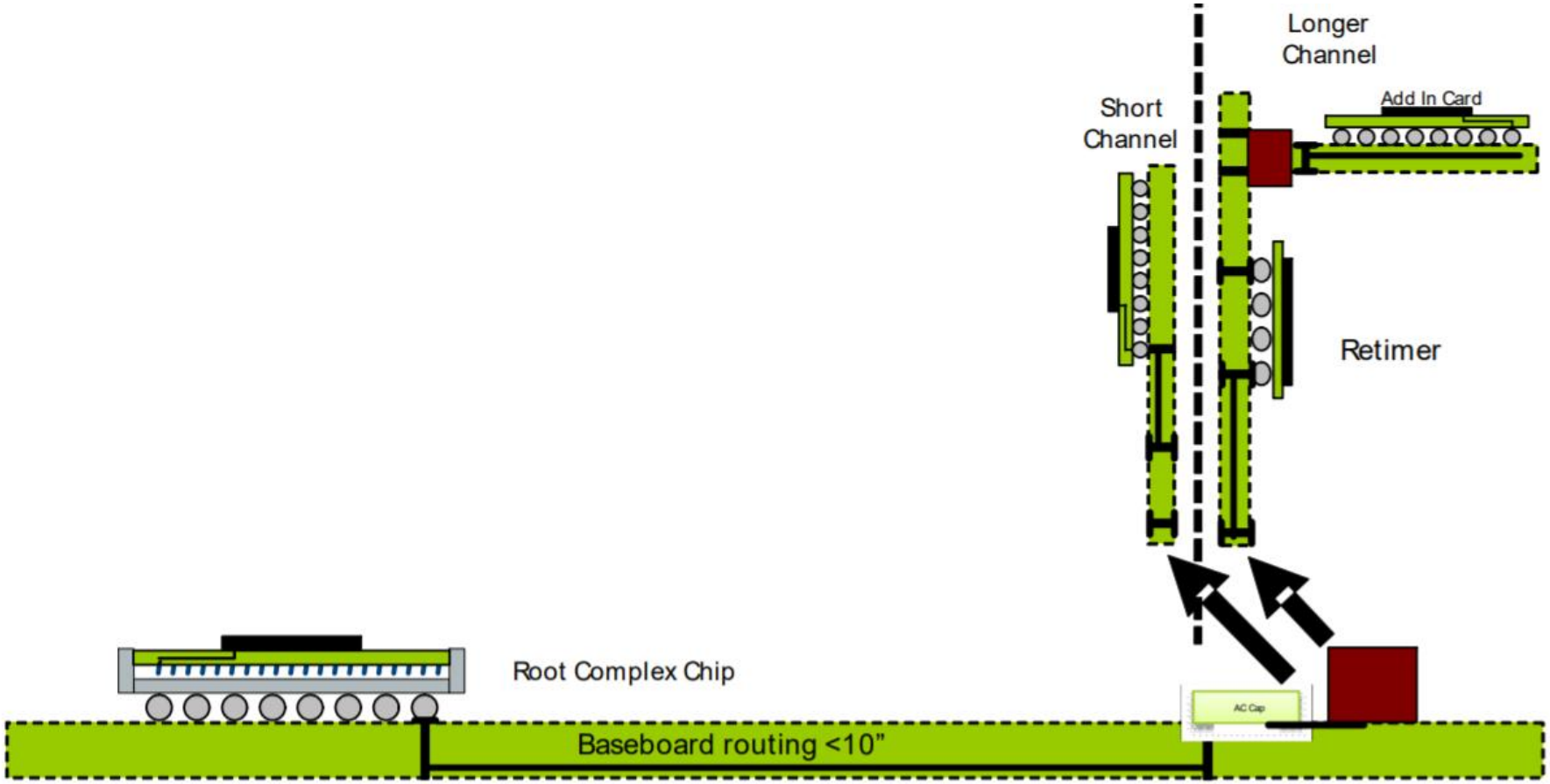
	Bit Rate / Lane	Link BW	Lane BW	x16 bi BW
PCIe 1.x	2.5 GT/s	2.0 Gb/s	250 MB/s	8 GB/s
PCIe 2.x	5.0 GT/s	4.0 Gb/s	500 MB/s	16 GB/s
PCIe 3.x	8.0 GT/s	8.0 Gb/s	~1 GB/s	32 GB/s
PCIe 4.x	16.0 GT/s	16.0 Gb/s	~2 GB/s	64 GB/s
PCIe 5.x	32.0 GT/s	32.0 Gb/s	~4 GB/s	128 GB/s
PCIe 6.x	64.0 GT/s	64 Gb/s	~8 GB/s	256 GB/s

PCIe 4.0 to 6.0 Base Specification Updates

Parameters	PCIe 4.0	PCIe 5.0	PCIe 6.0
Data Rate	16 GT/s	32 GT/s	64 GT/s (PAM4)
Add-in Card Loss	8dB @ 8Ghz	9.5dB @ 16GHz	~ 8.5dB @ 16GHz
Rx Test (Channel Loss)	- (27 to 30) dB @ 8GHz	- (34 to 37) dB @ 16GHz	- (30 to 33) dB @ 16GHz
Reference CTLE	2 Poles; 1 Zero; DC Gain Range (-6 to -12) dB	4 Poles; 2 Zero; DC Gain Range (-5 to -15) dB	6 Poles; 3 Zero; DC Gain Range (-5 to -15) dB
Reference DFE	2-Taps	3-Taps	16-Taps
Eye Width (Rx Test)	18.75 ps	9.375 ps	3.125 ps (top eye)
Eye Height (Rx Test)	15 mV	15 mV	6 mV (top eye)
Lane Margining	Required timing only	Required timing/voltage	Required timing/voltage
Refclk Jitter Limits	<= 500 fs	<= 150 fs	<=100 fs

Increase in complexity of PCIe specifications

PCIe 5.0 Channel Solution Space



- End to end loss target ~= 36 dB
- Root Package loss ~= 9 dB
- Add-in Card Package loss (Non root) ~= 4 dB

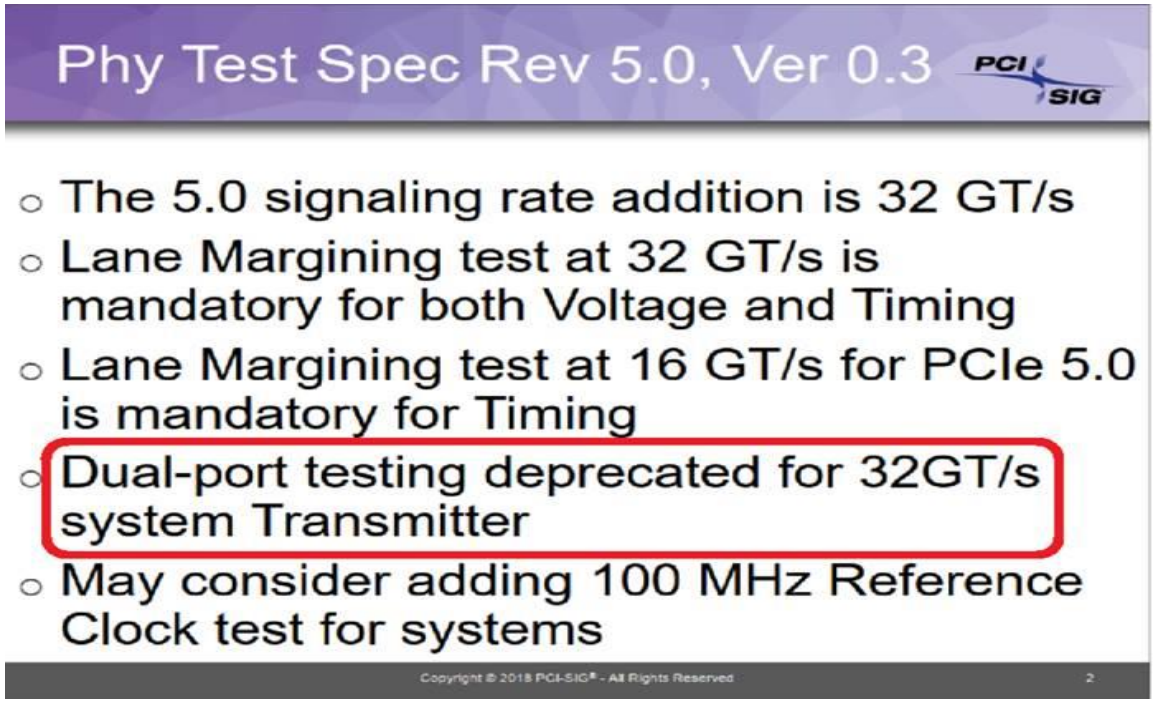
PCIe 5.0 Specification Snapshot

- **PCIe 5.0 Base Specification – Rev 1.0 Released (Q2 2019)**
  - Describes chip-level behavior on all levels of the stack
- **PCIe 5.0 CEM Specification – Rev 1.0 Released (Q2 2021)**
  - Card electro-mechanical (CEM) defines system and Add-in Card level
- **PCIe 5.0 PHY Test Specification – Rev 1.0 Released (Q1 2022)**
  - Describes electrical compliance tests for Tx, Rx LEQ, Refclk & PLL Bandwidth
- **PCIe 4.0 – All Specifications at Rev 1.0**
  - Integrators List testing began August 2019

PCI Express 5.0 CEM Tx

PCIe Gen 5 TX CEM

DUAL PORT TESTING REMOVAL



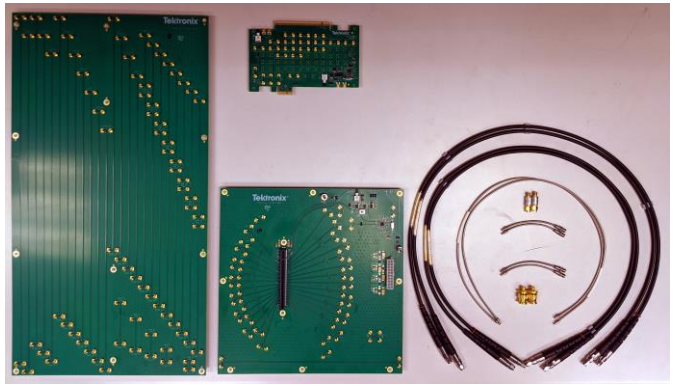
- CEM workgroup voted in March 2020 to remove the Dual Port Requirement for 5.0 System Tx requirement
- Workgroup exploring a new 5.0 System refclk jitter compliance test
- Systems at 32 GT/s will be tested with the same CDR & reference Rx EQ algorithms as 32 GT/s Add-in Cards
- Only 2 scope channels needed!

PCI Express CEM Tx Eye Mask

	PCIe 5.0 Base Spec Eye Limits	CEM 5.0 Eye Limits
System TX	EH=15mV	17.5mV (2.5mV↑)
	EW=0.3UI, 9.375ps	0.31 UI, 9.688 ps (1%UI↑)
AIC TX	EH=15mV	22 mV (7mV↑)
	EW=0.3UI, 9.375ps	0.34 UI, 10.625 ps (4 %UI↑)

Tektronix Gen5 Tx Solution Status

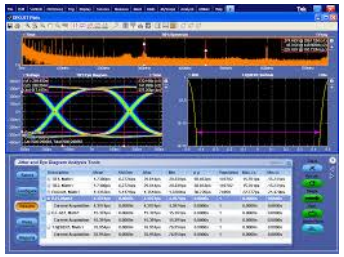
- PCI Express 5.0 Base Tx – Released Q1 2020
- PCI Express 5.0 CEM Tx – Released Q1 2021
  - Currently Gen5 CEM compliance fixtures available from PCI-SIG



PCIe Gen5 Solution Landscape

Debug

DPOJET Plugin for Debug



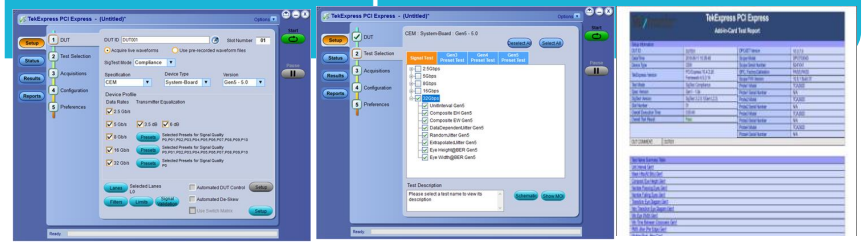
SDLA

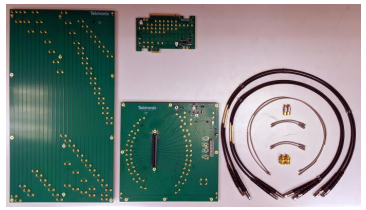
Transmitter

- Base
- CEM
- Ref CLK

SigTest Phoenix

TekExpress PCE5



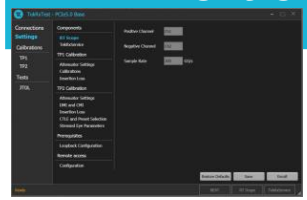


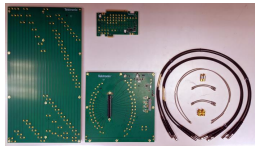
Receiver

BASE	CEM
TP3-TP2	TP3-TP2
JTOL	JTOL / Rx/Tx LEQ

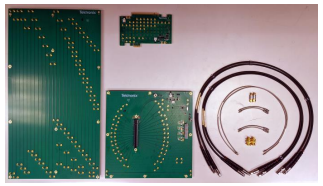
Seasim & SigTest Phoenix

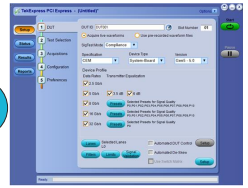
Tektronix Rx automation

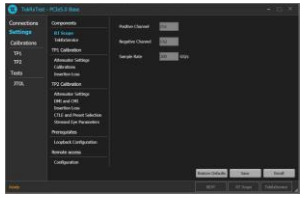




Complete PCIe Gen5 Portfolio offering Tx + Rx







Tektronix PCIe Gen5 Solution Offering

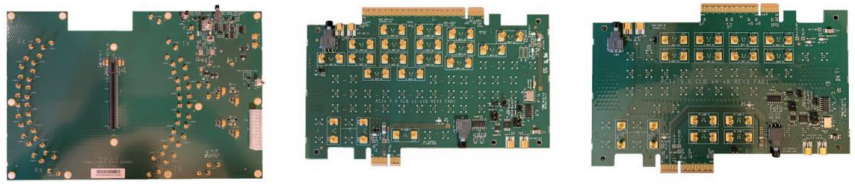
SUMMARY

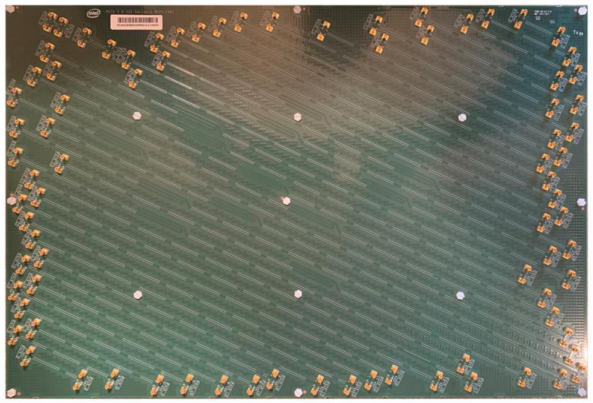
Transmitter		
	Item	**Status**
HW	BW ≥33GHz DX/SX Scope	Available
	Arbitrary Function Generator[1]	Available
	Gen5 CEM Test Fixtures [2]	Available
SW	TekExpress Gen5 Tx	Available
	TekExpress Gen4 Tx	Available
	TekExpress Gen1/2/3 Tx	Available
	DPOJET	Available
	SDLA	Available

Receiver		
	Item	**Status**
HW	≥20Gbps BERT[3]	Available
	Dual Stack ≥50GHz Sx Scope	Available
	Gen5 CEM Test Fixtures [2]	Available
SW	Tektronix PCI Express Receiver Test Suite	Available
	DPOJET	Available
	SDLA	Available

[1]Optional automated DUT Tx pattern toggling.
[2] PCI-SIG Fixture - Available from PCI-SIG
[3]BERT from Anritsu, link: https://www.anritsu.com/en-US/test-measurement/products/mp1900a
[3]Error Detector and Clock Recovery requires for the USB3.2 Receiver testing

Gen 5 Test Fixtures





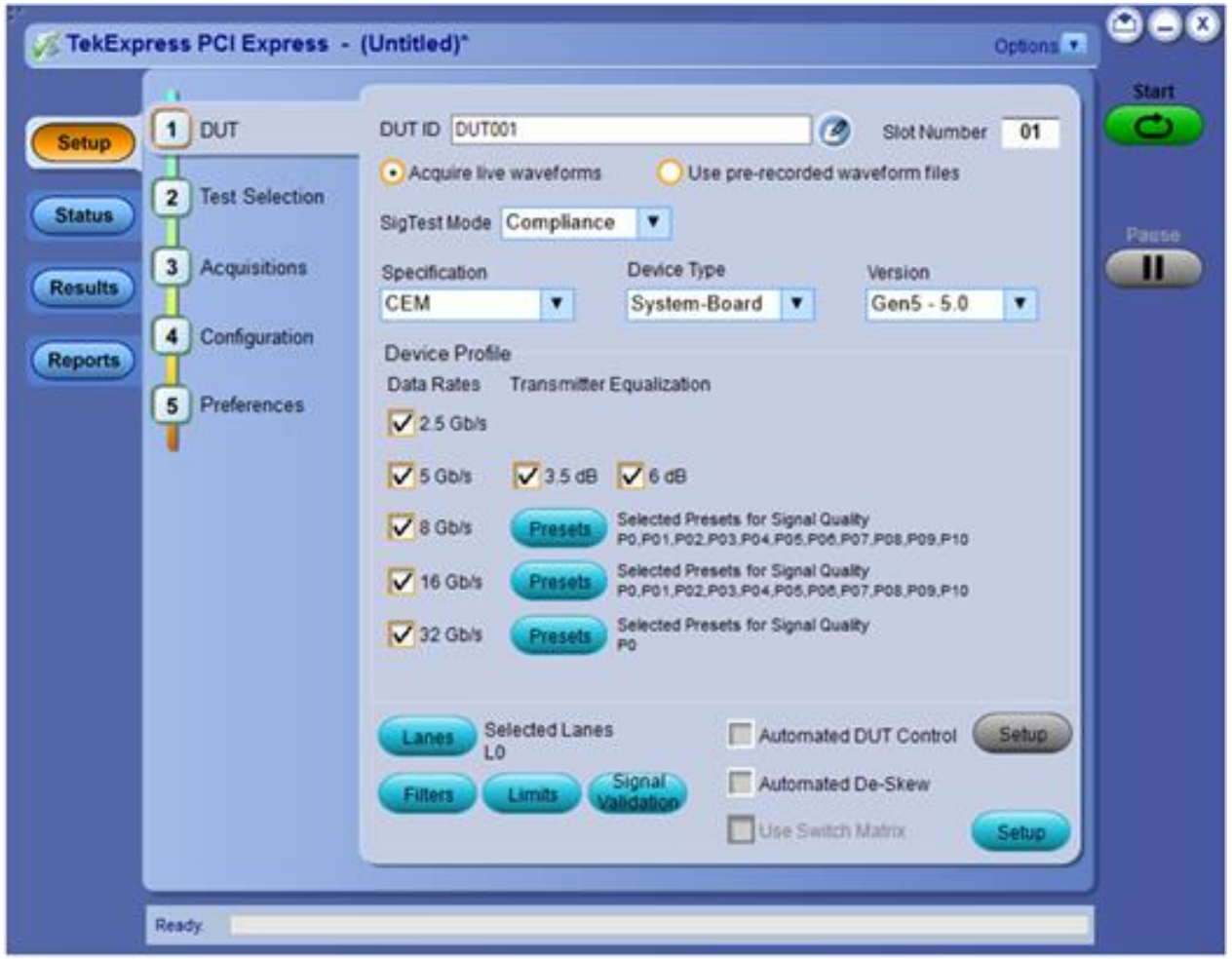
- **Official Gen5 CEM Compliance Fixtures**
  - Built by Intel & sold through PCI-SIG
  - Available to SEG members June 2021 and available to full PCI-SIG members now
  - RF Connectors – MMPX (Huber Suhner)
  - PCB – Meg6

- **Tektronix Fixtures**
  - Gen5 CEM NON-OFFICIAL Fixture available for purchase December 2020
  - Insertion Loss Spec & Return Loss Mask met
  - Successfully closed Gen5 CEM Rx Calibration & tested with Gen5 System & AIC
  - Variable ISI Board
    - Step sizes of 0.5dB & 16GHz
    - Rx Calibration – Used to dial in 34dB to 37dB channel
    - Tx Signal Quality – Used to dial in loss of link partner (9.5dB AIC or 26.5dB System)
      - PCI-SIG may decide to use embedding instead of physical ISI

Transmitter Test Software

TEKEXPRESS

- Compliance of PCIe Gen1/2/3/4/5 based on PCIe Base and CEM specs
- Automated acquisition & waveform management
- Automated DUT control
- De-embed channel, test fixtures, and cables
- User-selectable test selection.
- Integrated waveform validation & SigTest (Phoenix) analysis
- Comprehensive test reporting

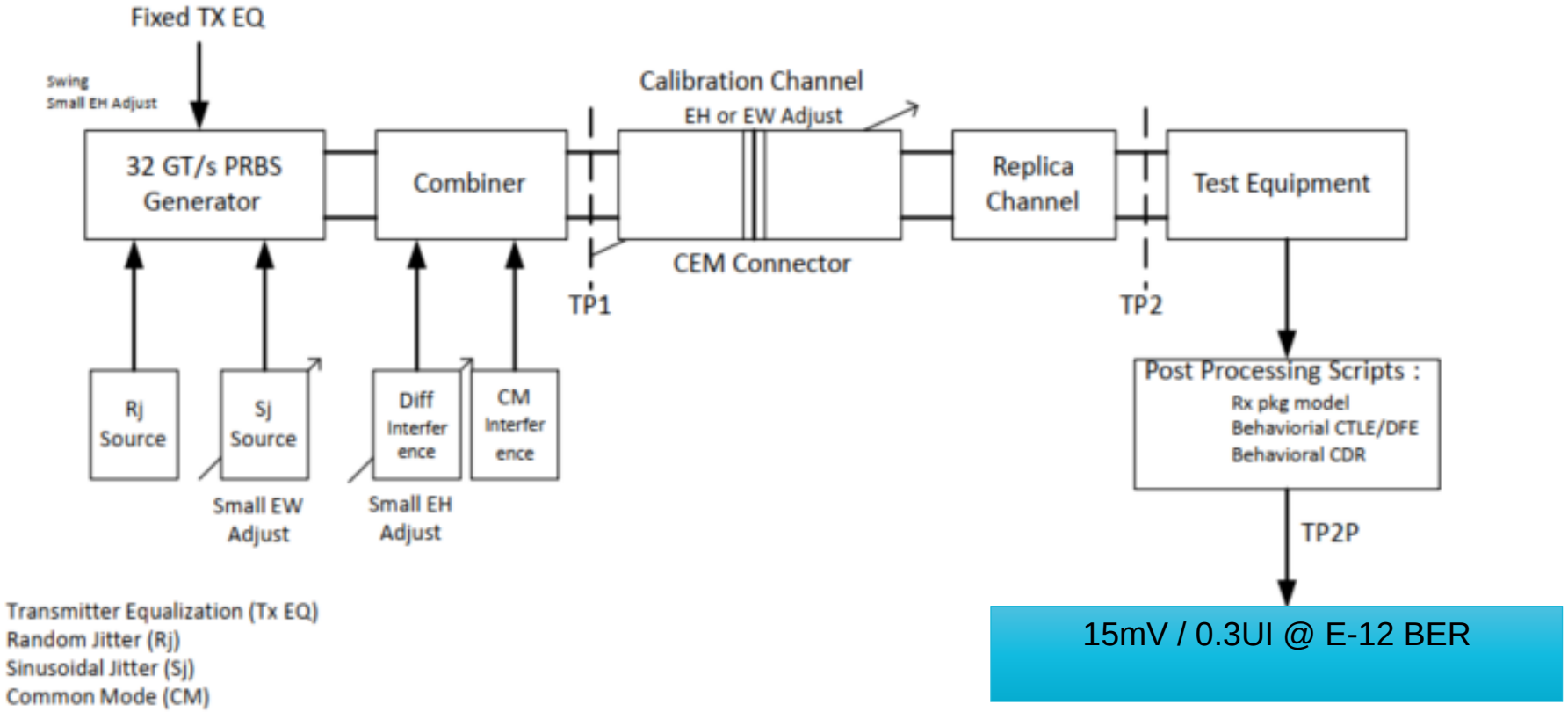


Transmitter Software Features

- Compliance and advanced analysis modes
- User-selectable SigTest version for each PCIe data rate
- Reduced & full swing voltage tests
- Jitter, voltage, preset, and eye diagram tests via SigTest (Phoenix)
- Analysis and debug tools if failures encountered
- Comprehensive programmatic interface for automation of tests

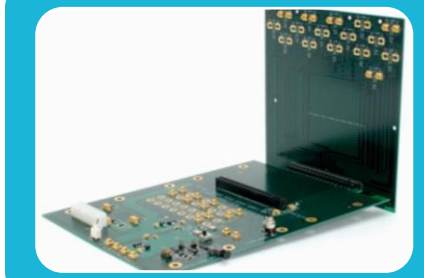
PCI Express 5.0
32GT/s Rx PG Calibration & Test

32GT/s Rx Calibration



Transmitter Equalization (Tx EQ)
Random Jitter (Rj)
Sinusoidal Jitter (Sj)
Common Mode (CM)
Eye Width (EW)
Eye Height (EH)
Test Point (TP)

Rx Calibration Evolution



8GT/s Rx Calibration

- Fixed Channel Loss (package embedded with SigTest)
- Knobs – Rj/DMI (often results in unrealistic Rj values – no bounds)
- Only CEM fixtures for sale through PCI-SIG
- Seasim (Base) & SigTest (CEM)

16GT/s Rx Calibration

- Variable ISI (27 to 30dB) – improved test equipment correlation
- Knobs – Amplitude/Sj/DMI (with allowable ranges defined)
- Limit BASE fixtures for sale through PCI-SIG & implementation note in BASE Spec
- Seasim/SigTest (Base) & SigTest (CEM)

32GT/s Rx Calibration

- Variable ISI (34 to 37dB)
- Knobs – Same as 16GT/s
- Base Rev2 fixtures under development (MMPX coaxial connector)
- Seasim (Base) –& SigTest EH Extrapolation under investigation & noise impact

PCI Express 5.0 Tx/Rx setup details

Configuration details

Setup Details

Tektronix Solution Configuration

PCIE GEN5 BASE TX

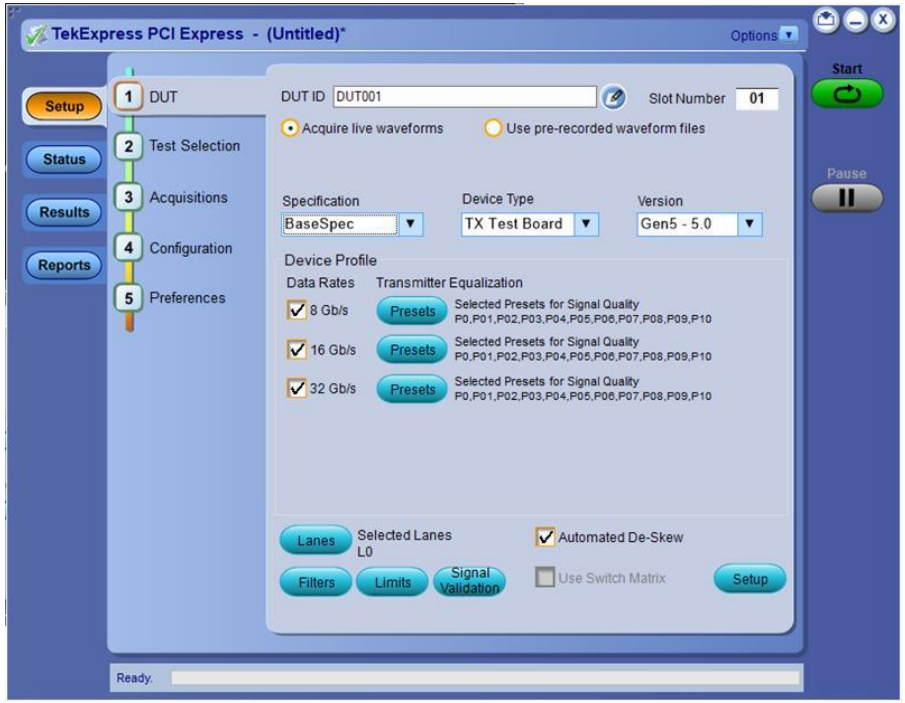
Description	Tek P/N	QTY	Manufacturer	Req/Opt	Comments
Dual Stack 50GHz Sx Scope	DPS75004SX	1	Tektronix	Required	50G or better *
Attenuator Kit	DPO7RFK2	2	Tektronix	Required	Attenuator kit + DC Blocks
Connector Savers (1.85mm)	103047400	2	Tektronix	Required	1.85mm scope channel input connection
TekExpress Gen5 Tx	PCE5	1	Tektronix	Required	TekExpress Gen5 Tx
TekExpress Gen4 Tx	PCE4	1	Tektronix	Required	TekExpress Gen4 Tx
Require for B6:I6PPG output & Scope input	PCE3	1	Tektronix	Required	TekExpress Gen1/2/3 Tx
DPOJET Advanced option	DJA	1	Tektronix	Required	DPOJET advanced option
Serial Data Link Analysis Software	SDLA64	1	Tektronix	Required	Serial Data Link Analysis Software
Cable; 2.92-to-2.92mm, Straight, 1.5ps phase-matched, 40GHz	PMCABLE1M	2 pairs	Swiftbridge	Required	DUT to replica & replica to scope **

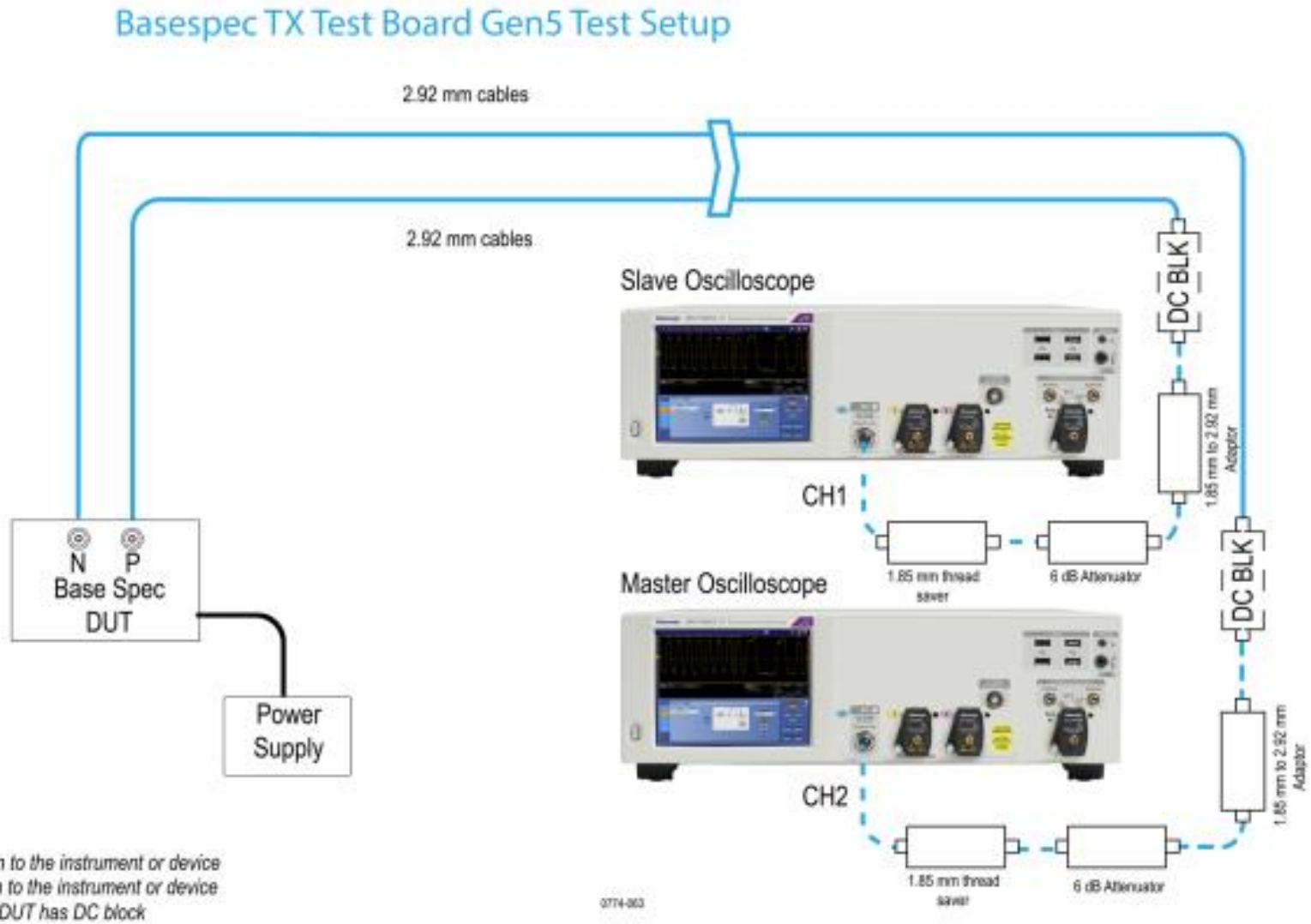
* If ATI channels will be used for refclk measurements they will need Option Key 4 (50XL)

** Additional adaptors may be needed if eval & replica boards are not 2.92mm compatible

Tektronix Solution Configuration

TEST SYSTEM VIEW PCIE GEN5 BASE TX





Tektronix Solution Configuration

PCIE GEN5 CEM TX

Description	Tek P/N	QTY	Manufacturer	Req/Opt	Comments
Dual Stack 50GHz Sx Scope	DPS75004SX	1	Tektronix	Required	50G or better *
Attenuator Kit	DPO7RFK2	2	Tektronix	Required	Attenuator kit + DC Blocks
Connector Savers (1.85mm)	103047400	2	Tektronix	Required	1.85mm scope channel input connection
TekExpress Gen5 Tx	PCE5	1	Tektronix	Required	TekExpress Gen5 Tx
TekExpress Gen4 Tx	PCE4	1	Tektronix	Required	TekExpress Gen4 Tx
TekExpress Gen1/2/3 Tx	PCE3	1	Tektronix	Required	TekExpress Gen1/2/3 Tx
DPOJET Advanced option	DJA	1	Tektronix	Required	DPOJET advanced option
Serial Data Link Analysis Software	SDLA64	1	Tektronix	Required	Serial Data Link Analysis Software
Arbitrary Function Generator	AFG31252	1	Tektronix	Optional	For automated DUT Tx pattern toggling
BNC to SMA Adaptor	015-0572-00	1	Tektronix	Optional	For automated DUT Tx pattern toggling
USB 2.0 Cable - Type A to Type B Male; 6ft	174-6053-01	1	Tektronix	Optional	Required when using AFG31252 for preset toggling
Cable; SMA - SMP cable pair	174-6659-01	1 pair	Tektronix	Optional	For AFG connection to DUT Rx Lane 0 (toggling)
Cable; 2.92-to-2.92mm, Straight, 1.5ps phase-matched, 40GHz	PMCABLE1M	1 pair	Swiftbridge	Required	DUT Tx to Scope
Cable; SMP-to-SMP, Right Angle, 2.5ps phase-matched	174-6658-xx	1 pair	Tektronix	Required	For Manual DUT Preset Toggling
SMP 50 Ohm Terminator	131-9399-xx	**	Tektronix	Required	**
ATX Power Supply for System Board Power	ATX Power Supply	1	Corsair	Required	Required for System DUT power
Gen 5 CEM Test Fixtures (with MMPX cables) ***	TF−PCIE5−CEM−X16	1	Tektronix or PCI-SIG	Required	Tektronix fixtures are not officially approved by PCI-SIG ****

* If ATI channels will be used for refclk measurements they will need Option Key 4 (50XL)

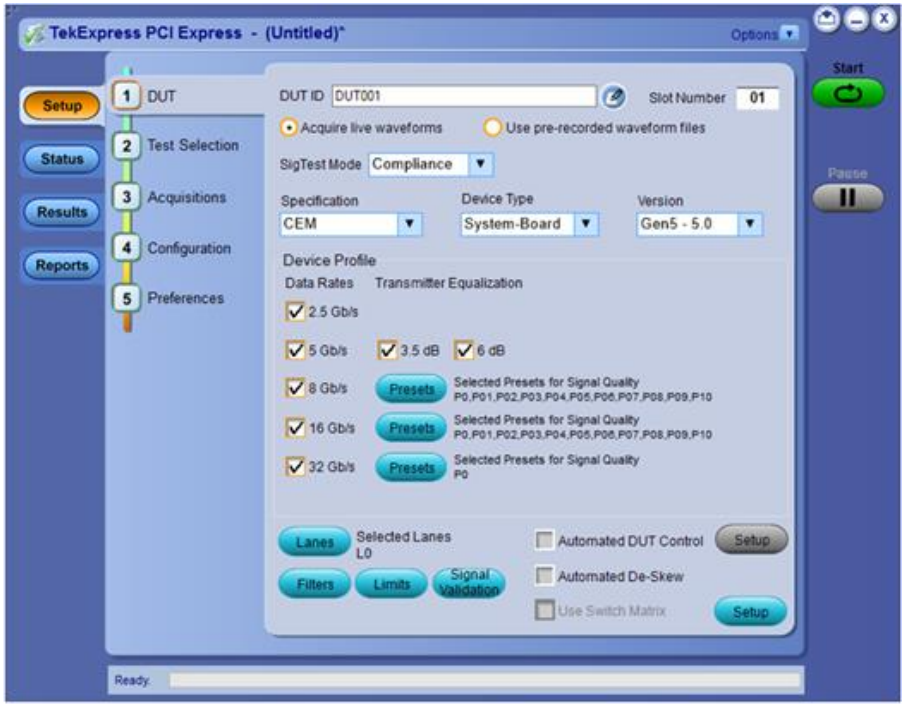
** Quantity depends upon the link width to be tested: x1 = Qty 0, x4 = Qty 6, x8 = Qty 14, x16 = Qty 30

*** Gen5 CEM Test Fixtures are expected to be backwards compatible for Gen1/2/3/4 Tx, if not then Gen4 fixtures may be required

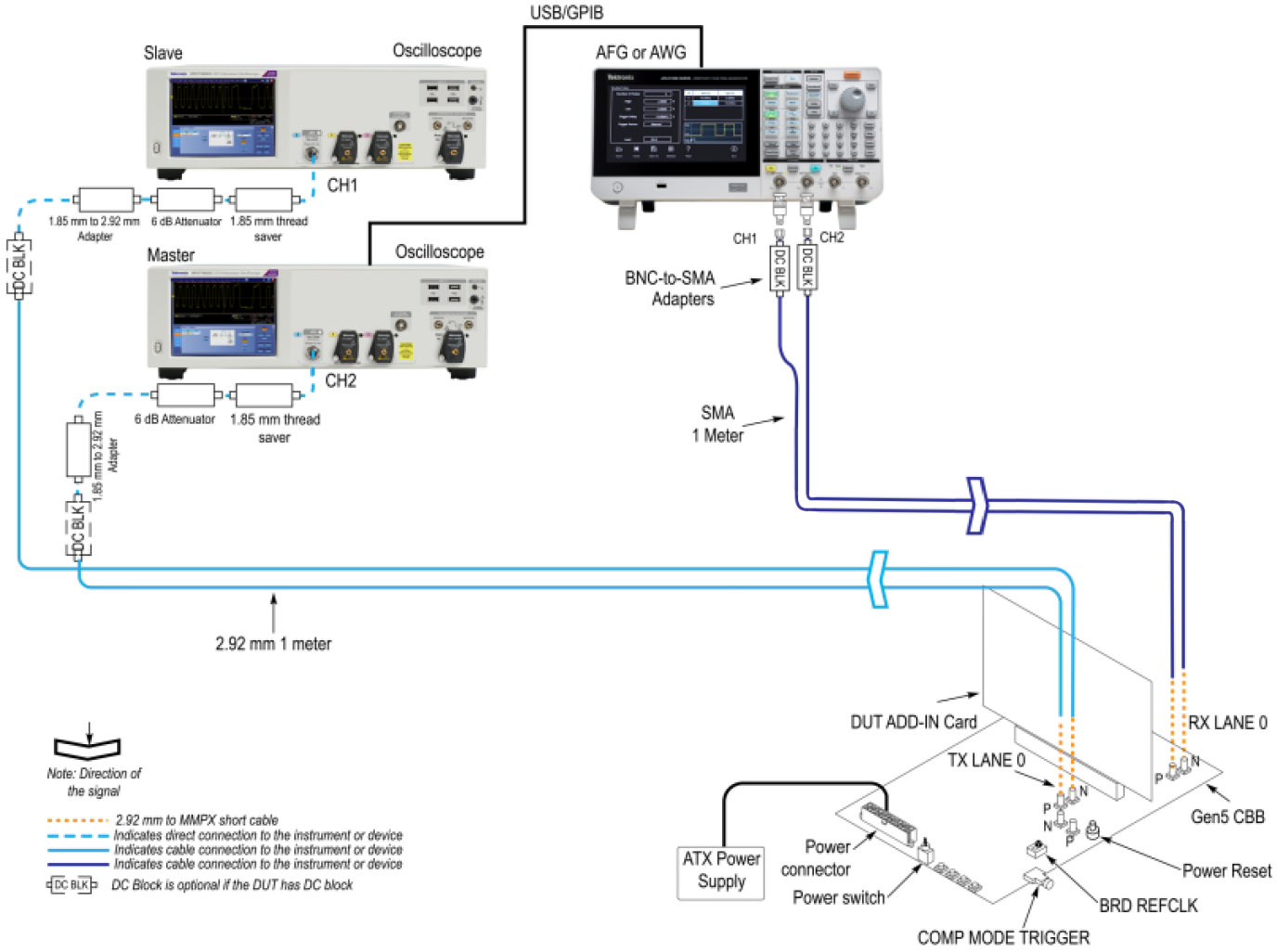
**** It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit

Tektronix Solution Configuration

TEST SYSTEM VIEW PCIE GEN5 CEM TX



CEM Add-In Card Gen5 Test With Automatic Toggle Mode Setup



Tektronix Solution Configuration

PCIE GEN5 BASE RX

Description	Tek P/N	QTY	Manufacturer	Req/Opt	Comments
Dual Stack 50GHz Sx Scope	DPS75004SX	1	Tektronix	Required	50G or better
Attenuator Kit	DPO7RFK2	2	Tektronix	Required	Attenuator kit + DC Blocks
Connector Savers (1.85mm)	103047400	2	Tektronix	Required	1.85mm scope channel input connection
Bit Error Rate Tester (BERT) *	**	1	3rd Party	Required	Configuration provided by 3rd Party **
Tektronix PCIe Gen5 Rx CEM and BASE Automation SW	RXSW-xxx-PCIE5	1	Tektronix	Required	Available under CAA until 30th Jan 2021
DPOJET Advanced option	DJA	1	Tektronix	Required	DPOJET advanced option
Serial Data Link Analysis Software	SDLA64	1	Tektronix	Required	Serial Data Link Analysis Software
Cable; SMA - SMP cable pair (1000mm)	174-6659-01	1 pair	Tektronix	Required	Refclk connection between DUT & BERT
Cable; 2.92-to-2.92mm, Straight, 1.5ps phase-matched, 40GHz (1000 mm)	PMCABLE1M	2 pairs	Swiftbridge	Required	Equipment connections to relica channel & DUT
Gen 5 Base Rev3 Test Fixtures ***	TBD	1	PCI-SIG	Required	Rev3 is Meg6 material with MMPX connectors ****

* Cables required for connection between BERT modules shall be included for the 3rd party vendor

** Configuration for BERT provided by 3rd party vendor

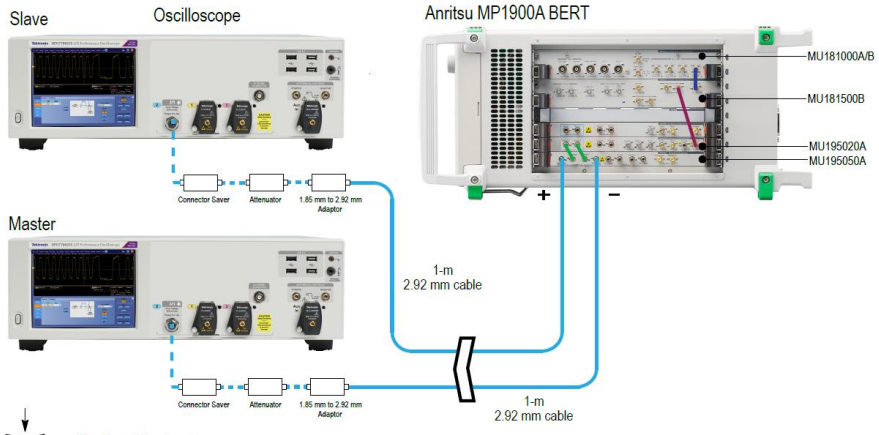
*** Gen5 BaseTest Fixtures are not backwards compatible for Gen3 & Gen4 Base Rx

**** It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit

Tektronix Solution Configuration

TEST SYSTEM VIEW GEN5 BASE RX CAL + TEST SETUP

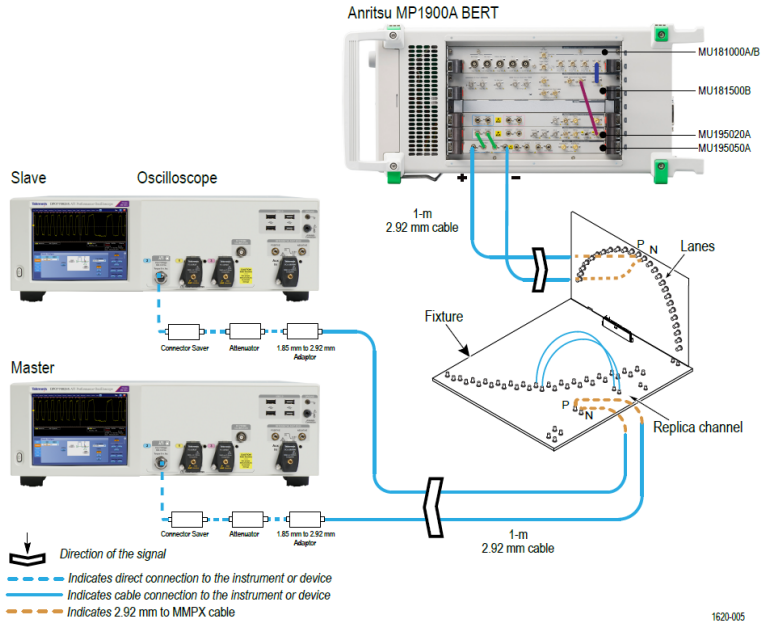
TP1 Calibration setup



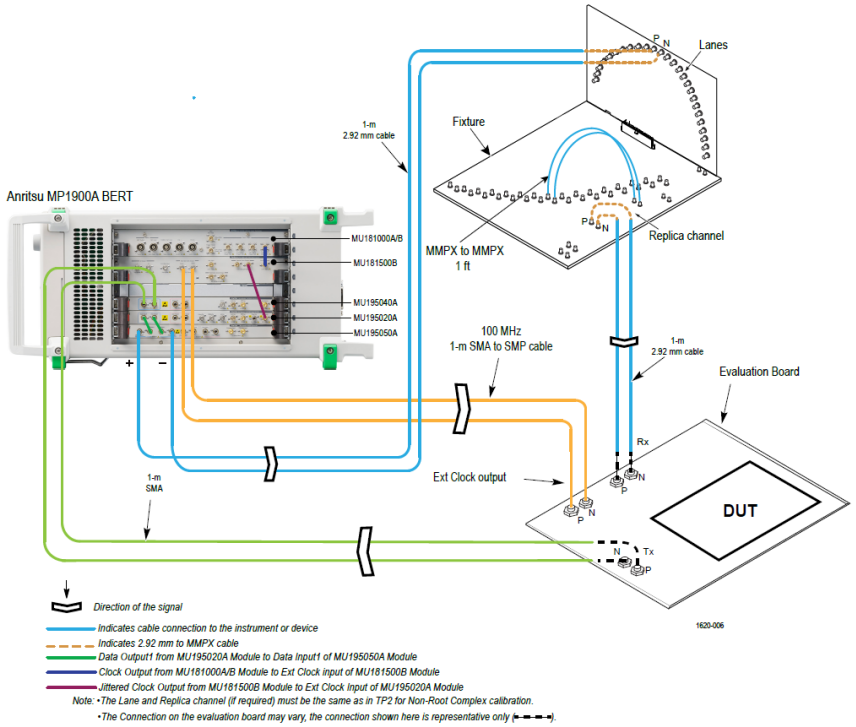
Tektronix Receiver Solution

TP2 Calibration setup

SYS/AIC



BER Tests



Tektronix Solution Configuration

PCIE GEN5 CEM RX

Description	Tek P/N	QTY	Manufacturer	Req/Opt	Comments
Dual Stack 50GHz Sx Scope	DPS75004SX	1	Tektronix	Required	50G or better
Attenuator Kit	DPO7RFK2	2	Tektronix	Required	Attenuator kit + DC Blocks
Connector Savers (1.85mm)	103047400	2	Tektronix	Required	1.85mm scope channel input connection
Bit Error Rate Testor (BERT) *	**	1	3rd Party	Required	Configuration provided by 3rd Party **
Tektronix PCIe Gen5 Rx CEM and BASE Automation SW	RXSW-xxx-PCIE5	1	Tektronix	Required	Available under CAA until 30th Jan 2021
DPOJET Advanced option	DJA	1	Tektronix	Required	DPOJET advanced option
Serial Data Link Analysis Software	SDLA64	1	Tektronix	Required	Serial Data Link Analysis Software
Cable; 2.92-to-2.92mm, Straight, 1.5ps phase-matched, 40GHz (1000 mm)	PMCABLE1M	2 pr	Tektronix	Required	Equipment connection to fixtures and DUT
Cable; 2.92-to-2.92mm, Straight, 1.5ps phase-matched, 500mm, 40GHz (500 mm)	174-6663-01	1 pr	Tektronix	Required	Signal Connection between scope and BERT for Tx LEQ
Cable; SMA-to-SMA, Right Angle-Right Angle, (500mm)	174-6666-01	2 pr	Tektronix	Required	Signal Connection between scope and BERT for Tx LEQ & Trigger
Cable; SMA - SMP cable pair (1000 mm)	174-6659-01	1 pr	Tektronix	Required	Refclk connection between DUT & BERT
Power Divider	MPR40M	2	Fairview Microwave	Required	Split signal from DUT Tx to the scope and Error Detector
Right Angle Male-Female 2.92mm adapter	C7035	4	CentricRF	Optional	Cable management
2.92mm Male to 2.92mm Male Adaptor	C7049	3	CentricRF	Required	Power divider output to scope input
Active Gen5 Redriver (back channel equalization) ***		1	Texas Instrument	Optional	High loss back channels (DUT Tx to Error Detector) may need EQ
Power USB Power Strip	PowerUSB - Basic	1	PowerUSB	Optional	Automate DUT power cycle
Gen 5 CEM Test Fixtures ****	TF–PCIE5–CEM–X16	1	Tektronix or PCI-SIG	Required	Tektronix fixtures are not officialy approved by PCI-SIG *****

* Cables required for connection between BERT modules shall be included for the 3rd party vendor

** Configuration for BERT provided by 3rd party vendor

*** Another matched pair of cables (e.g. 174-6663-xx) will be required if the Active redriver is used for Rx or Tx LEQ

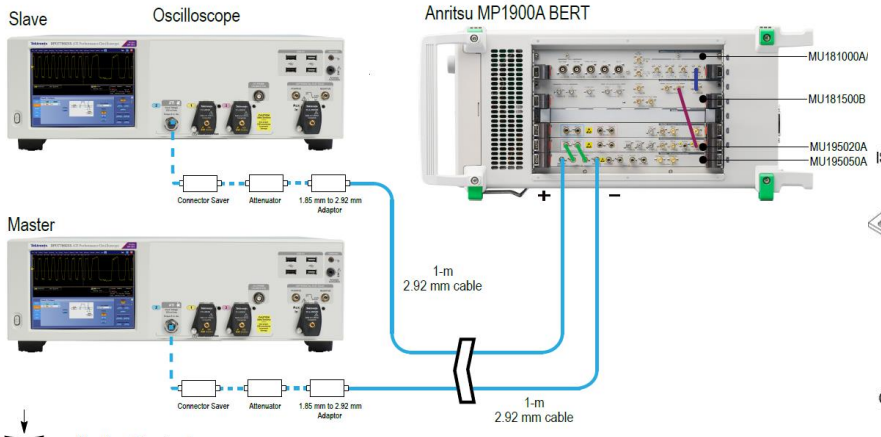
**** Gen5 BaseTest Fixtures are not backwards compatible for Gen3 & Gen4 Base Rx

***** It is assumed MMPX cables and MMPX to SMA adaptor cables for test fixture connections are included with the fixture kit

Tektronix Solution Configuration

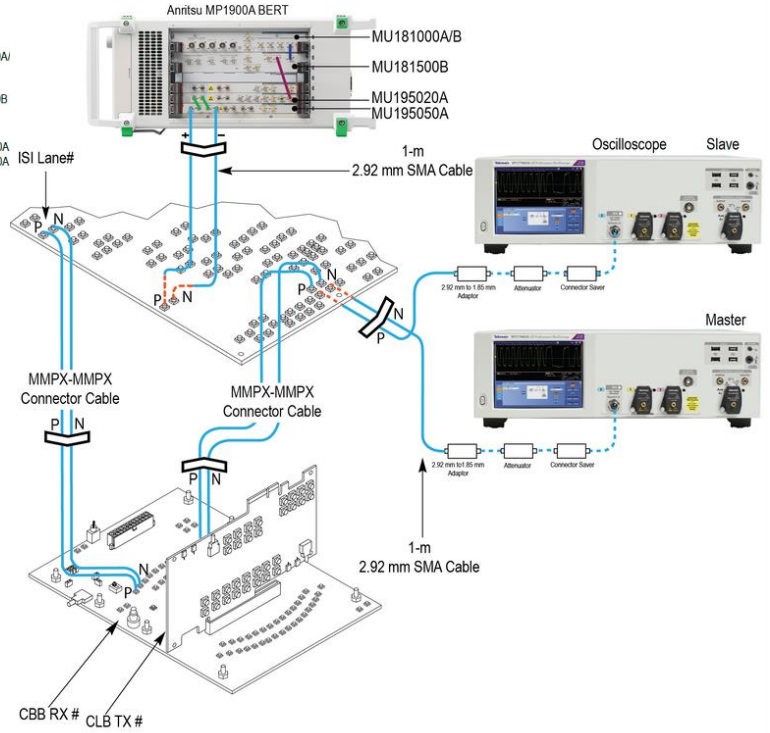
TEST SYSTEM VIEW GEN5 CEM RX CALIBRATION

TP1 Calibration

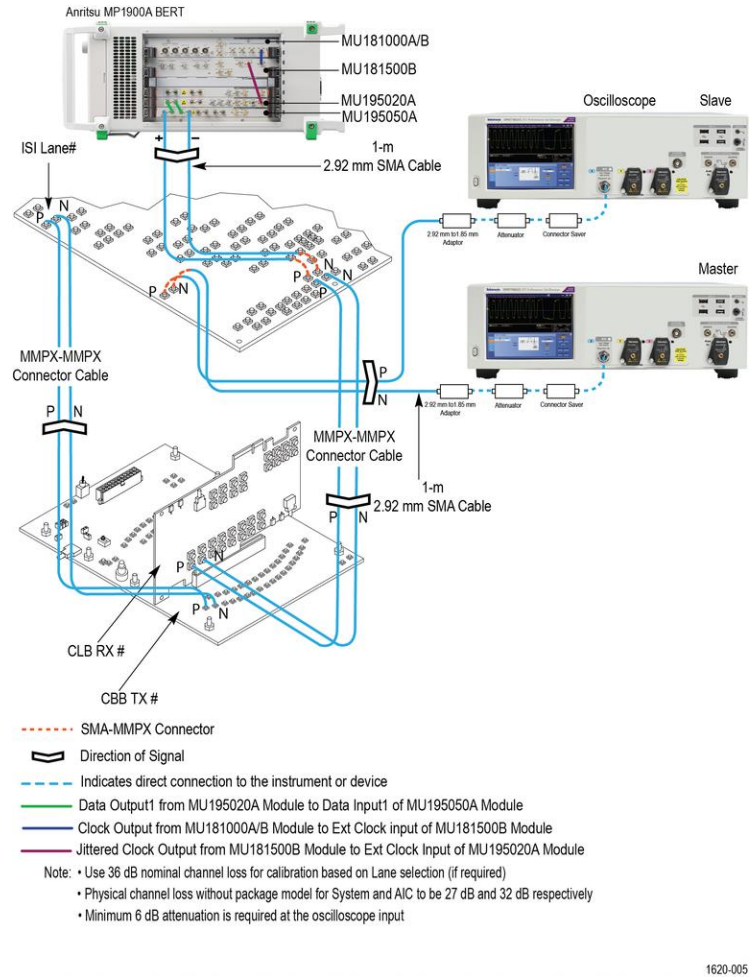


Tektronix Receiver Solution

TP2 AIC Calibration



TP2 SYS Calibration

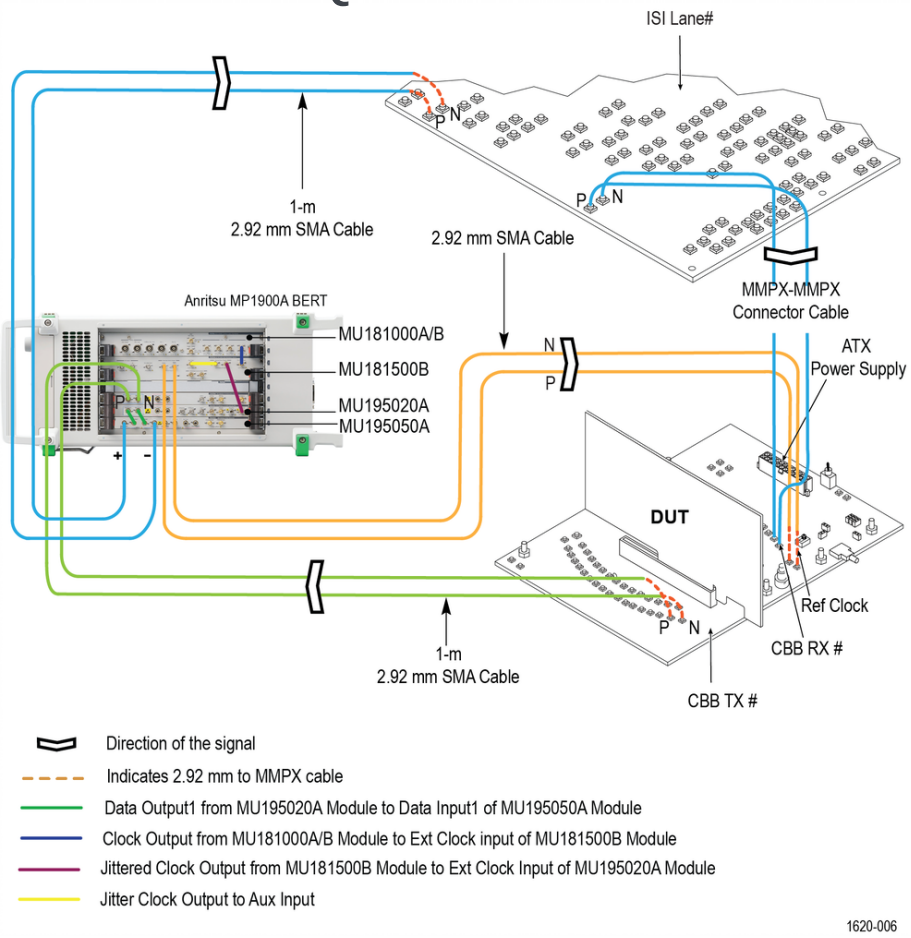


Tektronix Solution Configuration

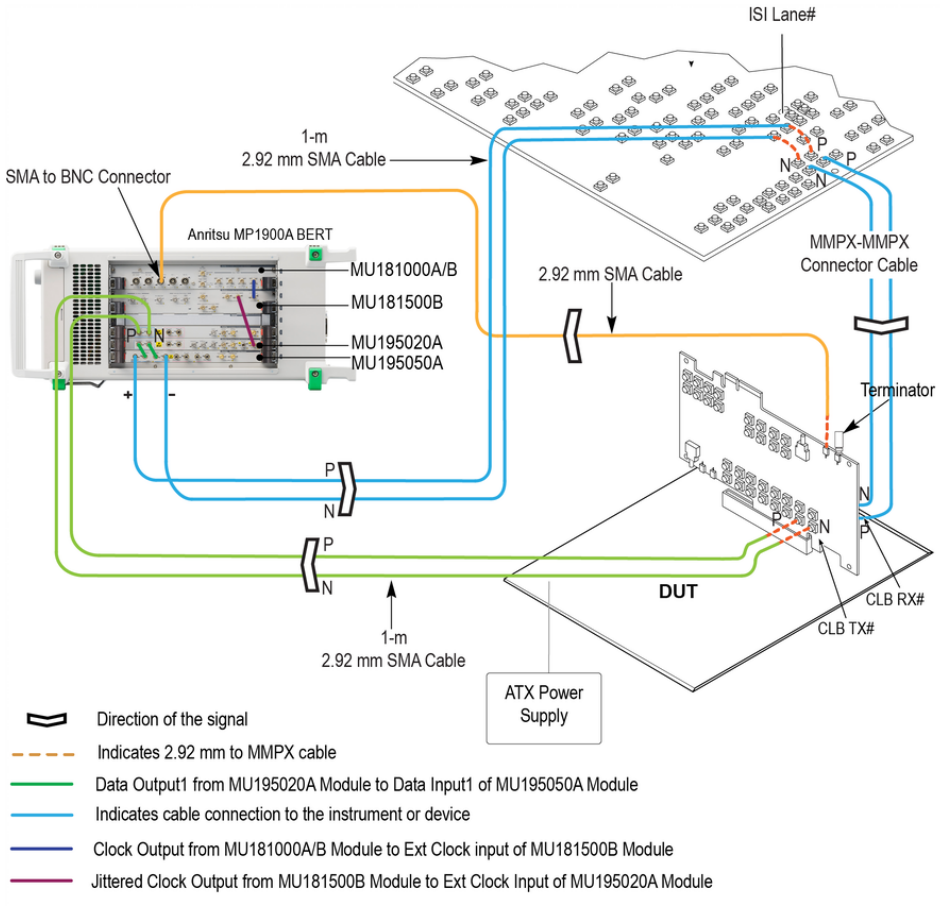
TEST SYSTEM VIEW GEN5 CEM RX TEST

Tektronix
Receiver Solution

RX LEQ AIC Tests



RX LEQ SYS Tests



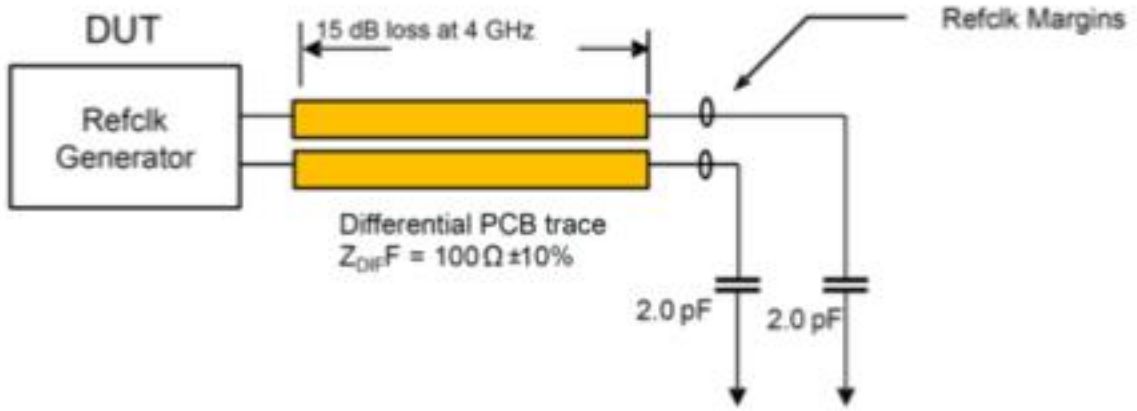
PCI Express 5.0 Refclk Jitter Measurements

Reference Clock Phase Jitter Test

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73	BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73	BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15
BW_{CDR}(min) = 10 MHz, 1st order	64 combinations				8.0, 16.0 GT/s

Ref CLK requirements for PCIe 5.0 have become more stringent and testing methodologies have changed

Spec Revision	Data Rate	Refclk Component Max Jitter	
Gen1	2.5 **GT/s**	86 ps	PTP
Gen2	5.0 **GT/s**	3.1 ps	RMS
Gen3	8.0 **GT/s**	1.0 ps	RMS
Gen4	16.0 **GT/s**	0.5 ps	RMS
Gen5	32.0 **GT/s**	0.15 ps	RMS
Gen6	64.0 **GT/s**	0.10 ps	RMS



Tektronix – PCI Express 5.0 Refclk Solution

- Fully Automated Solution – TekExpress with Skyworks Clock Jitter Tool
- Targeted Support
  - High Frequency Jitter Measurements (Gen1 to Gen5)
    - Optional scope Noise removal algorithm
  - Refclk DC Specifications and AC Requirements
  - Data Rate Independent Refclk Parameters
- Real Time Scopes (>=5G BW to meet CEM Spec.)
  - DPO70K Scope
  - MSO64 or MSO64B

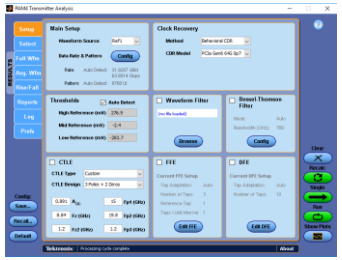
PCI Express 6.0 Specification Status

PCIe 6.0 Specification Snapshot (Q3 2022)

- **PCIe 6.0 Base Specification – Rev 1.0 Released**
  - Describes chip-level behavior on all levels of the stack
- **PCIe 6.0 CEM Specification – Rev 0.5 under development**
  - Card electro-mechanical (CEM) defines system and Add-in Card level
- **PCIe 6.0 PHY Test Specification – Rev 0.5 under development**
  - Describes electrical compliance tests for Tx, Rx LEQ, Refclk & PLL Bandwidth

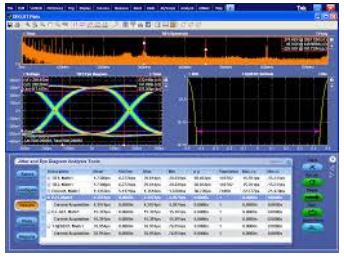
Tektronix PCIe Gen6 Solution Landscape

PAMJET (PAM4 Analysis)



SDLA

DPOJET Plugin for Debug



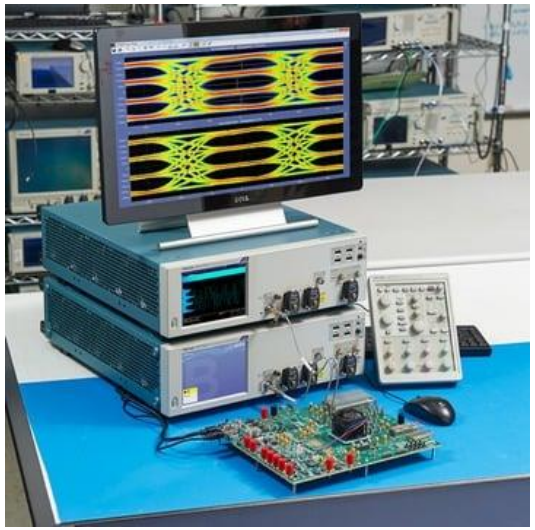
Tektronix Innovative Gen6 DSP Tools

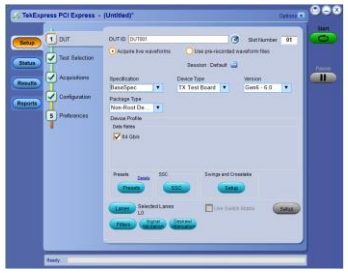
Transmitter

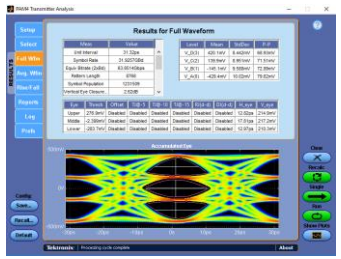
Base | CEM | Ref CLK

PAMJET + DPOJET + SDLA

TekExpress Automation





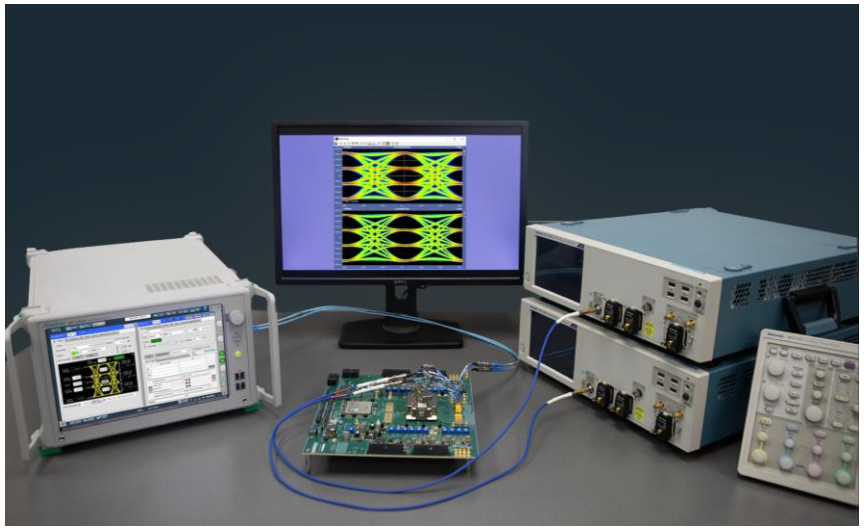


Receiver

Base | CEM

Calibration | JTOL

Tektronix Rx Automation



Released

Upcoming / to be announced

Early Gen6 Rx Customer Engagements

Active PCI-SIG & industry participation

PCI- SIG Developer Conference 2022

- First physical DevCon since 2019 and added live stream of presentations.
- Joint demonstration with Anritsu, Synopsys & Tektronix on Gen6 Rx!
- Electrical Deep session led by Tektronix! : **850** attendees

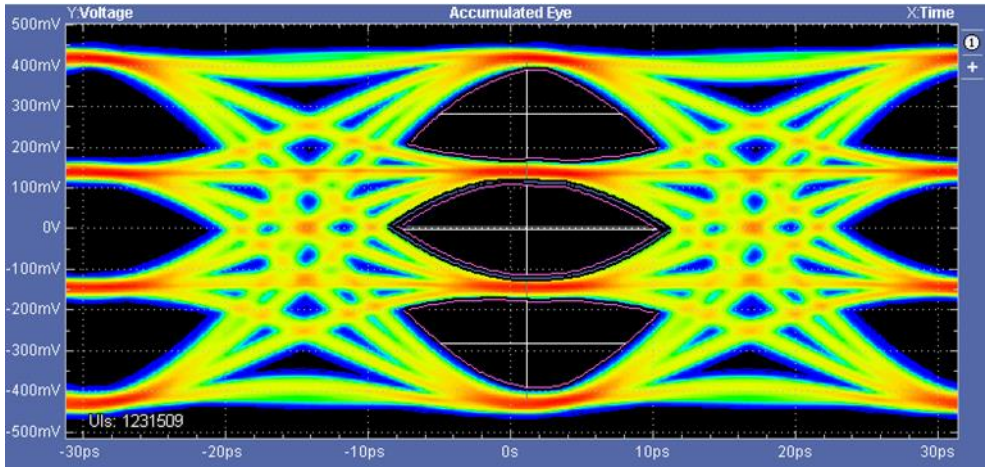
Customer engagement

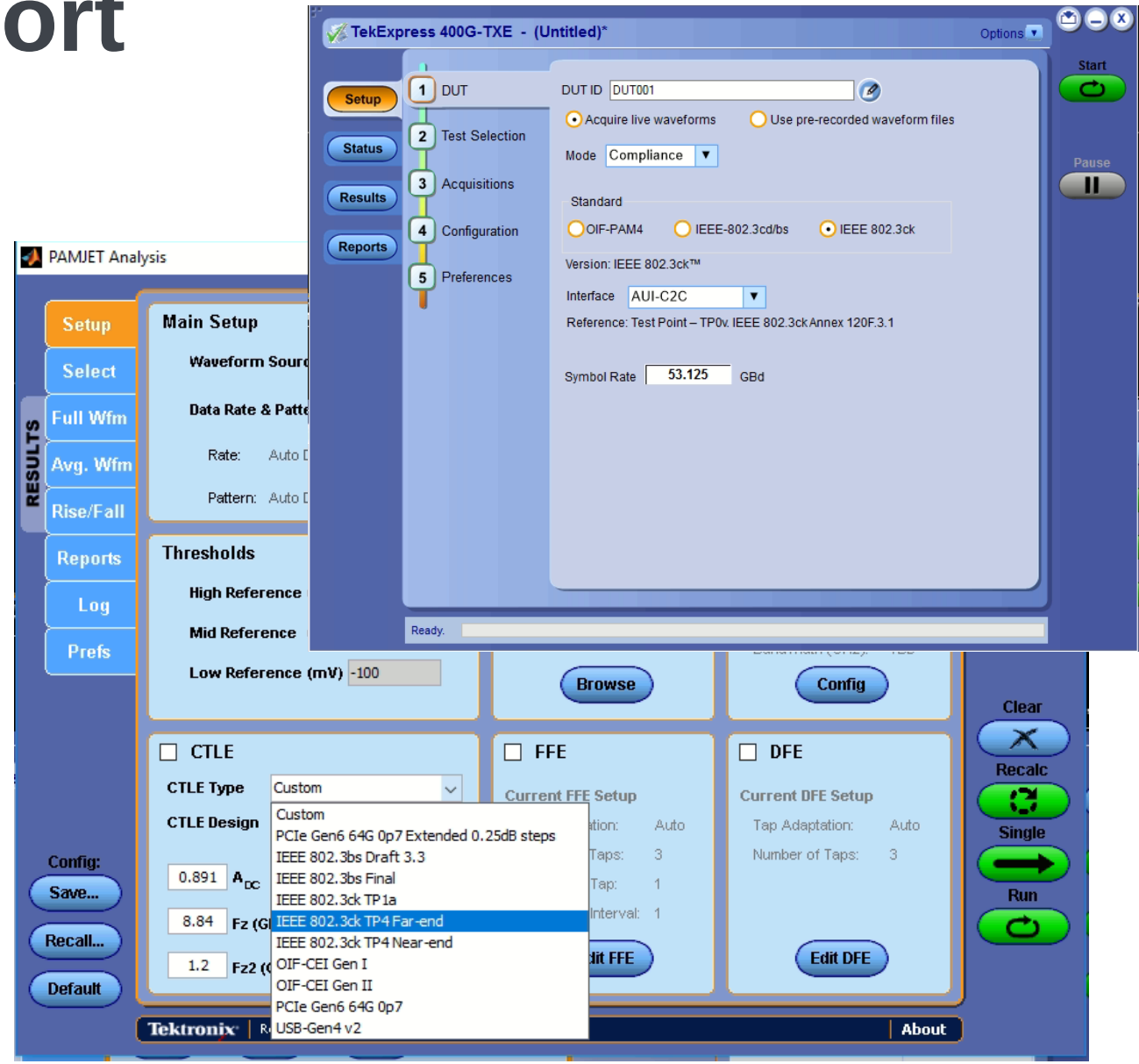
First PCIe 6.0 Rx order from Intel (Folsom)!!

- Fastest time to close calibration ~ ½ day
- Intel has accepted Anritsu/Tektronix calibration

New Technology Support

- PCIe Gen 6 (32GBd PAM4)
- IEEE802.3ck (53GBd PAM4)
- USB Gen4 v2 (80Gbps, PAM3)





Questions