

Octal D Flip-Flop

MC74AC273, MC74ACT273

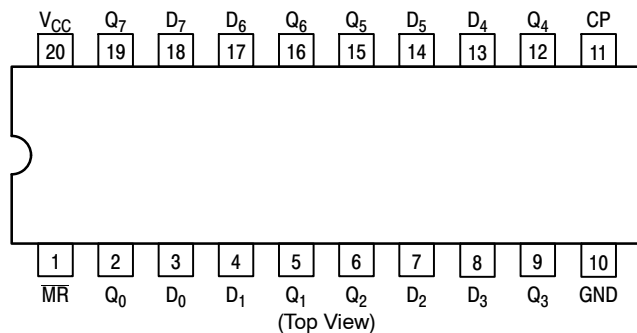
The MC74AC273/74ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- 'ACT273 Has TTL Compatible Inputs
- These are Pb-Free Devices



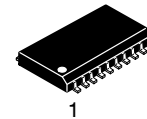
Pinout: 20-Lead Packages Conductors

MODE SELECT-FUNCTION TABLE

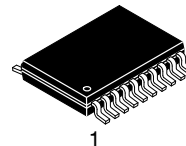
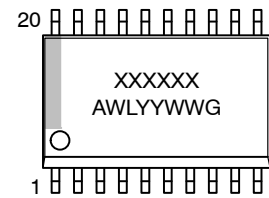
Operating Mode	Inputs			Outputs
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load '1'	H	┐	H	H
Load '0'	H	┐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
┐ = LOW-to-HIGH Clock Transition

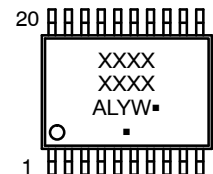
MARKING DIAGRAMS



SOIC-20W
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E

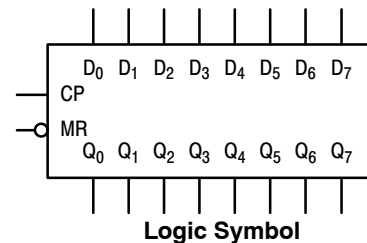


XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT

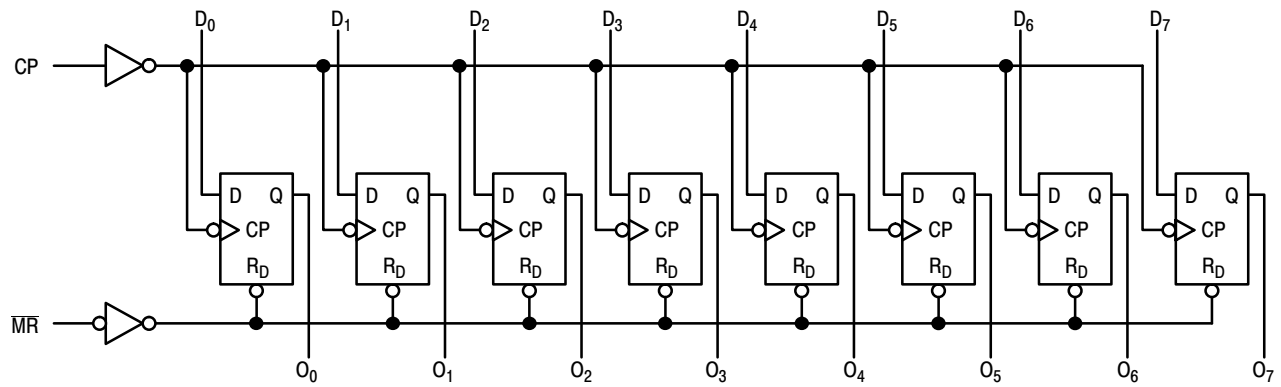
PIN	FUNCTION
D ₀ -D ₇	Data Inputs
$\overline{\text{MR}}$	Master Reset
CP	Clock Pulse Input
Q ₀ -Q ₇	Data Outputs



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74AC273, MC74ACT273



NOTE: That this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1. Logic Diagram

MC74AC273, MC74ACT273

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +6.5	V
V _{IN}	DC Input Voltage (Referenced to GND)	–0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND) (Note 1)	–0.5 to V _{CC} +0.5	V
I _{IK}	DC Input Diode Current	±20	mA
I _{OK}	DC Output Diode Current	±50	mA
I _{OUT}	DC Output Sink/Source Current	±50	mA
I _{CC}	DC Supply Current, per Output Pin	±50	mA
I _{GND}	DC Ground Current, per Output Pin	±100	mA
T _{STG}	Storage Temperature Range	– 65 to + 150	°C
T _L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	140	°C
θ _{JA}	Thermal Resistance (Note 2)	SOIC TSSOP 96 150	°C/W
MSL	Moisture Sensitivity	SOIC TSSOP Level 3 Level 1	
F _R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V–0 @ 0.125 in
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Charged Device Model (Note 4)	> 2000 > 1000
I _{Latchup}	Latchup Performance	Above V _{CC} and Below GND at 85°C (Note 5)	±100

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{OUT} absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD 51–7.
3. Tested to EIA/JESD22–A114–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 6) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	–	150	ns/V
		V _{CC} @ 4.5 V	–	40	
		V _{CC} @ 5.5 V	–	25	
t _r , t _f	Input Rise and Fall Time (Note 7) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	–	10	ns/V
		V _{CC} @ 5.5 V	–	8.0	
T _A	Operating Ambient Temperature Range	–40	25	85	°C
I _{OH}	Output Current – High	–	–	–24	mA
I _{OL}	Output Current – Low	–	–	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
7. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC273, MC74ACT273

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
V _{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I _{OUT} = -50 μA	
		3.0 4.5 5.5	- - -	2.56 3.86 4.86	2.46 3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA	
V _{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I _{OUT} = 50 μA	
		3.0 4.5 5.5	- - -	0.36 0.36 0.36	0.44 0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD} I _{OHD}	†Minimum Dynamic Output Current	5.5 5.5	- -	- -	75 -75	mA	V _{OLD} = 1.65 V Max V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175	- -	75 125	- -	Mhz
t _{PLH}	Propagation Delay Clock to Output	3.3 5.0	4.0 3.0	7.0 5.5	12.5 9.0	3.0 2.5	14.0 10.0	ns
t _{PHL}	Propagation Delay Clock to Output	3.3 5.0	4.0 3.0	7.0 5.0	13.0 10.0	3.5 2.5	14.5 11.0	ns
t _{PHL}	Propagation Delay MR to Output	3.3 5.0	4.0 3.0	7.0 5.0	13.0 10.0	3.5 2.5	14.0 10.5	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V. Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Unit
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW Data to CP	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5		ns
t _h	Hold Time, HIGH or LOW Data to CP	3.3 5.0	−2.0 −1.0	0 1.0	0 1.0		ns
t _w	Clock Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5		ns
t _w	MR Pulse Width HIGH or LOW	3.3 5.0	2.0 1.5	5.5 4.0	6.0 4.5		ns
t _{rec}	Recovery Time MR to CP	3.3 5.0	1.5 1.0	3.5 2.0	4.5 3.0		ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V. Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC273, MC74ACT273

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0		V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8		V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4		V	I _{OUT} = –50 μA
		4.5 5.5	– –	3.86 4.86	3.76 4.76		V	*V _{IN} = V _{IL} or V _{IH} I _{OH} –24 mA –24 mA
		4.5 5.5	– –	0.36 0.36	0.44 0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1		V	I _{OUT} = 50 μA
		4.5 5.5	– –	0.36 0.36	0.44 0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		4.5 5.5	– –	0.36 0.36	0.44 0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	–	1.5		mA	V _I = V _{CC} – 2.1 V
I _{OLD} I _{OHD}	†Minimum Dynamic Output Current	5.5	–	–	75		mA	V _{OLD} = 1.65 V Max V _{OHD} = 3.85 V Min
		5.5	–	–	–75			
I _{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit
			T _A = +25°C C _L = 50 pF			T _A = –40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	5.0	125	200	–	125	–	MHz
t _{PHL}	Propagation Delay Clock to Output	5.0	3.0	6.0	10	2.5	11.0	ns
t _{PLH}	Propagation Delay Clock to Output	5.0	3.0	6.5	11	2.5	12.0	ns
t _{PHL}	Propagation Delay $\overline{\text{MR}}$ to Output	5.0	3.0	7.0	11	2.5	11.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Unit
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW – Data to CP	5.0	3.0	4.5	5.0	ns
t _h	Hold Time, HIGH or LOW – Data to CP	5.0	−2.5	2.0	2.0	ns
t _w	Clock Pulse Width – HIGH or LOW	5.0	2.5	4.0	4.5	ns
t _w	$\overline{\text{MR}}$ Pulse Width – HIGH or LOW	5.0	2.5	4.0	4.5	ns
t _{rec}	Recovery Time – $\overline{\text{MR}}$ to CP	5.0	−1.0	2.0	3.0	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V

MC74AC273, MC74ACT273

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74AC273DWG	AC273	SOIC-20WB	38 Units / Rail
MC74AC273DWR2G	AC273	SOIC-20WB	1000 / Tape & Reel
MC74AC273DTR2G	AC 273	TSSOP-20	2500 / Tape & Reel
MC74ACT273DWG	ACT273	SOIC-20WB	38 Units / Rail
MC74ACT273DWR2G	ACT273	SOIC-20WB	1000 / Tape & Reel
MC74ACT273DTR2G	ACT 273	TSSOP-20	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED
SOLDERING FOOTPRINT*



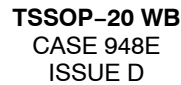
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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SCALE 2:1

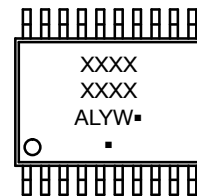


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Technical drawing of a 16-pin connector layout. The drawing shows two rows of 8 pins each, separated by a 7.06 mm gap. The pitch between pins is 0.65 mm. The overall width of the pin array is 16X 0.36 mm. The distance from the center of the pin array to the center of the connector is 1.26 mm. The drawing is labeled "DIMENSIONS: MILLIMETERS".

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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