ANALOG DEVICES

ADRV9008-1/ADRV9008-2/ADRV9009 Profile Configuration Tool User Guide

Profile Configuration Tool User Guide for the
ADRV9008-1, ADRV9008-2, and ADRV9009

INTRODUCTION

This user guide describes the installation and use of the Profile Configuration Tool used with the ADRV9008-1 receiver (Rx), ADRV9008-2 transmitter (Tx) and observation receiver (ORx), and the ADRV9009 transceiver. This type of tool has been referred to as Filter Wizard for previous products since one of its primary functions is the creation of custom finite impulse response (FIR) filter coefficient files.

TABLE OF CONTENTS

REVISION HISTORY

1/2019—Revision A: Preliminary Version

INTRODUCTION

The ADRV9008-1, ADRV9008-2, and ADRV9009 Profile Configuration Tool (hereafter referred to as the "profile tool" or "tool") is used to design the receiver, transmitter, and observation receiver FIR filters for the ADRV9008-x and ADRV9009 wideband integrated transceivers. This tool creates filters which equalize the desired passband while compensating for the signal transfer functions through the entire analog and digital signal paths in the transceiver. The tool also generates ADC profiles and clock rates that can be used with the Transceiver Evaluation Software to evaluate system performance. Any custom configuration of sampling rates and bandwidths must use this tool to create a profile that can be used by in a customer system or with the evaluation kit. The profile tool is available as MATLAB source code, a MATLAB app, and as a stand-alone executable. The tool can be used without hardware connected until the time in which the new profile is transferred to the TES GUI and then loaded into the evaluation system or into the customer code and system.

With this tool, users can perform the following tasks:

- Design new profiles which are a combination of sampling rates and bandwidths which adhere to the transceiver minimum and maximum operating limits while also meeting the requirements the on-chip ARM algorithm processor

- Design programmable FIR filters for these new custom profiles, save the filter coefficients to a file and load them into a customer system or the Transceiver Evaluation System (TES) GUI which then loads them into the transceiver itself

- Use or bypass the AD9528 JESD204B Clock Generator which is included on board the ADRV9008-x and ADRV9009 evaluation boards

- Examine the responses of the filters in each signal path, which consists of the composite analog, composite digital, and aggregate responses

- Perform "what if" experiments by adjusting filter weighting parameters to trade off pass band ripple with stop band rejection

REVISION LIST, CHANGE LOG, AND KNOWN LIMITATIONS

The release notes document has the historical list of changes and limitations of the tool itself. It is available here:
https://www.analog.com/en/design-center/landing-pages/001/transceiver-evaluation-software.html

PROFILE CONFIGURATION TOOL OPTIONS AND DOWNLOADS

The tool is available in three forms, allowing for maximum flexibility. The tool is available as MATLAB source code, a MATLAB App, and as an executable.

EXECUTABLE

The executable includes the exe which allows the tool to run as a separate application without requiring the MATLAB program to be running. The program provides a GUI that allows users to define the input parameters, generate filters, view the output results, and save all output parameters for their own use or use in the ADI EVB GUI software. Note the name of the executable is Talise_Configuration_wizard.exe.

The executable is available here: https://www.analog.com/en/design-center/landing-pages/001/transceiver-evaluation-software.html

For the executable to run as a stand alone application, the MATLAB runtime engine needs to be installed on the PC. The runtime engine is automatically installed when the executable above is installed. For reference, the runtime engine is available to be downloaded separately from this link: https://www.mathworks.com/products/compiler/mcr.html. The runtime engine can take more than a minute to start up the first time it is run, so please be patient while it initializes. The runtime engine version R2015B or later must be used.

MATLAB APP

The app runs as an application within MATLAB. Use of the app requires MATLAB to be running with valid licenses for the Control System Toolbox as well as MATLAB itself. The GUI and flexibility are identical to the executable but running as an app in MATLAB allows the user to write additional code to post-process the data files created by the tool.

More information on installing and running MATLAB apps is found here: http://www.mathworks.com/help/matlab/creating_guis/install-and-run-app.html

The MATLAB App is available here: https://www.analog.com/en/design-center/landing-pages/001/transceiver-evaluation-software.html

MATLAB SOURCE CODE

These are MATLAB functions which users can launch from the MATLAB command window by properly defining the input parameters. Used this way, users have more control of the internal design process.

The MATLAB source code is available here: https://www.analog.com/en/design-center/landing-pages/001/transceiver-evaluation-software.html

USING THE MATLAB APP AND EXECUTABLE

This section elaborates on the first two options, the executable and the App, and addresses both identically since the input and output functionality is the same.

A QUICK START EXAMPLE

The following steps show the process of creating a simple profile, saving it, and loading it into the TES GUI.

- Open the Profile Genereation Tool and select the correct transceiver part number

- Enter the sample rate and bandwidth parameters for all enabled signal paths

- Enable ORx stitching if the ORx bandwidth is greater than 200 MHz

- Adjust the AD9528 VCXO and refclk settings as needed to generate a device clock usable by the transceiver for the entered sampling rates

- Genereate and save the profiles

- Open the TES GUI and connect it to the hardware evaluation system using the desired refclk frequency

- In the TES GUI, under "File" select "Load Custom Profile" and select the file just saved by the configuration tool

- In the TES GUI, adjust the JESD settings and any other GUI parameters as desired, program the evaluation system and then enable the desired signal paths to evaluate the performance

USING THE TOOL GUI TO CREATE A NEW PROFILE

The first screen visible after starting the Tool includes an Instruction screen in the center with the input parameters on the left side and is shown in the picture below:

Please read through the short text on the Instruction tab before using the tool. Note also the links at the bottom, one of which is a path back to this web page and is a link to the ADI Engineer Zone forum. Any questions about the Tool will be addressed in this forum.

The Instructions page is one of several tabs in the GUI. The other tabs are used to display filter responses for each channel type after clicking on "Generate Profiles" as described below.

While the transceiver has separate transmitter, receiver, and observation receiver signal paths, all of the digital filters and data converters in those paths receive their clocks from a common clocking system. Even though the input fields show user configurable sampling rates for each of the different sections, there are rules that must be followed to generate a configuration that the transceiver can use. While some limitations may be obvious such as the maximum sampling rate supported by the transceiver, others are can dependent on additional parameters and are not as intuitive. Some examples of invalid configurations that illustrate the following rules are shown later in this document.

Some less intuitive rules that can come up frequently are listed below. The complete set of rules is listed in the Profile Generation Rules section of this document.

1. The Tx Input Sample Rate must be the same as the ORx Output Sample Rate since internal and external transceiver calibrations require these rates to be the same

2. The ORx Output Sample Rate must be a power of two multiple of the Rx Output Rate to satisfy JESD204B requirements

3. The Tx Total RF BW must be less than 92% or 81% of the Tx sample rate depending on the configuration of the signal paths

4. The ORx RF BW must be less than 92% or 82% of the ORx sample rate depending on the configuration of the signal paths

5. The Rx RF BW must be greater than 40% and less than 82% of the Rx sample rate

Select a Product

There are three different products available in the ADRV900x family that serve different appliations. All of them have one main RF PLL as well as an auxiliary PLL used for calibration functions.

The ADRV9008-1 is a two-receiver-only device, intended for receive-only use cases or for use cases requiring that the receive (Rx) and transmit (Tx) signal paths operate on different RF frequencies such as frequency division duplex (FDD) applications.

The ADRV9008-2 is a two-Tx plus observation receiver (ORx) device intended for use cases in which only a transmitter or a transmitter plus observation receiver is needed. The ORx path is used DPD applications for example, which require monitoring the power amplifier output. In FDD applications, the ADRV9008-2 is paired with the ADRV9008-1 to address both Rx and Tx (plus ORx) signal paths.

The ADRV9009 combines the functionality of the previous two devices, including signal paths for two receivers, two transmitters, and observation receiver. Since there is still only one primary RF PLL, the ADRV9009 is intended for time division duplex (TDD) use cases in which both the receiver and trasnmitter signal paths opereate at the same RF frequency. There are cases in which the ADRV9009 is the target product but the transmit signal path is not used. The tool allows the ADRV9009 to be selected but a checkbox then allows the Tx path to be ignored.

The tool creates profiles for specific devices. If the target device is the ADRV9008-1, then only receive signal path parameters are needed so the tool only generates FIR filter coefficients and other files pertinent to the receive-only device. This also makes the most efficient use of the tool since only those parameters necessary for a particular signal path need to be entered.

The first step when using the tool is to select the proper device from the drop-down menu at the top of the window.

Entering the Transmit Signal Path Parameters

If either the ADRV9008-2 or the ADRV9009 device has been selected, the Tx parameters must be entered into the Tx Profile area unless the checkbox "Disable Tx" is checked. As mentioned above, there are occasions when the ADRV9009 is the target product but the transmit signal path is not needed for a particular application. In that case, check the Disable Tx box.

"Tx Input Sample Rate" is the data rate of the "I" and "Q" samples. This is the data rate output from the baseband processor to the ADRV9008-2 or ADRV9009. These samples are serialized and sent across the JESD204B interface. Once deserialized by the JESD204B processing blocks in the transceiver, the data rate input to the filtering blocks is this same "Tx Input Sample Rate". The rate must be greater than 30.625 MSPS and less than 500 MSPS. Note that the sample rate clock within the transceiver is derived from other clocks and dividers. The rate passed from the tool to the GUI and to the hardware must be exactly what is needed for the application. The JESD204B interface, for example, must use exactly the same serial bit rate on both sides of the link. To reduce the chance that the software could inadvertently adjust a rate without it being obvious to the user, the tool always rounds rates to the nearest kHz. For example, the rate 245.7655 MHz would be rounded to be exactly 245.766 MHz.

"Tx Primary Signal BW (MHz)" is a simpler concept to describe than the "Total BW" entry above it so Primary BW will be covered first. "Primary" BW is the bandwidth used by the desired signal that contains information. It is also referred to as "Large Signal Bandwidth" indicating that the digital signal power provided by the baseband processor can be up to approximately -1 dBFS peak. It is not 0 dBFS peak due to a small amount of digital filter gain at the edges of the primary BW as well as gain due in the Tx QEC compensation filters. The Primary Signal BW must be greater than or equal to 5 MHz and less than or equal to 200 MHz. Adjusting this bandwidth parameter changes analog and digital filters within the transceiver.

As indicated by the data sheet, the Tx signal path can handle a much wider bandwidth than just the primary limit of 200 MHz. The ADRV9008-2 and ADRV9009 devices were designed to address digital predistortion (DPD) applications which require a transmitted signal that is wider than the desired signal. The extra bandwidth, typically 2.5x to 5x wider than the primary BW, is used to linearize a PA that has been pushed into compression. Note that the gain of the digital filters outside of the primary bandwidth can be significant so the maximum signal level must be below that level to avoid clipping. 6-7 dB is required in most cases. In addition, the rejection of images by the digital filters is better in the primary BW. The Profile Configuration Tool will graphically show the digital filter performance. If less image power is needed, one option is to reduce the signal level of the frequencies outside of the primary signal BW. For non-DPD applications, the primary and total BW parameters may be the same value but this value must follow both primary BW and total BW rules. The Total BW must be greater than or equal to 10 MHz and less than or equal to 450 MHz.

The next two parameters, "Pass Band Weight" and "Stop Band Weight", are used to specify how the tool should compromise between pass band ripple and stop band rejection. The weight parameters are used as a ratio in the tool. If the ratio is "1", then equal weighting is given to achieving low passband ripple and high stopband attenuation. The tool will use all FIR taps it has available and maximize the performance of the pass band ripple and stop band rejection equally. When a specific set of input parameters makes it difficult to generate a FIR filter with both expected ripple and attenuation performance, the tool will achieve a compromise, but it may not meet the requirements of the application. For example, it may also be desirable to have better stop band attenuation while allowing a bit more ripple in the pass band. Changing the ratio of weights alters the emphasis the tool places on meeting its objectives. For example, changing the ratio by setting the Stop Band Weight to "100" will sacrifice some passband ripple but improve the stop band attenuation. The resulting digitial filters from the tool depend both on the difficulty the tool has meeting the critera as well as the ratio. A fixed ratio doesn't always result in the same tradeoffs between pass band ripple and stop band attenuation. It is best to start with a ratio of one and then change it after the tool has generated the filters for the first time. The values are real numbers so setting the weights to 1:10 (passband to stopband) is the same as setting them to 0.1:1.

Entering the ORx Signal Path Parameters

The ORx signal path is used in DPD appliations as a receiver of the total transmitted signal after the power amplifier, including the excess bandwidth used to reduce spectral regrowth. For this reason, if the transmit signal path of the ADRV9008-2 or ADRV9009 is used ("Disable Tx" box *not* checked), the "ORx Output Sample Rate (MHz)" *must be the same* as the "Tx Input Sample Rate (MHz)" value. The "ORx RF BW (MHz)" is not required to be the same as the "Tx Total RF BW (MHz)" but for DPD appliations it usually is so that the entire signal is captured. The ORx sample rate has the same range as the Tx sample rate: 30.625 to 500 MSPS. The ORx BW range is 5 MHz to 450 MHz.

For non-DPD applications including those which may have the Tx signal path disabled ("Disable Tx" checked), the ORx sample rate and bandwidth values are more flexible but are still bound by other rules as indicated in the Profile Generation Rules section later in this document and those stated in the paragraph above.

The pass band and stop band weighting values control the tool in the same manner as those used for the Tx Profile and are described in the Tx section here.

The "ORx Stitching" box is worth special mention. If the ORx RF bandwidth is greater than 200 MHz, the ADRV900x devices must use a technique called "stitching" (described in the hardware user guide) which ties together two signal paths to handle the higher sampling rates and wider bandwidths.

The tool *doesn't* automatically check this box when the ORx RF BW exceeds 200 MHz. Checking the box must be done manually. This is because finding optimized settings and filters when stitching two channels together can take several minutes. If the ORx RF BW is 200 MHz or higher and if there is a need to iterate several times to optimize an Rx or Tx profile, leave the box unchecked while iterating and optimizing the Rx or Tx profiles. This allows the tool to generate profiles quickly. Once the Rx and Tx profiles have been optimized, check the stitching box and optimize the ORx profile.

The tool provides text next to the stitching checkbox as a reminder to check the box when necessary and will throw a warning if an ORx profile is saved when the RF BW is greater than 200 MHz but the box is unchecked.

Entering the Rx Signal Path Parameters

For ADRV9008-1 and ADEV9009 devices, the "Rx Output Sample Rate (MHz)" is the data rate output from the transceiver to the baseband processor. These samples are serialized and sent across the JESD204B interface. Once deserialized by the JESD204B processing blocks in the baseband processor, the data rate is this same "Rx Output Sample Rate (MHz)". The valid range is from 25 MSPS to 370 MSPS. As mentioned in the Tx Profile section, the sample rate is rounded to the nearest 1 kHz.

The "Rx RF BW (MHz)" value should be equal to the desired signal bandwidth. Adjusting this parameter changes the analog and digital filters in the transceiver. The valid range is from 10 MHz to 200 MHz.

The pass band and stop band weighting values are used in the same manner as those for the Tx Profile and are described in the Tx section here.

Entering the AD9528 Parameters:

To begin, a short summary describing the functions of the checkboxes and parameter fields is provided below. Then, a more complete description of the operation of the AD9528 on the evaluation system is provided further down.

If "Write AD9528 settings to file" is checked, the output files generated by the tool includes a file with the AD9528 clock distribution settings. The GUI uses these settings when it loads the complete profile. If this box is not checked, the GUI assumes that the settings were not changed from the default values of a 30.72 MHz reference clock and 122.88 MHz VCXO.

"Bypass PLL1" allows an external frequency to be injected directly into the AD9528. This is useful when the required device clock can't be accommodated by the available VCXOs. Note that the externally injected frequency must be low phase noise, similar to the VCXO itself, to achive proper operation and performance.

The "AD9528 VCXO Freq (MHz)" field is the on-chip VCXO or externally provided frequency. Change this only if the VCXO is changed to another frequency or if the frequency is provided externally. If the frequency is provided externally, also check the "Bypass PLL1" box.

The "AD9528 RefClk A Freq (MHz)" field is the network reference frequency that also can synchronize the evaluation system to a master test equipment clock. This is a submultiple of the VCXO frequency. Change this only if this externally-provided frequency is different from the 30.72 MHz default.

The following information provided more detail on the AD9528 settings.

The evaluation system includes the AD9528 clock distribution chip. It requires a separate voltage-controlled crystal oscillator (VCXO) and it requires a reference clock. The VCXO is included with the evaluation system and by default is 122.88 MHz. The reference clock must be provided by the customer from an external clock source to SMA J401 on the evaluation board. It is assumed to be 30.72 MHz by default.

The reference clock (refclk A) does not have to be an extremely low phase noise source since the PLL on the AD9528 filters out much of the noise. In a customer system, this would normally be a master clock used to synchronize the entire network. The VCXO, however, must be very low phase noise since it's noise is not filtered like the refclk A is filtered.

The AD9528 does not use fractional-N PLLs but it does multiply frequencies up to a high rate and then divide them back down again to achieve the desired clock rates so it is possible to generate output frequencies that are not integer-related to the VCXO or the refclkA. For example, an output of 153.6 MHz from the AD9528 to the device clock transceiver input can be generated using the stock 122.88 MHz.

The transceiver also multiplies the device clock frequency up to a high rate and then divides it back down to generate the internal clock rates so as an example, the transceiver can similarly take a device clock frequency of 122.88 MHz and generate the internal clocks needed for a 153.6 MHz-based profile.

The on-board VCXO should be changed to another frequency if 122.88 MHz will not allow the configuration of the proper clock frequencies for the desired profile. In many cases, the customer system will provide a particular VCXO frequency to the AD9528 and it may be desirable to change the VCXO to match the final customer system frequency to remove that variable between the evaluation system and the customer system.

There are two methods for changing this VCXO frequency as described in the evaluation system user guide. One method is to change the VCXO to another frequency. Another is to bypass PLL1 of the VCXO and inject an external frequency directly into the AD9528 which allows for frequencies not supported by the available VCXOs.

To test whether the default freuqencies will work for a given profile, provide the parameters needed to define a profile. Press "Generate Profiles". Check the box "Write AD9528 settings to file" which checks that the specified "AD9528 VCXO Freq (MHz)" value. If not, an error message is thrown and the VCXO frequency will need to be changed.

If the VCXO frequency is changed from its default value of 122.88 MHz, the "AD9528 RefClk A Freq (MHz)" will most likely need to be changed as well to be an integer submultiple of the VCO frequency.

Generate Profiles

Press the "Generate Profiles" button to have the tool create a set of profiles and digital filter coefficients for the desired configuration

Selecting the device clock

After generating a profile, check the "Write AD9528 settings to file" checkbox in the AD9528 section to verify that the device clock can be generated by the selected VCXO frequency. If a warning message indicates that it is not possible, close the warning message and change the VCXO and RefClk A frequencies to values that support the desired device clock and sampling rates.

If a warning does not result, then determine which device clock frequency is desired. Clicking the down arrow to the right of the "Device Clock (MHz)" field shows the available frequencies at a particular "Ref Clk divider" setting. The incoming device clock is divided down by the Ref Clk divider and then provided to the various transceiver PLLs as detailed in the transceiver user guide.

Be sure to try various divider settigns to see if a desired device clock frequency is present with a particular divider.

If the Generate Profiles button is pressed again, the divider and the device clock fields reset to a defalt of a divider of one and the maximum device clock at that divider setting.

Saving Output Files

After the tool generates a profile, the files can be imported into customer system software or the TES GUI. The tool generates several files at the location and with a filemame specified by the user. One file contains all of the paramers needed by the GUI to specify a profile as well a the FIR filter coefficients for all necessary signal paths and the ADC coefficients for the Rx and ORx signal paths.

Up to three additional files appended with a signal path name and "stf" are also generated depending on the signal paths enabled. These are signal transfer function files used by the GUI to plot the frequency responses.

If the AD9528 parameters are also written to a file, an additional file will appear

USING A NEW PROFILE

Importing a new profile into the GUI is done by merely connecting the GUI to an evaluation system that has booted up, selecting "File" in the GUI menu bar, selecting "Load Custom Profile", and browsing to the file name saved by the tool. The other "stf" and clock files if present will automatically be loaded by the GUI as needed.

Be sure to adjust the AD9528 settings by navigating to the AD9528 tab in the GUI if the VCXO and/or refclk frequencies have changed.

How to Apply the Tool output to a Customer System

To use the new profile in a customer system new initialization files need to be generated. With the new profile loaded into the GUI as above, go to the TOOLS menu, Create Script > then select the desired format. A typical customer system will use the *Init .c Files* option, which generates all the files in C needed for configuring the device in the current setup state of the GUI. The talise_config.c file contains all the new settings of the custom profile but note all files generated with this profile including a new stream file (TaliseStream.bin) are stored in the selected folder and should all be utilized in the customer system to be sure there are no conflicts with files generated from prior profile settings.

ADVANCED SETTINGS

Almost all applications can be handled by adjusting the parameters already discussed but some use cases demand additional parameter specifications. Checking the "Advanced settings" checkbox opens a new window allowing these additional parmeters to be adjusted.

Tx Advanced Settings

There are two independent anti-imaging analog filters after the DAC. The tool normally optimizes the analog filters based on the "Tx Total RF BW (MHz)" setting such that the best compromise of image rejection and FIR filter gain at the band edges is achieved. In some cases, however, there is a desire to change the balance between rejection and filter gain and this can be accomplished by adjusting one or both of the filter corners in the advanced settings window. The "Tx Baseband filter" is a 2nd order filter while the "Real pole" is by definition a 1st order filter. The DAC feeds the baseband filter which in turn feeds the real pole.

Rx Advanced Settings

The receive signal path also has an analog filer, the Trans-impedance amplifier or TIA. The advanced settings window allows this corner to be adjusted independently from the "Rx RF BW (MHz)" setting.

This function is not currently supported: The tool normally chooses an Rx FIR decimation factor that best suits the available clock rates and the sampling rate. If a particular decimation rate is desired, it can be forced by setting this field to 1, 2, or 4.

There are several options for the decimating filters closest to the ADC. The tool normally selects the best optiosn for the available clock rates, desired sampling rate, and best ADC and filtering performance. Occasionally, however, sampling rate-based spurs can be present which requires additional frequency planning. Checking the "Force" box allows the "Decimation mode" setting to be fixed to the best value in these cases.

"Real IF mode Enable" configures the tool and the transceiver for the mode in which only the "I" signal path carries data which aligns with the interface protocols of some baseband processors. The transceiver use guide has more information on this mode of operation.

The transceiver provides several dual band modes that split a single received spectrum into two halves so that two different bands can be handled separately by two different digitial signal paths. Each signal path has independent numerically controlled oscillators and filters allowing each band to be handled independently. The transceiver user guide has much more information on this mode of operation. The advanced settings window allows access to all of these parameters if dual band operation is desired.

Saving Advanced Settings

Confirm or Discard the settings as desired, both of which will close the window. If all other standard parameters have been entered, new profiles may be generated by pressing the "Generate Profiles" button.

MANIPULATING THE INTERACTIVE PLOTS

Plot Information

The tool generates frequency response plots for all enabled signal paths, including the loopback path, after a profile has been generated.

Each plot has the same valuable markers, response curves, and information to quickly show the resulting performance:

- The Composite Analog Response plot is the total response of all analog filters in the signal path
- The Composite Digital Response plot shows the total response of all digital filters, including the programmable FIR filter, in the signal path
- The Composite Final Response is the overall magnitude response of the entire signal path
- Passband ripple is indicated both by limit lines across the passband frequency range as well as a specific value shown as text on the plot
- Stopband riplle is shown by limit lines and text on the plot for different Nyquist bands

The Zoom Feature

To view a certain area of a plot in more detail, holding the left mouse button down while drawing across the desired area will create a rectangular outline. Releasing the mouse button will cause the plot to zoom in on just the area within the rectangle.

Further magnification can be achieved by repeating the process.

Pointing the mouse at a particular location on the plot and pressing the left mouse button results in a quick 2x zoom.

To return to a previous zoom level, right click the mouse on the plot and select either "Zoom Out" which returns to the magnification level before the last zoom or "Return to Original View" which shows the original plot before zooming.

By default, the zoom function affects both axes. To limit the action to either the horizontal or veritical axis, right click the mouse, select "Zoom Options" and then select the desired zoom style.

EXAMPLES

USING PASS BAND AND STOP BAND WEIGHTS TO OPTIMIZE PERFORMANCE

The typical ratios found in fourth generation (4G) communciations systems have relatively large ratios of sampling rates to bandwidths. Larger ratios such as 1.2288 allow the on-chip FIR filters to optimize both the pass band ripple and the stop band rejection with excellent results. Some applications, however, require the bandwidth to be very close to the sampling rate and in these cases, the on-chip FIR filters may not have enough taps to achieve results needed without some additional optimization.

As an example, assume that the following parameters are needed for a Tx/ORx (ADRV9008-2) system.

- Input Parameters to the Tool
    - o Tx Input Sample Rate = 245.76 MSPS
    - o Tx Total RF BW = 226 MHz
    - o Tx Primary Signal BW = 100 MHz
    - o Orx Output Sample Rate = 245.76 MSPS
    - o Orx RF BW = 226 MHz
- Output Requirements Parameters
    - o Tx Ripple < 0.25 dB
    - o Tx Stopband rejection > 45 dB
    - o Orx Ripple < 0.5 dB
    - o Orx Stopband rejection > 45 dB

Setting up the profile and generating the profile with the default weight ratios of 1:1 for both Tx and Orx results in Tx ripple equal to 0.11 dB and stopband rejection of -46.8 dB at 132.7 MHz and improves dramatically at higher frequencies offset from the LO.
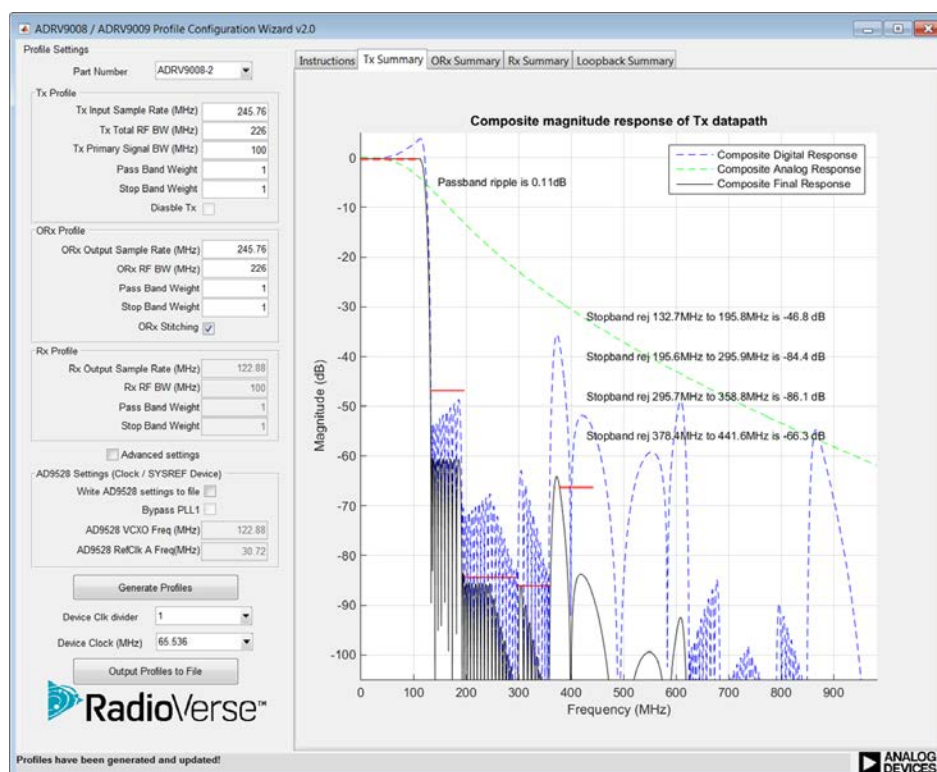
The Orx signal path struggles more and achives a passband ripple of 0.21 dB and a stopband rejection of -37.4 dB at 132.7 MHz. Clearly more weight is needed for the stopband rejection.
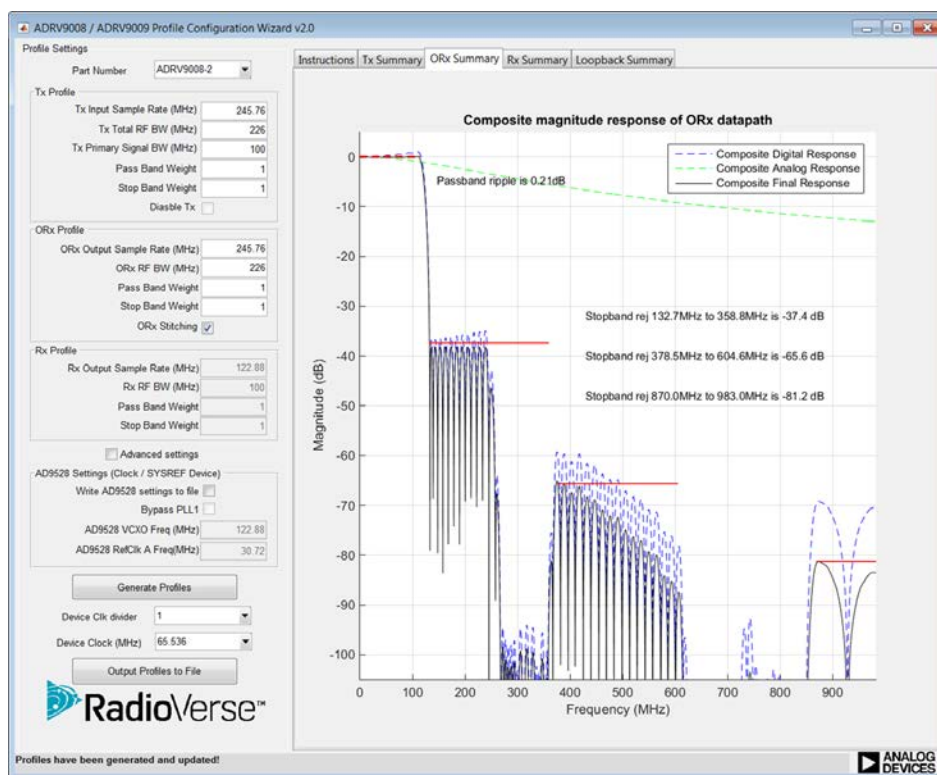
Increasing the Stop Band Weight to 10 results in stopband rejection that achieves the goal but the ripple is unacceptably high. Changing the weight to 6 meets both passband ripple and stopband rejection goals.
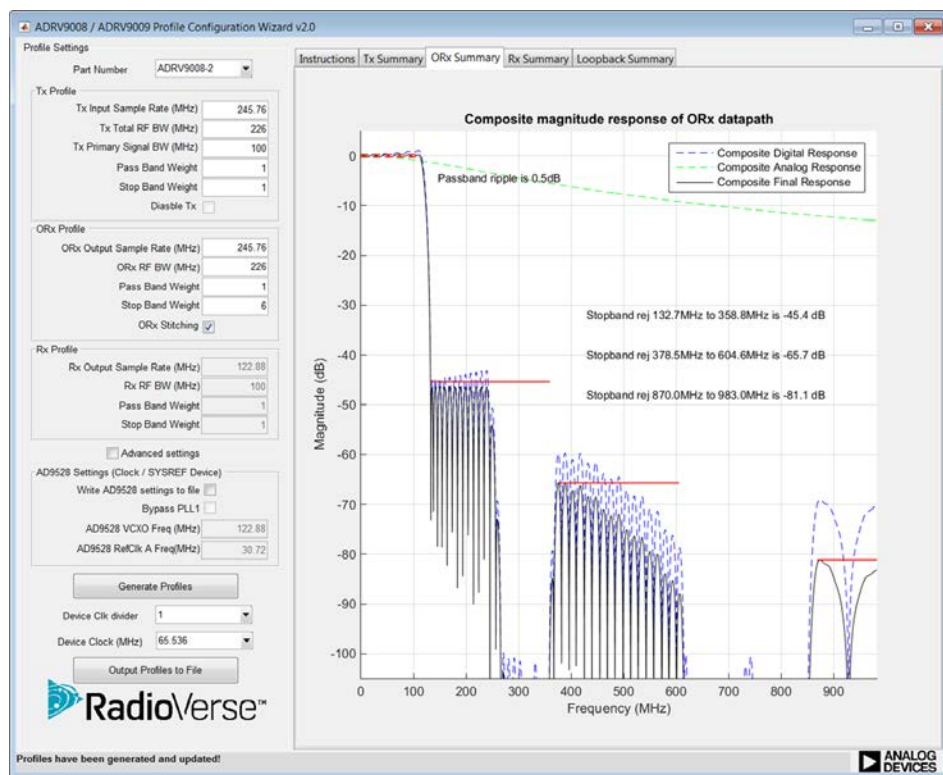
ADJUSTING THE AD9528 SETTINGS TO ENABLE A CUSTOM PROFILE

In this example, a custom profile is created which requires changes to be made to the AD9528 settings to achieve the clock rates needed for the new profile.

Assume the following for an ADRV9009-based application:

- Tx Sample Rate = Orx Sample Rate = Rx Sample Rate = 100 MSPS
- Tx Total BW = Orx RF BW = Tx Primary BW = Rx RF BW = 50 MHz

With the parameters entered, a profile is generated but as indicated in the AD9528 section, checking the "Write AD9528 settings to file" checkbox reveals whether the default VCXO can be used with the custom profile. In this case, an error is returned that no possible device clocks can be generated with the 122.88 MHz rate. Either the VCXO must be changed or PLL1 must be bypassed.
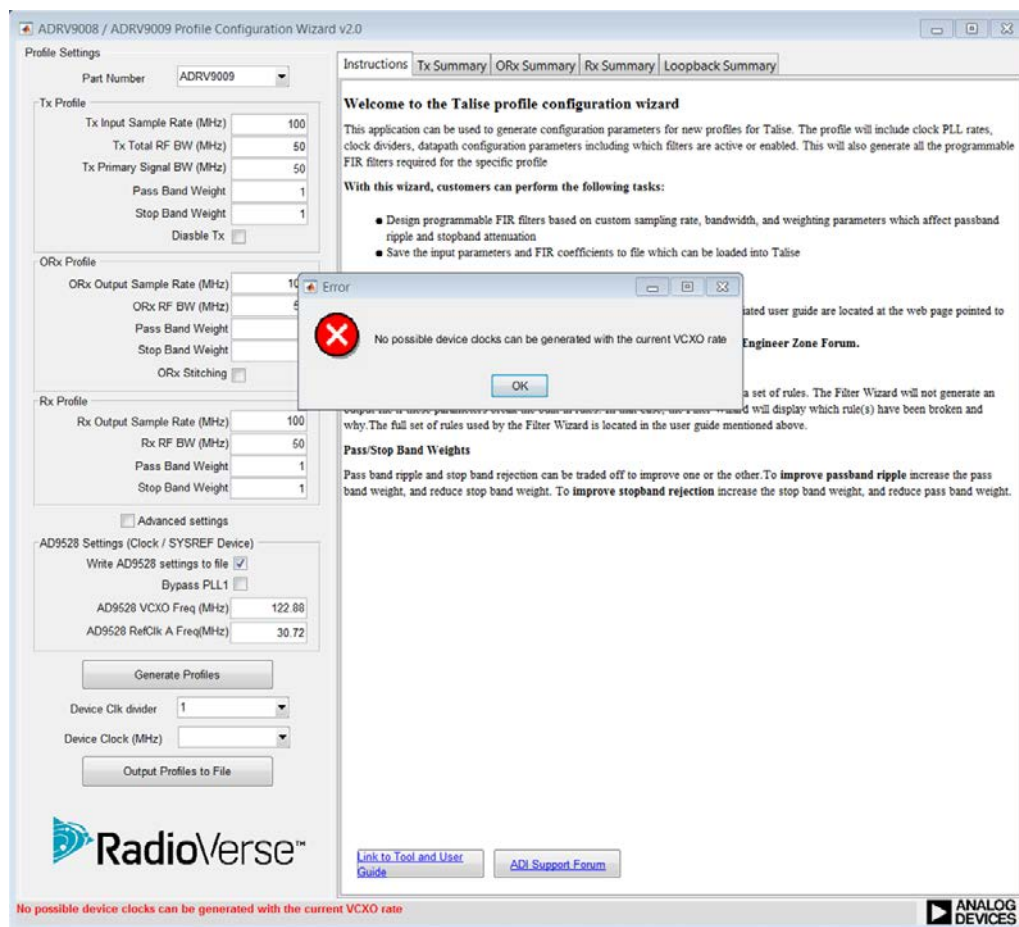
In this example, the VCXO itself is changed on the evaluation system to 50 MHz. Changing the value in the tool causes a new error to pop up indicating that the AD9528 reference clock of 30.72 MHz won't work with the 50 MHz VCXO.

The reference clock is then changed to 25 MHz. This causes the options for the Device Clock and Device Clock Divider to change to valid options that meet the VCXO, reference clock, sampling rate, and all internal clock rates for the system.
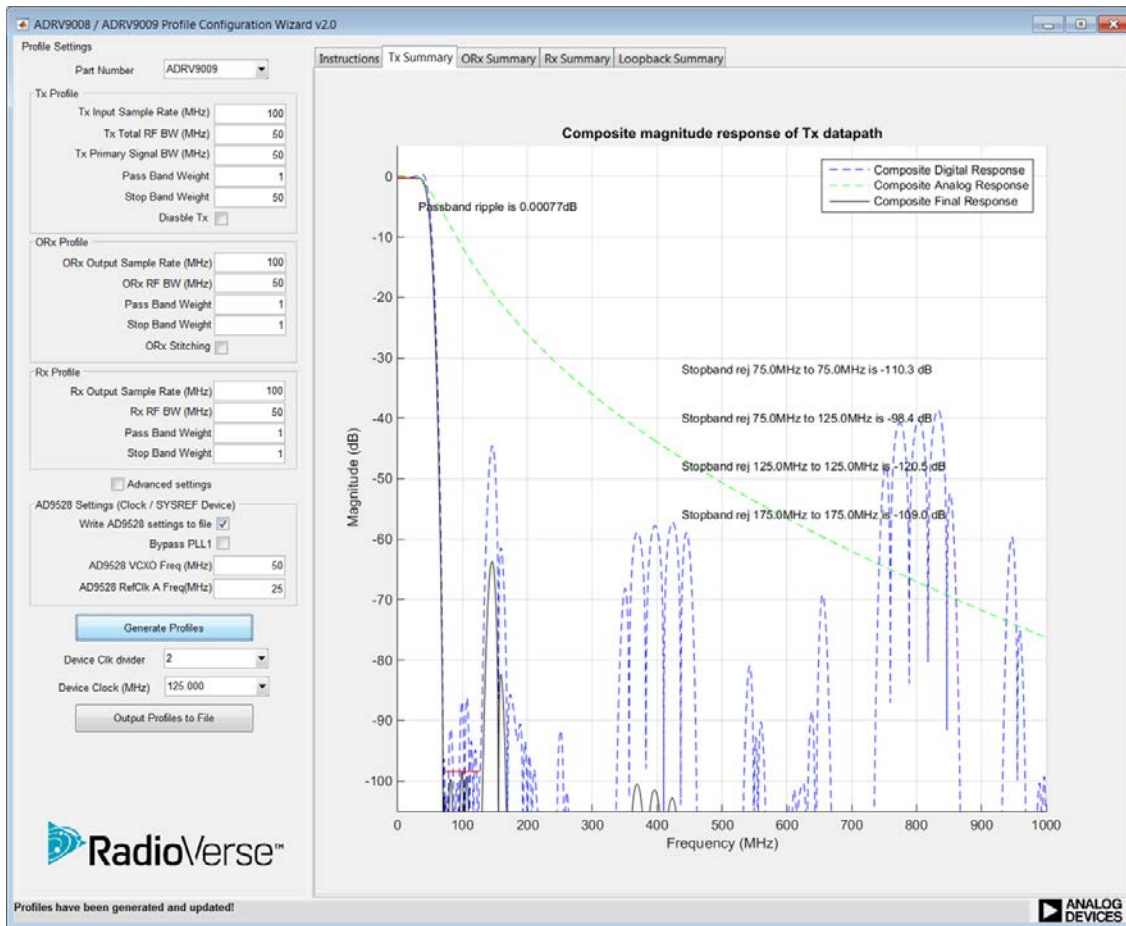
PROFILE GENERATION RULES

The following tables list all of the rules that the tool uses to evaluate whether a custom profile can be created. It is helpful to review these rules occasionally to reduce the number of iterations needed when creating a new profile.

CONSTRAINTS FOR THE TX SIGNAL PATH

Parameter	Constraint
Tx Input Sample Rate (MHz)	30.625
Minimum	30.625
Maximum	500
Relationship to ORx Sample Rate	Must equal the ORx Output Sample Rate (MHz)
Tx Total RF BW (MHz) (Absolute Limits)	
Minimum	10
Maximum	450
Tx Total RF BW (MHz) [INT1,2,4, and 8 modes]*	≤ 0.92*Tx input Sample Rate (MHz)
Tx Total RF BW (MHz) [INT5 mode]*	≤ 0.81*Tx input Sample Rate (MHz)
Tx Primary Signal BW (MHz) (Absolute Limits)	
Minimum	5
Maximum	200
Tx Primary Signal BW (MHz) [INT1,2,4, and 8 modes]*	≤ 0.41*Tx input Sample Rate (MHz)
Tx Primary Signal BW (MHz) [DEC5 mode]*	≤ 0.55*Tx input Sample Rate (MHz)
DAC Clock Rate (MHz)	
Minimum	980
Maximum	2000
Total Signal Path Interpolation	
Minimum	2
Maximum	32
Maximum Programmable FIR Input Rate (MSPS)	500
Maximum Programmable FIR Output Rate (MSPS)	500
Tx Programmable FIR Sample Processing Clock (DP_CLK)	(N * Tx Input Sample Rate) where N = 1, 2, 4 or 8 AND (N x Tx Input Sample Rate) ≤ 500 MHz
Tx Programmable FIR Taps	((20*DP_CLK)/Tx Input Sample Rate (MHz)) with possible values of 20, 40, 60 or 80

*The transmit signal path final (closest to DAC) half-band filter stages can be set up to interpolate by x1, x2, x4, x8, and x5. The Rx or ORx signal paths have decimate by 4 or 5 options for the first (closest to ADC) filter stages. When the Rx or ORx signal paths use the x5 decimation option, the Tx (if used) must use the interpolate-by-5 (INT5) stage. This filter stage introduces a tighter restriction on the bandwidth-to-sampling rate ratio.

CONSTRAINTS FOR THE ORX SIGNAL PATH

Parameter	Constraint
ORx Output Sample Rate (MHz)	
Minimum	30.625
Maximum	500
Relationship to Tx Sample Rate	Must equal the Tx Input Sample Rate (MHz)
Relationship to Rx Sample Rate	Must be a power-of-two multiple of Rx Output Sample Rate (MHz)
ORx RF BW (MHz) (Absolute Limits)	
Minimum	5
Maximum	450
Orx RF BW (MHz) [DEC4 mode]**	
Minimum	≥ 0.4*Orx Output Sample Rate (MHz)

Maximum	≤ 0.92*Orx Output Sample Rate (MHz)
Orx RF BW (MHz) [DEC5 mode]**	
Minimum	≥ 0.4*Orx Output Sample Rate (MHz)
Maximum	≤ 0.82*Orx Output Sample Rate (MHz)
Orx TIA BW (MHz) (Advanced Settings)	
Minimum	100
Maximum	225
ADC Clock Rate (MHz)	
Minimum	980
Maximum	2000
Relationship to Rx ADC Rate	Must equal Rx ADC Clock Rate for ADRV9009
Maximum Programmable FIR Input Rate (From HB1) (MSPS)	500
Maximum Half-Band 1 (HB1) Input Rate (MSPS)	500
Total Signal Path Interpolation	
Minimum	4
Maximum (DEC4 Mode)**	32
Maximum (DEC5 Mode)**	20
Orx Programmable FIR Decimation	1, 2, 4
Orx Programmable FIR Sample Processing Clock (DP_CLK)	(N * Orx Output Sample Rate) where N = 1, 2, 4 or 8 AND (N x Orx Output Sample Rate) ≤ 500 MHz
Orx Programmable FIR Taps	((24*DP_CLK)/Orx Output Sample Rate (MHz)) with possible values of 24, 48 and 72

**The first (closest to ADC) half-band stages in the Orx signal path can be configured to decimate by 4 or by 5 as shown in the hardware user guide. The two options have different RF BW and total decimation limits.

CONSTRAINTS FOR THE RX SIGNAL PATH

Parameter	Constraint
Rx Output Sample Rate (MSPS)	
Minimum	25
Maximum	370
Relationship to ORx Sample Rate	ORx Output Sample Rate (MHz) must be a power-of-two multiple of the Rx Output Sample Rate (MHz)
RX RF BW (MHz) (Absolute Limits)	
Minimum	5
Maximum	200
RX RF BW (MHz) (Complex Mode)	
Minimum	≥ 0.4*ORx Output Sample Rate (MHz)
Maximum	≤ 0.82*ORx Output Sample Rate (MHz)
RX RF BW (MHz) (Real IF Mode)	
Maximum	≤ 0.41*ORx Output Sample Rate (MHz)
Signal Position in Rx Spectrum	Final output spectrum must have entire BW on one side of LO (DC)
ORx TIA BW (MHz) (Advanced Settings)	
Minimum	40
Maximum	225
ADC Clock Rate (MHz)	
Minimum	980
Maximum	2000
Relationship to ORx ADC Rate	Must equal ORx ADC Clock Rate for ADRV9009

Maximum Programmable FIR Input Rate (From HB1) (MSPS)	500
Maximum Half-Band 1 (HB1) Input Rate (MSPS)	500
Total Signal Path Decimation (Not Including Dual Band Digital Downconverter (DDC) DC Half-Band)	
Minimum	4
Maximum	40
Rx Programmable FIR Decimation	1, 2, 4
Rx Programmable FIR Sample Processing Clock (DP_CLK)	(N * Rx Output Sample Rate) where N = 1, 2, 4 or 8 AND (N x Rx Output Sample Rate) ≤ 500 MHz
Rx Programmable FIR Taps	((24*DP_CLK)/Rx Output Sample Rate (MHz)) with possible values of 24, 48 and 72
DDC Mode	
Maximum Output Rate with Filter Enabled (MSPS)	370
Maximum BW (of One Band)	≤ 0.4*DDC Half-Band Input Rate
Maximum BW (of Other Band)	BW of the other band should be > (checking w/Aakash on greater than vs. less than) 0.6*DDC Half-Band Input Rate

CONSTRAINTS FOR THE LOOPBACK RX SIGNAL PATH

The transceiver uses a loopback path internally to enable some calibrations. While the loopback path parameters are automatically configured by the tool and are not accessible by the user, occasionally a custom profile will not break the rules of the Tx, ORx, or Rx signal paths but the loopback path rules are broken. The table below will help explain the cause when an error message indicates that a loopback parameter has been exceeded.

Parameter	Constraint
Loopback (LPBK) Rate at Programmable FIR output (MSPS)	
Minimum	20
Maximum	500
Relationship to ORx Signal Path	Must be same as ORx Output Sample Rate (MHz)
LPBK RF Signal BW (MHz)	
Minimum	5
Maximum	200
Relationship to Tx Signal Path	Must be same as Tx Input Sample Rate (MHz)
LPBK TIA BW (MHz)	225
LPBK ADC Clock Rate	
Minimum	980
Maximum	2000
Relationship to ORx Signal Path	Must be same as ORx ADC Rate
LPBK Programmable FIR Maximum Input Rate (MHz)	500
LPBK Half-Band 1 Maximum Input Rate (MHz)	500
LPBK Total Signal Path Decimation	
Minimum	4
Maximum (DEC4 Mode)*	32
Maximum (DEC5 Mode)*	20
LPBK Programmable FIR Decimation	1, 2, 4; same as on ORx
Available Options	1, 2, or 4
Relationship to ORx Signal Path	Must be same as ORx programmable FIR decimation
LPBK Programmable FIR Sample Processing Clock (DP_CLK)	(N * LPBK Output Sample Rate) where N = 1, 2, 4 or 8 AND (N x LPBK Output Sample Rate) ≤ 500 MHz
LPBK Programmable FIR Taps	

Options	((24*DP_CLK)/Rx Output Sample Rate (MHz)) with possible values of 24, 48 and 72
Relationship to ORx Signal Path	Must be same number of taps as ORx programmable FIR

***The first (closest to ADC) half-band stages in the LPBK signal path can be configured to decimate by 4 or by 5 as shown in the hardware user guide. The two options have different RF BW and total decimation limits.

ANALOG DEVICES

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