Deadman Timer (DMT)

HIGHLIGHTS

This section of the manual contains the following major topics:

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Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices.

Please consult the note at the beginning of the "**Deadman Timer (DMT)**" chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Website at: http://www.microchip.com.

1.0 INTRODUCTION

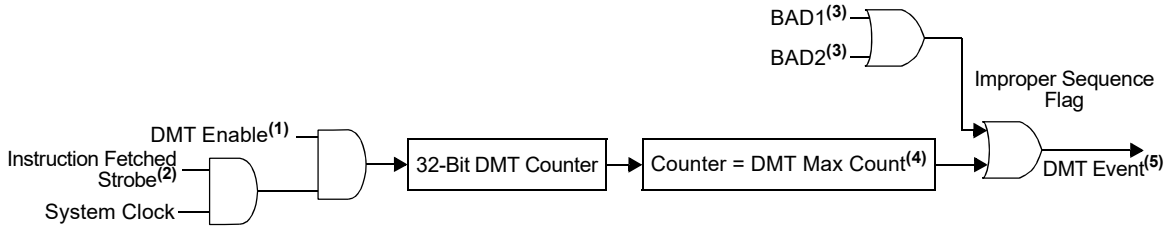
The Deadman Timer (DMT) module is designed to enable users to monitor the health of their application software by requiring periodic timer interrupts within a user-specified timing window. The DMT module is a synchronous counter and when enabled, counts instruction fetches, and is able to cause a soft trap/interrupt. Refer to the **"Interrupt Controller"** chapter in the current device data sheet to check whether the DMT event is a soft trap or interrupt if the DMT counter is not cleared within a set number of instructions. The DMT is typically connected to the system clock that drives the processor (TCY). The user specifies the timer time-out value and a mask value that specifies the range of the window, which is the range of counts that is not considered for the comparison event.

Some of the key features of this module are:

- Configuration or software enable controlled
- User-configurable time-out period or instruction count
- Two instruction sequences to clear timer
- 32-bit configurable window to clear timer

Figure 1-1 shows a block diagram of the Deadman Timer module.

Figure 1-1: Deadman Timer Module Block Diagram



Note 1: The DMT can be enabled either in the Configuration register, FDMT, or in the Special Function Register (SFR), DMTCON.

2: The DMT is clocked whenever the instructions are fetched by the processor using a system clock. For example, after executing a GOTO instruction (which uses four instruction cycles), the DMT counter will be incremented only once.

3: BAD1 and BAD2 are the improper sequence flags. For more information, refer to **Section 3.5 "Resetting the DMT"**.

4: The DMT Max Count is controlled by the initial value of the FDMTCNL and FDMTCNH registers.

5: A DMT event is a non-maskable soft trap or interrupt.

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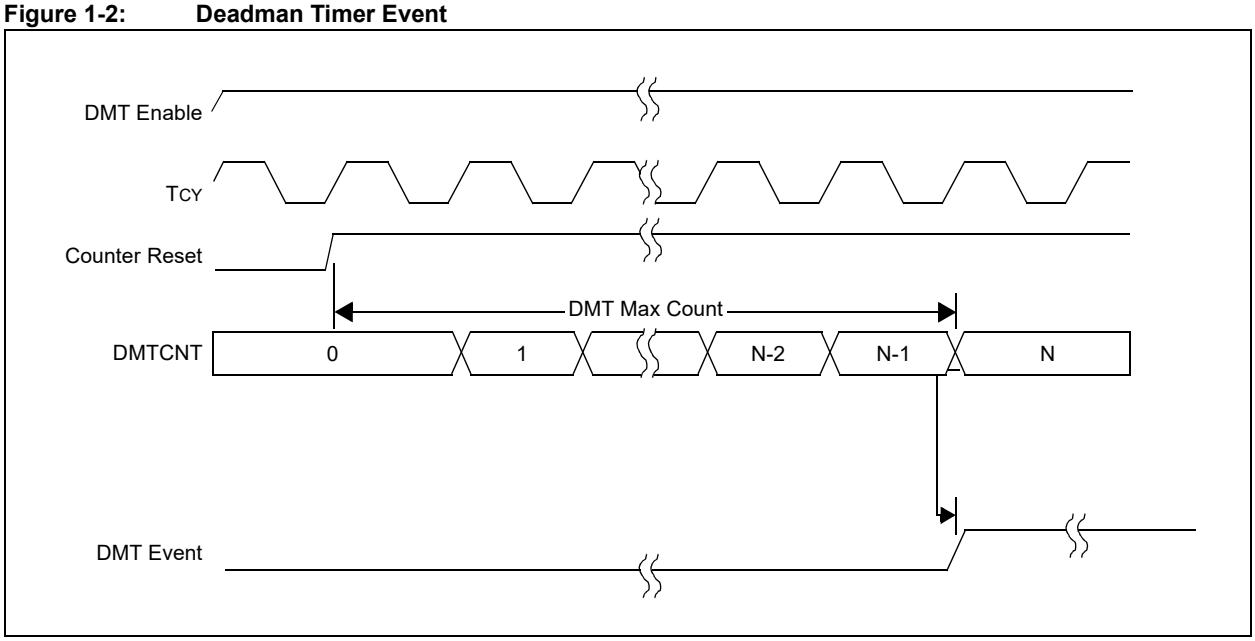
Figure 1-2 shows the timing diagram of a Deadman Timer event.

Figure 1-2: Deadman Timer Event



2.0 DMT REGISTERS

Note: Each dsPIC33/PIC24 family device variant may have one or more DMT modules. Refer to the specific device data sheets for more details.

The DMT module consists of the following Special Function Registers (SFRs):

- **DMTCON: Deadman Timer Control Register**

This register is used to enable or disable the Deadman Timer.

- **DMTPRECLR: Deadman Timer Preclear Register**

This register is used to write a preclear keyword to eventually clear the Deadman Timer.

- **DMTCLR: Deadman Timer Clear Register**

This register is used to write a clear keyword after a preclear word has been written to the DMTPRECLR register. The Deadman Timer will be cleared following a clear keyword write.

- **DMTSTAT: Deadman Timer Status Register**

This register provides status for incorrect keyword values or sequences, or Deadman Timer events and whether or not the DMT clear window is open.

- **DMTCNTL: Deadman Timer Count Register Low** and **DMTCNTH: Deadman Timer Count Register High**

These lower and higher count registers, together as a 32-bit counter register, allow user software to read the contents of the DMT counter.

- **DMTPSCNTL: Post Status Configure DMT Count Status Register Low** and **DMTPSCNTH: Post Status Configure DMT Count Status Register High**

These lower and higher registers provide the value of the DMTCNTx Configuration bits in the FDMTCNTL and FDMTCNTH registers, respectively.

- **DMTPSINTVL: Post Status Configure DMT Interval Status Register Low** and **DMTPSINTVH: Post Status Configure DMT Interval Status Register High**

These lower and higher registers provide the value of the DMTIVTx Configuration bits in the FDMTIVTL and FDMTIVTH registers, respectively.

- **DMTHOLDREG: DMT Hold Register**

This register holds the last read value of the DMTCNTH register when the DMTCNTH and DMTCNTL registers are read.

Table 2-1: Fuse Configuration Registers that Affect Deadman Timer Module

Register Name	Description
FDMT	Setting the DMTEN bit in this register enables the DMT module and if this bit is clear, DMT can be enabled in software through the DMTCON register.
FDMTCNTL and FDMTCNTH	Lower (DMTCNT[15:0]) and upper (DMTCNT[31:16]) 16 bits configure the 32-bit DMT instruction count time-out value. The value written to these registers is the total number of instructions that are required for a DMT event.
FDMTIVTL and FDMTIVTH	Lower (DMTIVT[15:0]) and upper (DMTIVT[31:16]) 16 bits configure the 32-bit DMT window interval. The value written to these registers is the minimum number of instructions that are required to clear the DMT.

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2.1 Register Map

A summary of the registers associated with the Deadman Timer (DMT) module is provided in Table 2-2.

Table 2-2: DMT Register Map

SFR Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DMTCON	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DMTPRECLR	STEP1[7:0]								—	—	—	—	—	—	—	—
DMTCLR	—	—	—	—	—	—	—	—	STEP2[7:0]							
DMTSTAT	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN
DMTCNTL	COUNTER[15:0]															
DMTCNTH	COUNTER[31:16]															
DMTHOLDREG	UPRCNT[15:0]															
DMTPSCNTL	PSCNT[15:0]															
DMTPSCNTH	PSCNT[31:16]															
DMTPSINTVL	PSINTV[15:0]															
DMTPSINTVH	PSINTV[31:16]															

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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2.2 DMT Control Register

Register 2-1: DMTCON: Deadman Timer Control Register

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ON(1,2)	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** Deadman Timer Module Enable bit(1,2)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is not enabled

bit 14-0 **Unimplemented:** Read as '0'

Note 1: This bit has control only when DMTEN = 0 in the FDMT register.
2: DMT cannot be disabled in software. Writing '0' to this bit has no effect.

Register 2-2: DMTPRECLR: Deadman Timer Preclear Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP1[7:0](1)							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **STEP1[7:0]:** DMT Preclear Enable bits(1)
01000000 = Enables the Deadman Timer preclear (Step 1)
All Other Write Patterns = Sets the BAD1 flag.

bit 7-0 **Unimplemented:** Read as '0'

Note 1: Bits[15:8] are cleared when the DMT counter is reset by writing a correct sequence of STEP1 and STEP2.

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Register 2-3: DMTCLR: Deadman Timer Clear Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP2[7:0](1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STEP2[7:0]:** DMT Clear Timer bits(1)

00001000 = Clears STEP1[7:0], STEP2[7:0] and the Deadman Timer if preceded by the correct loading of the STEP1[7:0] bits in the correct sequence. The write to these bits may be verified by reading the DMTCNT register and observing the counter being reset.

All Other Write Patterns = Sets the BAD2 flag. The value of STEP1[7:0] will remain unchanged and the new value being written by STEP2[7:0] will be captured.

Note 1: Bits[7:0] are cleared when the DMT counter is reset by writing a correct sequence of STEP1 and STEP2.

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Register 2-4: DMTSTAT: Deadman Timer Status Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	U-0	U-0	U-0	U-0	R-0
BAD1(1)	BAD2(1)	DMTEVENT(1)	—	—	—	—	WINOPN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Bad STEP1[7:0] Value Detect bit(1)
- 1 = Incorrect STEP1[7:0] value was detected
- 0 = Incorrect STEP1[7:0] value was not detected

bit 6 **BAD2:** Bad STEP2[7:0] Value Detect bit(1)
- 1 = Incorrect STEP2[7:0] value was detected
- 0 = Incorrect STEP2[7:0] value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit(1)
- 1 = Deadman Timer event was detected (counter expired, or incorrect STEP1[7:0] or STEP2[7:0] value was entered prior to counter increment)
- 0 = Deadman Timer event was not detected

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit
- 1 = Deadman Timer clear window is open
- 0 = Deadman Timer clear window is not open

Note 1: BAD1, BAD2 and DMTEVENT bits are cleared only on a Reset.

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Register 2-5: DMTCNTL: Deadman Timer Count Register Low

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
COUNTER[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
COUNTER[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **COUNTER[15:0]:** Read Current Contents of Lower DMT Counter bits

Register 2-6: DMTCNTH: Deadman Timer Count Register High

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
COUNTER[31:24]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
COUNTER[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **COUNTER[31:16]:** Read Current Contents of Higher DMT Counter bits

Register 2-7: DMTPSCNTL: Post Status Configure DMT Count Status Register Low

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSCNT[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSCNT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT[15:0]:** Lower DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTL Configuration register.

Register 2-8: DMTPSCNTH: Post Status Configure DMT Count Status Register High

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSCNT[31:24]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSCNT[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT[31:16]:** Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

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Register 2-9: DMTPSINTVL: Post Status Configure DMT Interval Status Register Low

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSINTV[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSINTV[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSINTV[15:0]:** Lower DMT Window Interval Configuration Status bits
This is always the value of the FDMTIVTL Configuration register.

Register 2-10: DMTPSINTVH: Post Status Configure DMT Interval Status Register High

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSINTV[31:24]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSINTV[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSINTV[31:16]:** Higher DMT Window Interval Configuration Status bits
This is always the value of the FDMTIVTH Configuration register.

Register 2-11: DMTHOLDREG: DMT Hold Register

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
UPRCNT[15:8](1)							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
UPRCNT[7:0](1)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **UPRCNT[15:0]:** Contains Value of the DMTCNTH Register When DMTCNTL and DMTCNTH Registers were Last Read bits(1)

Note 1: The DMTHOLDREG register is initialized to '0' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

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3.0 DMT OPERATION

3.1 Modes of Operation

The primary function of the Deadman Timer (DMT) module is to interrupt the processor in the event of a software malfunction. The DMT module, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. The instructions are not fetched when the processor is in Sleep mode.

The DMT module consists of a 32-bit counter, the read-only DMTCNTL and DMTCNTH registers with a time-out count match value, as specified by the two external, 16-bit Configuration Fuse registers, FDMTCNTL and FDMTCNTH. Whenever the count match occurs, a DMT event will occur, which is nothing but a soft trap/interrupt. Refer to the **"Interrupt Controller"** chapter in the current device data sheet to check whether the DMT event is a soft trap or interrupt.

A DMT module is typically used in mission-critical and safety-critical applications, where any failure of the software functionality and sequencing must be detected.

3.2 Enabling and Disabling the DMT Module

The DMT module can be enabled or disabled by the device configuration or it can be enabled through software by writing to the DMTCON register.

If the DMTEN Configuration bit in the FDMT register is set, the DMT is always enabled. The ON control bit (DMTCON[15]) will reflect this by reading a '1'. In this mode, the ON bit cannot be cleared in software. To disable the DMT, the configuration must be rewritten to the device. If DMTEN is set to '0' in the fuse, then the DMT is disabled in hardware.

Software can enable the DMT by setting the ON bit in the Deadman Timer Control (DMTCON) register. However, for software control, the DMTEN Configuration bit in the FDMT register should be set to '0'. Once enabled, disabling the DMT in software is not possible.

3.3 DMT Count Windowed Interval

The DMT module has a Windowed Operation mode. The DMTIVT[15:0] and DMTIVT[31:16] Configuration bits in the FDMTIVTL and FDMTIVTH registers, respectively, set the window interval value. In Windowed mode, software can clear the DMT only when the counter is in its final window before a count match occurs. That is, if the DMT counter value is greater than or equal to the value written to the window interval value, then only the clear sequence can be inserted into the DMT module. If the DMT is cleared before the allowed window, a Deadman Timer soft trap or interrupt is immediately generated.

3.4 DMT Operation in Power-Saving Modes

As the DMT module is only incremented by instruction fetches, the count value will not change when the core is inactive. The DMT module remains inactive in Sleep and Idle modes. As soon as the device wakes up from Sleep or Idle, the DMT counter again starts incrementing.

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3.5 Resetting the DMT

The DMT can be reset in two ways: one way is using a system Reset and another way is by writing an ordered sequence to the DMTPRECLR and DMTCLR registers. Clearing the DMT counter value requires a special sequence of operations:

1. The STEP1[7:0] bits in the DMTPRECLR register must be written as '01000000' (0x40):
   - If any value other than 0x40 is written to the STEP1x bits, the BAD1 bit in the DMTSTAT register will be set and it causes a DMT event to occur.
   - If Step 2 is not preceded by Step 1, BAD1 and DMTEVENT Flags are set. BAD1 and DMTEVENT flags gets cleared only on a device Reset.
2. The STEP2[7:0] bits in the DMTCLR register must be written as '00001000' (0x08). This can only be done if preceded by Step 1 and the DMT is in the open window interval. Once correct values are written, the DMT counter will be cleared to zero. The DMTPRECLR, DMTCLR and DMTSTAT registers' value will also be cleared zero.
   - If any value other than 0x08 is written to the STEP2x bits, the BAD2 bit in the DMTSTAT register will be set and causes a DMT event to occur.
   - Step 2 is not carried out in the open window interval; it causes the BAD2 flag to be set. A DMT event immediately occurs.
   - Writing back-to-back preclear sequences (0x40) also causes the BAD2 flag to be set and causes a DMT event.

Note:	After an invalid preclear/clear sequence, it takes at least two cycles to set the BAD1/BAD2 flag and three cycles at least to set the DMTEVENT.

The BAD2 and DMTEVENT flags gets cleared only on a device Reset. Refer to the flowchart as shown in Figure 3-1.

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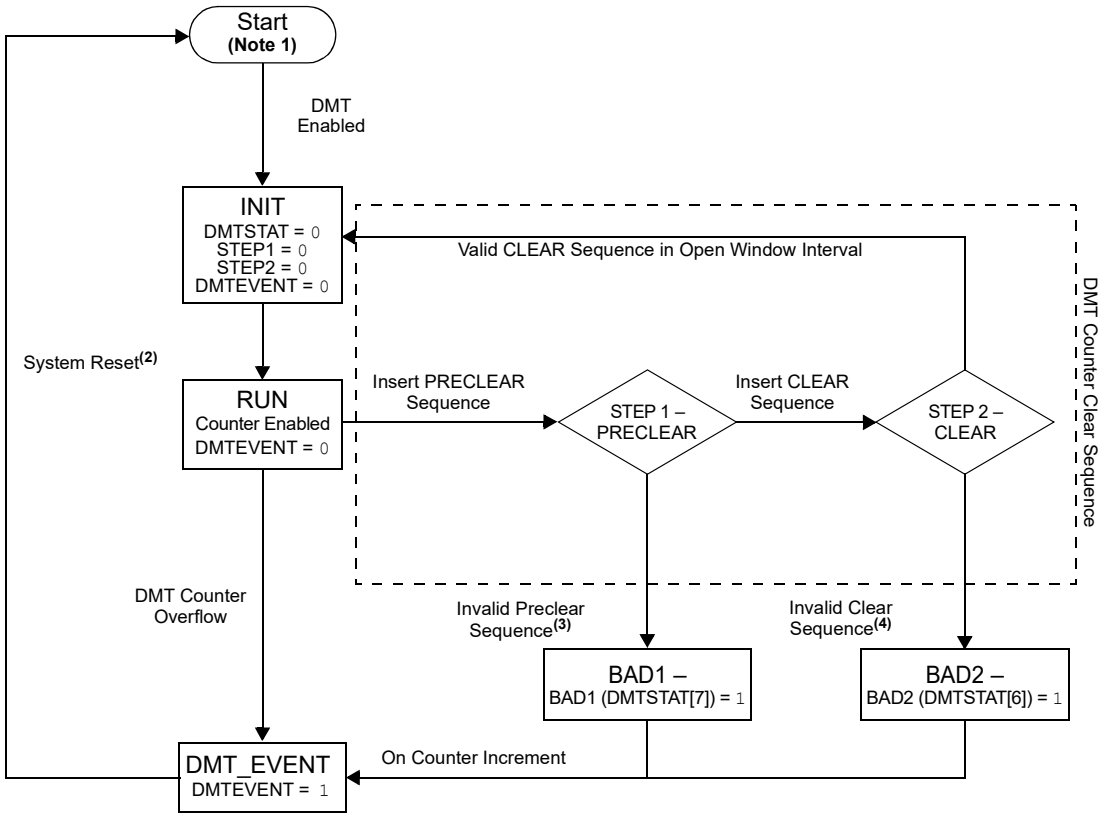
Figure 3-1: Flowchart for DMT Event



Note 1: DMT is enabled (ON (DMTCON[15]) as qualified by FDMT in the Configuration Fuses.

2: DMT counter can be reset after the counter expiry or BAD1/BAD2 occurrences only by device Reset.

3: STEP2x before STEP1x (DMTCLEAR written before DMTPRECLEAR) or BAD_STEP1 (DMTPRECLEAR written with value not equal to 0x40).

4: STEP1x (DMTPRECLEAR written again after STEP1x), or BAD_STEP2 (DMTCLR written with value not equal to 0x08) or window interval is not open.

3.6 DMT Count Selection

The Deadman Timer count is set by the DMTCNTL[15:0] and DMTCNTH[31:16] register bits in the FDMTCNTL and FDMTCNTH registers, respectively. The current DMT count value can be obtained by reading the lower and higher Deadman Timer Count registers, DMTCNTL and DMTCNTH.

The PSCNT[15:0] and PSCNT[31:16] bits in the DMTPSCNTL and DMTPSCNTH registers, respectively, allow the software to read the maximum count selected for the Deadman Timer. That means these PSCNTx bit values are nothing but the values that are initially written to the DMTCNTx bits in the Configuration Fuse registers, FDMTCNTL and FDMTCNTH. Whenever the DMT event occurs, the user can always compare to see whether the current counter value in the DMTCNTL and DMTCNTH registers is equal to the value of the DMTPSCNTL and DMTPSCNTH registers, which hold the maximum count value.

The PSINTV[15:0] and PSINTV[31:16] bits in the DMTPSINTVL and DMTPSINTVH registers, respectively, allow the software to read the DMT window interval value. That means these registers read the value which is written to the FDMTIVTL and FDMTIVTH registers. So whenever the DMT current counter value in DMTCNTL and DMTCNTH reaches the value of the DMTPSINTVL and DMTPSINTVH registers, the window interval opens so that the user can insert the clear sequence to the STEP2x bits, which causes the DMT to reset.

The UPRCNT[15:0] bits in the DMTHOLDREG register hold the value of the last read of the DMT upper count values (DMTCNTH) whenever DMTCNTL and DMTCNTH are read.

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4.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 product families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Deadman Timer (DMT) are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip website (www.microchip.com) for additional Application Notes and code examples for the dsPIC33/PIC24 family of devices.

5.0 REVISION HISTORY

Revision A (February 2014)

This is the initial released version of this document.

Revision B (March 2022)

Updates Figure 1-1 and Figure 3-1.

Updates Register 2-1, Register 2-2, Register 2-3, Register 2-4, Register 2-9 and Register 2-10.

Updates Table 2-1 and Table 2-2.

Updates **Section 1.0 “Introduction”**, **Section 2.0 “DMT Registers”**, **Section 3.1 “Modes of Operation”**, **Section 3.2 “Enabling and Disabling the DMT Module”**, **Section 3.3 “DMT Count Windowed Interval”**, **Section 3.5 “Resetting the DMT”** and **Section 3.6 “DMT Count Selection”**.

Moves the Register Map to **Section 2.0 “DMT Registers”**.

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