Multi Channel DMA Intel® FPGA IP for PCI Express* Release Notes

Online Version
Send Feedback

RN-1242

683791
2024.01.19

Contents

1. Multi Channel DMA Intel FPGA IP for PCI Express : IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- Multi Channel DMA for PCI Express Intel FPGA IP User Guide
- Multi Channel DMA for PCI Express Intel FPGA IP Design Example User Guide

1.1. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 23.1.0] [P-Tile: 7.1.0] [F-Tile: 8.0.0] [R-Tile: 4.1.0]

Table 1. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 23.1.0] [P-Tile: 7.1.0] [F-Tile: 8.0.0] [R-Tile: 4.1.0] : 2024.01.12

Intel Quartus Prime Version	IP Version	Description	Impact
23.4	[H-Tile: 23.1.0] [P-Tile: 7.1.0] [F-Tile: 8.0.0] [R-Tile: 4.1.0]	Added support for concurrent (run separately) 2x8 mode in P-Tile MCDMA IP for Intel Stratix® 10 DX device.	You can instantiate two separate instances of P-Tile MCDMA IP Core in 2 x8 mode for Intel Stratix 10 DX device.
		P-Tile MCDMA IP Performance values are consistent across DPDK and Custom Driver using max speed and link width	You can use DPDK or Custom Driver to get performance values.

continued...

Intel Quartus Prime Version	IP Version	Description	Impact
		Added support for Endpoint MSI interrupt interface in BAS and BAM+BAS modes for H-Tile MCDMA IP.	You can use MSI request interface to trigger MSI messages
		Removed `pld_warm_rst_rdy` and `link_req_rst_n` interfaces from F-Tile MCDMA IP and P-Tile MCDMA IP.	These internal interfaces were exported only when "Export pld_warm_rst_rdy and link_req_rst_n interface to top level" IP parameter GUI is selected. This IP parameter is not available on the P-Tile MCDMA IP and F-Tile MCDMA IP.
		Added PTM interfaces for R-Tile MCDMA Endpoint in Ports 0 and 1.	You can use PTM interfaces to trigger PTM messages.

1.2. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 23.0.0] [P-Tile: 7.0.0] [F-Tile: 7.0.0] [R-Tile: 4.0.0]

Table 2. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 23.0.0] [P-Tile: 7.0.0] [F-Tile: 7.0.0] [R-Tile: 4.0.0] : 2023.10.03

Intel Quartus Prime Version	IP Version	Description	Impact
23.3	[H-Tile: 23.0.0] [P-Tile: 7.0.0] [F-Tile: 7.0.0] [R-Tile: 4.0.0]	Fixed stability netdev_app tool issues on Network Device Driver with PIO bypass mode test.	netdev_app won't see instability issues on PIO bypass mode test.
		R-Tile MCDMA IP added support for Configuration via Protocol (CVP) flow for a single tile only.	You can configure the FPGA using CVP flows.
		Added support for PIPE Mode Simulation for R-Tile MCDMA IP only.	When enabled, the R-Tile MCDMA IP exposes PIPE interface. This interface is used to connect a BFM with PIPE interface support and improve the overall simulation time.
		Added Design Example simulation support for R-Tile PIO with MCDMA Bypass Mode in Xcelium*, QuestaSim* and Questa* Intel FPGA Edition.	You can only simulate PIO using MCDMA Bypass Mode with all supported User Modes up to Gen5 x8 link in the Intel Agilex® 7 I-Series FPGA devices using R-Tile.
		Added a new Hard IP Modes and PLD clock frequencies support for R-Tile MCDMA IP: • Gen5 4x4 Interface - 256 bits (PLD Clock Frequency 500 MHz / 475 MHz / 450 MHz / 425 MHz / 400 MHz)	You can implement Gen5 4x4 link in the Intel Agilex 7 FPGA devices using R-Tile MCDMA IP.
		Removed `pld_warm_rst_rdy` and `link_req_rst_n` interfaces from R-Tile MCDMA IP.	These internal interfaces were exported only when **Export pld_warm_rst_rdy and**

continued...

Intel Quartus Prime Version	IP Version	Description	Impact
			link_req_rst_n interface to top level parameter selected. This IP parameter is not available on the R-Tile MCDMA IP.
		Software directory is created multiple times depending on the number of Hard IP ports selected. pX_software folder where X = 0, 1, 2, 3.	Software folder is specific to the example design and IP port. You must use the corresponding software folder with each IP port.
		Added support to request memory PIO read and write with custom driver.	You can read and write from PIO address range in bar 2 from any valid custom memory.
		Fixed MCDMA Custom Driver issue for Ubuntu 22.04 LTS operating system when Virtual Function I/O (VFIO) kernel mode and MSIX mode are set.	You can use it with VFIO kernel and MSIX mode.
		Added Analog Parameters tab in the IP Parameter Editor for F-Tile MCDMA IP to enable transceiver analog settings for low loss PCIe design.	You should only enable this parameter for chip to chip PCIe design with F-Tile to ensure good link quality.

1.3. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 22.3.0] [P-Tile: 6.0.0] [F-Tile: 6.0.0] [R-Tile: 3.0.0]

Table 3. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 22.3.0] [P-Tile: 6.0.0] [F-Tile: 6.0.0] [R-Tile: 3.0.0] : 2023.06.26

Intel Quartus Prime Version	IP Version	Description	Impact
23.2	[H-Tile: 22.3.0] [P-Tile: 6.0.0] [F-Tile: 6.0.0] [R-Tile: 3.0.0]	Added support for 4x4 bifurcation mode only Root Port in P-Tile MCDMA IP P-Tile MCDMA IP Design Example Root Port simulation and hardware are not supported	You can instantiate 4x4 separate instances of P-Tile MCDMA IP Core in x4 mode in Root Port only
		Added support for independent and concurrent Gen4/3 4x4 bifurcation mode in R-Tile MCDMA IP. R-Tile MCDMA IP Design Example Root Port simulation and hardware are not supported. R-Tile MCDMA IP Design Example Endpoint simulation is not supported.	You can instantiate 4 separate instances of R-Tile MCDMA IP Core in x4 mode in Root Port and Endpoint: • Endpoint / Endpoint / Endpoint / Endpoint • Endpoint / Endpoint / Root port / Root port • Endpoint / Root port / Root port / Root port • Root port / Root port / Root port / Root port
		R-Tile MCDMA IP in 4x4 Port 2 and 3 don't support SRIOV, FLR, MSI-X and MSI features. These ports only support BAM, BAS and BAM+BAS User Modes	R-Tile MCDMA Endpoint has limited support for port 2 and 3.

continued...

Intel Quartus Prime Version	IP Version	Description	Impact
		Added new Hard IP Mode options and PLD clock frequencies support below for F-Tile MCDMA IP: • Gen4 1x4, Interface - 128 bit (PLD Clock Frequency 500 MHz / 450 MHz / 400 MHz / 350 MHz) for endpoint • Gen3 1x4, Interface - 128 bit (PLD Clock Frequency 250 MHz) for endpoint • Gen4 2x4, Interface - 128 bit (PLD Clock Frequency 500 MHz / 450 MHz / 400 MHz / 350 MHz) for root port • Gen3 2x4, Interface - 128 bit (PLD Clock Frequency 250 MHz) for root port • Gen4 4x4, Interface - 128 bit (PLD Clock Frequency 500 MHz / 450 MHz / 400 MHz / 350 MHz) for root port • Gen3 4x4, Interface - 128 bit (PLD Clock Frequency 250 MHz) for root port	You can generate the IP with the newly supported Hard IP Mode but not the design example.
		Fixed vector masking capability for User Event MSI-X interrupt in MCDMA IP.	MCDMA IP is capable to mask User Event MSI-X interrupt when mask-bit is set in the vector control register.
		Added the following new Hard IP Modes and PLD clock frequencies support for P-Tile MCDMA IP: • Gen4 4x4 Interface - 128 bit (PLD Clock Frequency 500 MHz / 450 MHz / 400 MHz / 350 MHz) • Gen3 4x4 Interface - 128 bit (PLD Clock Frequency 250 MHz)	PCIe port bifurcation x4 is now supported by P-Tile MCDMA IP
		Added support for Root Port Address Translation Table in BAS and BAM+BAS modes (R-Tile MCDMA IP)	You can use ATT to access 64-bit PCIe address space
		Added the following new Hard IP Modes and PLD clock frequencies support for R-Tile MCDMA IP: • Gen4/Gen3 4x4 Interface - 256 bits (PLD Clock Frequency 300 MHz / 275 MHz / 250 MHz) • Gen4 4x4 Interface - 128 bits (PLD Clock Frequency 500 MHz / 475 MHz / 450 MHz / 425 MHz / 400 MHz) • Gen3 4x4 Interface - 128 bits (PLD Clock Frequency 300 MHz / 275 MHz / 250 MHz)	PCIe port bifurcation is now supported by R-Tile MCDMA IP
		Added support for Endpoint MSI interrupt request interface in BAS and BAM+BAS modes (R-Tile MCDMA IP)	You can use MSI request interface to trigger MSI messages
		Added support for concurrent 2x8 bifurcation mode in R-Tile MCDMA IP	You can instantiate two separate instances of R-Tile MCDMA IP Core in x8 mode
		Fixed dropping Posted Writes in P-Tile MCDMA AVMM PIO when user logic backpressures by asserting `rx_pio_waitrequest_i`	MCDMA AVMM interface handles PIO wait request from user logic when there is Poste Writes back to back into AVMM PIO

1.4. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 22.2.0] [P-Tile: 5.1.0] [F-Tile: 5.1.0] [R-Tile: 2.0.0]

Table 4. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 22.2.0] [P-Tile: 5.1.0] [F-Tile: 5.1.0] [R-Tile: 2.0.0] : 2023.04.10

Intel Quartus Prime Version	IP Version	Description	Impact
23.1	[H-Tile: 22.2.0] [P-Tile: 5.1.0] [F-Tile: 5.1.0] [R-Tile: 2.0.0]	D2H throughput is no longer impacted in MCDMA R-Tile when the test is running on Ubuntu 22.04 Operating System.	You can run performance test on Ubuntu 22.04 LTS kernel:5.15.0-52-generic.
		DPDK Poll mode and NetDev drivers are supported on Ubuntu 22.04 LTS for MCDMA IP Intel Quartus Prime version 23.1 and beyond.	Ubuntu 22.0 LTS kernel: 5.15.0-52-generic supports all three drivers.
		Fixed completion reordering issue on MCDMA IP with BAS & MCDMA user modes when 10-bit tag feature is enabled but Intel Quartus Prime Hard IP auto negotiated to only a 8-bit tag.	MCDMA IP won't show this issue after negotiated 8-bit tag when 10-bit tag feature was initially enabled. This applies to P-Tile, F-Tile and R-Tile.
		R-Tile PIO using MCDMA Bypass Mode Design Example simulation is supported in VCS*/VCS MX in the Intel Quartus Prime 23.1 release.	You can only simulate PIO using MCDMA Bypass Mode with all supported User Modes up to Gen5 x8 link in the Intel Agilex® 7 I-Series FPGA devices using R-Tile.
		DPDK driver version upgraded to v21.11.2 for Ubuntu 22.04	You must use DPDK driver v21.11.2 for Ubuntu OS and v20.05-rc1 for CentOS

1.5. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 22.1.0] [P-Tile: 5.0.0] [F-Tile: 5.0.0] [R-Tile: 1.0.0]

Table 5. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 22.1.0] [P-Tile: 5.0.0] [F-Tile: 5.0.0] [R-Tile: 1.0.0] : 2022.12.27

Intel Quartus Prime Version	IP Version	Description	Impact
22.4	[H-Tile: 22.1.0] [P-Tile: 5.0.0] [F-Tile: 5.0.0] [R-Tile: 1.0.0]	The default User Mode parameter on m1 instance fixed when Root Port Mode is selected.	Users can implement MCDMA IP in Root Port Mode.
		Fixed the MCDMA P-Tile BAM performance issue when BAM+BAS Mode and Traffic Generator/Checker Design Example is compiled.	Hardware is capable to reach expected performance.
		Initial release of MCDMA R-Tile IP Core. Added support for R-Tile Gen5 x8, Gen4/Gen3 x16 and Gen4/Gen3 x8 (Root Port,Endpoint). MCDMA R-Tile Hardware support is available in Intel Quartus Prime 22.4 Release Patch 0.02.	Users can implement up to Gen5 x8 link in the Intel Agilex 7 FPGA devices using R-Tile.
		Added support for BAM-BAS-MCDMA (EP) user mode, for MCDMA H-Tile, P-Tile and F-Tile IP Cores.	Users can now use BAM, BAS and MCDMA modes simultaneously in Endpoint mode applications.

continued...

Intel Quartus Prime Version	IP Version	Description	Impact
		R-Tile MCDMA Design Example simulations are not supported in this Intel Quartus Prime release.	-
		MCDMA R-Tile MSI, simultaneous BAM+BAS+MCDMA and Root Port ATT features in the Intel Quartus Prime GUI are not supported	Support for these features may be added in a future Intel Quartus Prime release.
		Removed `pld_clrpcs_n_i` input from MCDMA P-Tile IP Core. New reset signals (`p#_warm_perst_n_i`, `p#_cold_perst_n_i`) are exported to the top-level block symbol when independent resets are enabled.	IP Upgrade tool does not upgrade automatically and requires manual upgrade (Upgrade in Editor). If `pld_clrpcs_n_i` reset was used by application logic, switch to new reset signals input before manual upgrade.
		Removed support for kernel mode Char driver.	Users can use netdev (kernel mode) driver and custom and DPDK (user mode) driver.
		Added support for Independent cold and warm reset operations for the ports in the x8x8 Endpoint in F-Tile.	New reset signals (`i_gpio_perst#_n`) are exported to the top-level block symbol when independent resets are enabled.

1.6. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 22.0.0] [P-Tile: 4.0.0] [F-Tile: 4.0.0]

Table 6. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 22.0.0] [P-Tile: 4.0.0] [F-Tile: 4.0.0] : 2022.10.11

Intel Quartus Prime Version	IP Version	Description	Impact
22.3	[H-Tile: 22.0.0] [P-Tile: 4.0.0] [F-Tile: 4.0.0]	Added support for Root Port Address Translation Table in BAS and BAM+BAS modes (MCDMA P and F Tiles)	You can use ATT to access 64-bit PCIe address space.
		Added support for Endpoint MSI request interface in BAS and BAM+BAS modes (MCDMA P and F Tiles)	You can use MSI request interface to trigger MSI messages.
		Added support for 2x8 bifurcation mode (MCDMA P and F Tiles)	You can instantiate two separate instances of MCDMA IP Core in x8 mode
		Added support for 64-byte non-aligned support for NetDev	With Enable address byte aligned transfer checked, this enables byte aligned data transfer in AVST H2D direction.
		Enhanced Packet Generator/Checker example design to support the Channel and Function ID information	Supported in Custom and DPDK based MCDMA drivers.

continued...

Intel Quartus Prime Version	IP Version	Description	Impact
		Added support for D2H Data Mover Data Drop feature	Supported in Custom and DPDK based MCDMA drivers.
		Added the following new Hard IP Modes and PLD clock frequencies support: • Gen4 1x16 Interface - 512 bit (PLD Clock Frequency 175 MHz / 200 MHz / 225 MHz / 250 MHz) • Gen4 2x8 Interface - 256 bit (PLD Clock Frequency 175 MHz / 200 MHz / 225 MHz / 250 MHz) • Gen3 2x8 Interface - 256 bit (PLD Clock Frequency 250 MHz)	PCIe port bifurcation is now supported by MCDMA IP for P-Tile and F-Tile. IT allows users to implement two PCIe links with MCDMA IP on a single tile. Lower PLD clock frequency options are provided to ease timing closure when the throughput of the PCIe link can be a trade off.
		Added Intel Agilex F-Series F-Tile ES FPGA Development Kit board preset for design example generation.	The VID-related settings including the pin assignments are included in the .qsf file of the generated design example when selected.
		Added Eye Viewer feature in F-Tile Debug Toolkit while in Endpoint mode and using Linux OS and Windows.	Allows users to measure on-die eye height margin.

1.7. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 21.5.0] [P-Tile: 3.1.0] [F-Tile: 3.0.0]

Table 7. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 21.5.0] [P-Tile: 3.1.0] [F-Tile: 3.0.0] : 2022.07.01

Intel Quartus Prime Version	IP Version	Description	Impact
22.2	[H-Tile: 21.5.0] [P-Tile: 3.1.0] [F-Tile: 3.0.0]	Enabled example designs for BAM+MCDMA mode AVST interface type	You can select 'Device-side Packet Loopback' and 'Packet Generate/Check' example designs when you choose BAM+MCDMA mode AVST type.
		Enabled F-Tile Debug Toolkit support for MCDMA F-Tile IP Core.	You can enable Debug Toolkit for MCDMA F-Tile IP Core
		Changed BAS AVMM Slave waitrequestAllowance to 0	BAS AVMM Slave interface accept no Read/Write transactions after waitrequest is asserted.
		Removed 32-bit prefetchable memory from BAR type options	32-bit prefetchable memory type is not supported
		Deprecated 4 port AVST interface support for MCDMA modes	MCDMA AVST interface supports 1 port mode only.

1.8. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 21.4.0] [P-Tile: 3.0.0] [F-Tile: 2.0.0]

Table 8. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 21.4.0] [P-Tile: 3.0.0] [F-Tile: 2.0.0] : 2022.04.04

Intel Quartus Prime Version	IP Version	Description	Impact
22.1	[H-Tile: 21.4.0] [P-Tile IP: 3.0.0] [F-Tile: 2.0.0]	No feature updates to MCDMA IP for the Intel Quartus Prime 22.1 release	-

1.9. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 21.3.0] [P-Tile: 2.2.0] [F-Tile: 1.1.0]

Table 9. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 21.3.0] [P-Tile: 2.2.0] [F-Tile: 1.1.0] : 2022.01.14

Intel Quartus Prime Version	IP Version	Description	Impact
21.4	[H-Tile: 21.3.0] [P-Tile: 2.2.0] [F-Tile: 1.1.0]	Multi-channel support in netdev	Currently supports 512 channels in each PF
		SRIOV support in netdev	You can enable multiple VFs by using sysfs interface
		ethtool enhancements	Queue management and Ring management support enabled from ethtool command
		Added a new MCDMA user mode, the Data Mover Only mode, for MCDMA P-Tile and F-Tile IP Cores.	You can attach external/ custom descriptor controller.
		Added 10-bit tag support	Enables MCDMA to support greater than 256 outstanding Non-Posted Requests
		Simulation bug fix for: • BAM user mode : PIO using MQDMA Bypass mode design example variant. • MCDMA+BAM : PIO using MQDMA Bypass mode design example variant. • BAM+BAS user mode : Traffic Generator/Checker design example variant.	Allows you to simulate the design examples with the supported simulator.

1.10. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 21.2.0] [P-Tile: 2.1.0] [F-Tile: 1.0.0]

Table 10. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [H-Tile: 21.2.0] [P-Tile: 2.1.0] [F-Tile: 1.0.0] : 2021.11.24

Intel Quartus Prime Version	IP Version	Description	Impact
21.3	[H-Tile: 21.2.0] [P-Tile: 2.1.0] [F-Tile: 1.0.0]	Added Intel Stratix 10 DX P-Tile Production FPGA Development Kit option for Target Development Kit	Allow users to generate design example with Intel Stratix 10 DX P-Tile Production FPGA Development Kit board settings.
		Removed `coreclkout_hip` output from MCDMA P-Tile IP Core	IP Upgrade tool doesn't upgrade automatically and requires manual upgrade (Upgrade in Editor). If this clock was used by application logic, switch to `app_clk` output before manual upgrade.
		Reduced Root Port Config Slave interface address (`cs_address_i`) width from 29 bits to 14 bits	This allows users to save system memory space. Requires 2 clock cycles to perform config read/write to Endpoint configuration registers.
		Increased DMA channel support to 2K for MCDMA AVST 1 port mode	Enables DMA bandwidth sharing up to 2K channels. This enables more VMs/PFs/VFs to utilize MCDMA to perform data move between the Host and device.
		Added support for "Traffic generator/checker" example design for BAS in EP mode and corresponing s/w support.	User can test the example application for BAS transactions. User needs to select ''BAM_BAS" user mode in the IP.
		Added MCDMA IP NetDev Mode driver	MCDMA network driver exposes the device as ethernet device. All TCP/IP socket based applications can use this driver to perform data transfer by using DMA. User needs to select "Device-side packet looback" example design.
		Initial release of MCDMA F-Tile IP Core. Added support for F-Tile Gen4/Gen3 x16 (Root Port,Endpoint) and x8 (Endpoint).	You can implement up to Gen4 x16 link in the Intel Stratix 10 and Intel Agilex FPGA devices using F-Tile.
		Support for AVST 1 port 2K DMA channels	Enables DMA bandwidth sharing up to 2K channels.

continued...

Intel Quartus Prime Version	IP Version	Description	Impact
		BAS Support	IP, Example design, Software enhanced to support BAS.
		Added Support for kernel net-dev driver.	MCDMA network driver, exposes the device as ethernet device. All TCP/IP socket based applications, can use this driver to perform data transfer by using DMA.
		Initial release of Debug Toolkit for MCDMA P-Tile IP Core	You can use the Debug Toolkit to monitor link status and various config registers for diagnostic and debugging purpose.

1.11. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [P-Tile: v2.0.0] [H-Tile: v21.1.0]

Table 11. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [P-Tile: 2.0.0] [H-Tile: 21.1.0] 2021.09.29

Intel Quartus Prime Version	IP Version	Description	Impact
21.2	[P-Tile: v2.0.0] [H-Tile: v21.1.0]	Fixed H-Tile IP revision number	Enables automatic upgrade by Intel Quartus Prime Pro Edition software
		Added 500 MHz support for Intel Agilex 7 P-Tile MCDMA IP	Provides maximum Gen4 link bandwidth
		Added P-Tile single port Avalon-ST DMA up to 256 channels	Enables efficient DMA bandwidth sharing and utilization
		Added MCDMA IP Kernel Mode (No SRIOV) driver	You can perform DMA operations to and from memory buffer allocated in user space using chardev system calls (open, close, poll, read, write, etc)
		Fixed port width of MCDMA P-Tile `usr_hip_tl_cfg_func_o` and `usr_hip_tl_cfg_ctl_o`: • `usr_hip_tl_cfg_func_o [1:0] --> usr_hip_tl_cfg_func_o [2:0]` • `usr_hip_tl_cfg_ctl_o [31:0] --> usr_hip_tl_cfg_ctl_o [15:0]`	You need to adjust application logic port width according to the IP port width if these ports are used in your application.

1.12. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [P-Tile: v1.0.0] [H-Tile: v2.0.0]

Table 12. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core [P-Tile: 1.0.0] [H-Tile: 2.0.0] 2021.07.19

Intel Quartus Prime Version	IP Version	Description	Impact
21.1	[P-Tile: v1.0.0] [H-Tile: v2.0.0]	Added support for P-Tile Gen4/Gen3 x16 (Root Port, Endpoint) and x8 (Endpoint).	You can implement up to Gen4 x16 link in Intel Stratix 10 DX and Intel Agilex 7 FPGA device families.
		Added support for H-Tile Gen3 x8 and Root Port mode.	You can implement Gen3 x16/x8 link in Intel Stratix 10 GX and MX device families.
		Added support for various user modes: Multi channel DMA (EP), Bursting Master (RP, EP), Bursting Slave (RP, EP), BAM-BAS (RP, EP) and BAM-MCDMA (EP).	You can implement a user mode that best suits your application needs based on the port usage (Root Port / Endpoint).
		Added support for Configuration Slave interface for Root Port mode.	You can write to/read from the downstream Endpoint configuration space registers using the Config Slave interface.
		Added support for user MSI-X in MCDMA mode.	You can trigger an MSI-X in MCDMA mode.
		Added support for user FLR in MCDMA mode.	Endpoint user logic can be reset by the Function Level Reset.
		Added support for SR-IOV.	You can implement multiple PFs/VFs: Up to 8 PFs in P-Tile and 4 PFs in H-Tile.
		Added support for MCDMA AVST 1 port interface.	AVST 1 port interface enables you to implement multiple channels of H2D/D2H DMA.
		Support for increased DMA channels: - • AVMM Interface: up to 2K (max 512 per function) • AVST 1 port Interface: [P-Tile: 64] [H-Tile: 256]	You can allocate more DMA channels to a function.
		Added support for D2H Descriptor Prefetch in AVST 1 port mode.	You can configure the number of prefetch channels and maximum descriptor fetch.
		Added support for 8-byte Metadata	In MCDMA AVST mode, you can re-purpose the descriptor H2D destination address and D2H source address fields to carry application specific metadata.
		Added support for DPDK PMD and Kernel mode drivers	You can implement MCDMA software using these drivers.

1.13. Multi Channel DMA Intel FPGA IP for PCI Express : IP Core v20.0.0

Table 13. Multi Channel DMA Intel FPGA IP for PCI Express : IP Version v20.0.0 2020.08.14

Intel Quartus Prime Version	Description	Impact
20.2	Initial Release	-

1.14. Multi Channel DMA Intel FPGA IP for PCI Express : User Guide Archives

For the latest and previous versions of this document, refer to the Multi Channel DMA Intel FPGA IP for PCI Express User Guide. If an IP or software version is not listed, the user guide for the previous IP or software version applies.