August 7th, 2025

1. Introduction

This document summarizes the results of Diodes Incorporated's (Diodes) analysis and testing of the quality, reliability, and usability of Diodes semiconductor finished good (FG) components that were subject to long-term storage (LTS) under controlled environmental conditions per applicable Jedec Standards, typically <30°C / 85%RH.

Diodes' goal was to generate and collect sufficient supporting data based on FG manufactured across multiple package types and assembly & test facilities to ensure product quality and reliability may not be negatively impacted by long-term storage of up to 3 years from the date of manufacture.

2. Background

Diodes has consistently been applying thorough and comprehensive qualification requirements to all semiconductor packages and assembly bill of materials (BOM) prior to making them available for selection for component qualification of FGs. Reliability test conditions as well as acceptance criteria are based on Jedec, and for automotive products, on AEC-Qxxx standards.

Furthermore, design and process technologies, equipment, and tools for the manufacture of semiconductor wafers, assembly BOM, packing and shipping materials, as well as handling and storage procedures have evolved and been continuously improved over many years to ensure that today's products shipped by Diodes are robust and not affected by extended age or shelf life.

As such, Diodes FG are initially qualified and subsequently handled, packed, stored, and shipped in accordance with applicable revisions of JESD22-A113, J-STD-020, J-STD-033, with Diodes following the guidelines and recommendations to maintain quality and reliability of components as outlined in JEP160 for LTS.

3. Procedure

For this particular study, Diodes sampled FG aged between 2 and 3 years from the date of manufacture. Samples originated from various distinct product families that were manufactured with die from different wafer fabs, different assembly BOM, and packages from multiple assembly & test sites. Components were then subjected to hi-reliability testing, solderability testing, inspection of packing material as well as tape & reel (T&R) peel testing, as applicable.

1) Package material evaluation and check, including labels, and for MSL 3 vacuum sealed products inspection of humidity indicator cards (HIC)
2) Cover tape peeling force test on T&R
3) Visual inspection of products on T&R, i.e. any visible discoloration or oxidization on leads.
4) Reliability Stress Tests on 77 units per lot per test
    a) Preconditioning – Bake 24 hours @ 125°C, Soak 168 hours @ 85°C / 85% RH (MSL 1), or 192 hours @ 30°C / 60% RH (MSL 3), 3x IR @ 260°C
    b) Highly Accelerated Stress Test (HAST) – 96 hours
    c) Temperature Cycling (TC) – 168 cycles
    d) Pressure Cooker Test (PCT) – 96 hours
    e) High Temperature Reverse Bias (HTRB) – 168 hours
    f) High Temperature Operating Life (HTOL) testing – 168 hours
5) Solderability Testing – 10 units per package
6) Reflow test: Three cycles reflow @ 260°C then electrical final test (FT) – 1,500 units per package

Assembly Site	# Sampled Lots	# Units	Package Types (incl. Cu, PdCu, Al, Au wire; and Clip)
# 1	114	31,361	DFN, ITO220, MSOP, PowerDi, QFN, SC, SIP, SO, SOD, SOT, TO
# 2	67	17,225	DFN, MSOP, PowerDi, QFN, SO, SOC, SOT, WLCSP
# 3	25	7,950	DO, SMA, SMB, SMC
# 4	23	7,314	DFS, GBJ, GBL, GBP, GBU, ITO220, KBJ, KBP, MiniDip, SOPA, TD, TO220

4. Packing Inspection Procedure

The product packing of sampled FG was carefully examined as soon as the samples were received at the corresponding labs. Labels on bags and boxes were evaluated for legibility and adhesion. For MSL 3 products, the Moisture Barrier Bags (MBB) were inspected for any vacuum leaks. The Humidity Indicator Cards (HIC) inside the MBBs were visually checked to ensure no color changes, i.e. no moisture penetration had occurred into the MBB. Subsequently, a cover tape peel test was performed to ensure adequate adhesion due to long term storage.

a. Packing Material Inspection

4.1: Sample of shipping box

4.2: Side view of shipping box

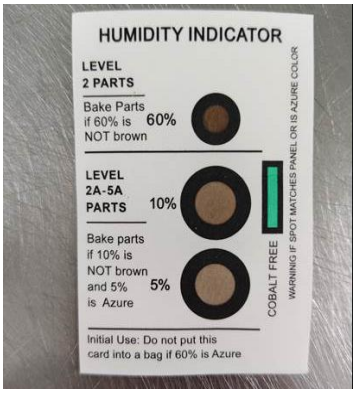
4.3: Inner box with MSL1 packing

4.4: MSL 1 Reel

4.5: Inner box with MSL 3 packing

4.6: Opened inner box - vacuum sealed bag with MSL3 packing

4.7: Opened vacuum sealed bag



4.8 HIC - Reel & HIC & Desiccant

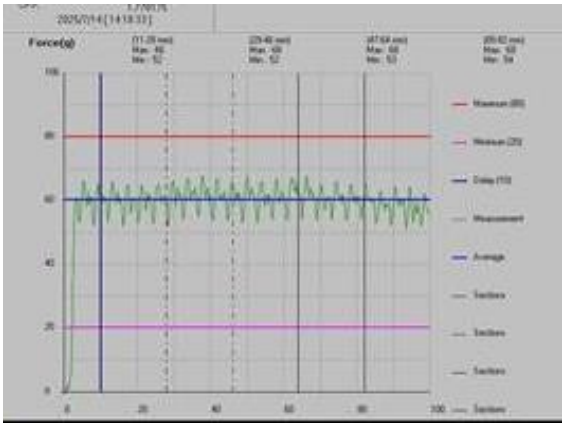
4.9: Moisture Barrier Bag (MBB) for MSL 3 products

In compliance with J-STD-033 and based on the test results and the analysis conducted by Diodes outlined in this report, the maximum shelf life in sealed bags currently stated in item #1 on the Caution label for MSL 3 products will be adjusted accordingly.

b. Cover Tape Peel Strength Evaluation

A sample strip was cut from the original tape and reel and the peel force of the cover tape was measured during the removal of the cover tape. The test was to evaluate that the cover tape adhesion did not change over the long term storage of the reel. The peel force of the cover tape was measured within the 10 gram minimum force and 130 gram maximum limit according to industry standard EIA 481. The peeling speed of the cover tape was set to 300 mm per minute. This test is also referenced as a peel-back test in the industry.

4.9: Peeling force measurement test setup



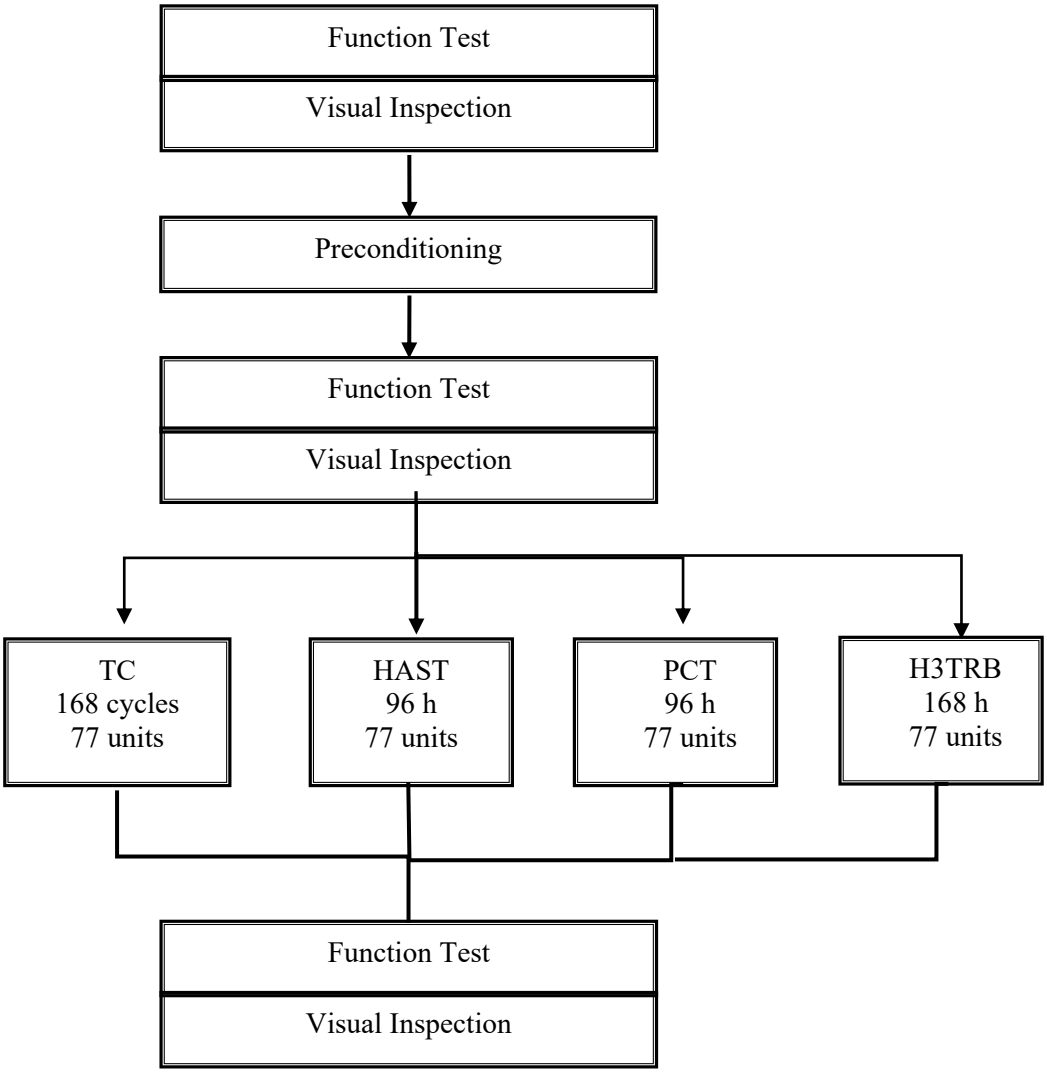
4.10: Peeling force measurement data, i.e. typical 8mm tape, 3 years

Subsequently, samples were prepared for and submitted for reliability stress and solderability testing as outlined above to ensure electrical performance and functionality, and wettability were within internal specifications as well as published product datasheets.

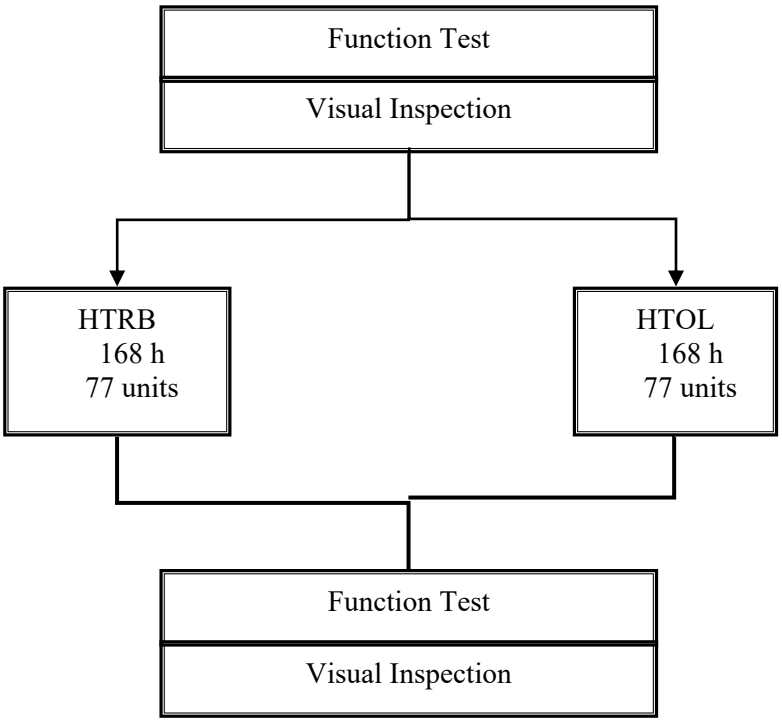
5. Reliability Test Evaluations

a. Reliability Test Flows

i. Test Flow with Preconditioning:



ii. Test flow without Preconditioning:



b. Preconditioning

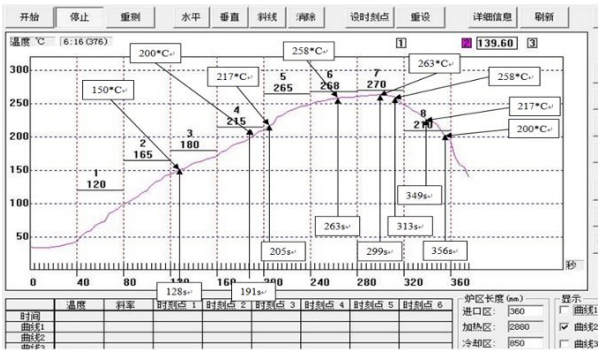
Samples were submitted to preconditioning per JESD22-A113 prior to hi-rel stress tests (HAST/PCT/TC). The post preconditioning test and visual inspection did not reveal any failures or package damages/cracks.

Preconditioning included 24 hours of bake at 125°C, 168 hours 85°C/85%RH (MSL 1) or 192 hours @ 30°C / 60% RH (MSL 3) moisture soak, and 3 cycles of IR reflow with a peak temperature of 260°C.

5.1: Baking Oven

5.2: Moisture Soak Chamber

5.3: Reflow Oven



5.4: Reflow Profile

c. HTRB (High Temperature Reverse Bias Test)

Discrete semiconductor samples were submitted to HTRB testing to evaluate product electrical functionality per industry standard MIL-STD-750-1 M1038/M1039. Post 168h HTRB test results showed all samples working normally with measured data being within datasheet specification limit.
Test Condition: Tjmax, V = 100% Bias

5.5: Manual ATE Test

5.6: Small PCB on HTRB Board

5.7: HTRB Chamber

d. HTOL (High Temperature Operation Life Test)

Analog semiconductor samples were submitted to HTOL testing to evaluate the product electrical functionality per industry standard JESD22-A108. Post 168h HTOL test results showed all samples working normally with measured data being within datasheet specification limit.
Test condition: Tjmax & V_{Bias} = Vcc(max).

5.8: Manual ATE Test

5.9: Small PCB on HTOL Board

5.10: HTOL Chamber

e. HAST (High Acceleration Stress Test)

HAST was performed per industry standard JESD22-A110 to evaluate the reliability of non-hermetic packaged solid-state devices within a humid environment. No electrical functionality failures or package cracks were seen after 96h of HAST. Test Condition: 130°C, 85% RH, 33.3 Psia and Vr 80% Bias or Max rated Vcc.

5.11: Manual ATE Test

5.12: Small PCB on HAST Board

5.13: HAST Chamber

f. TC (Temperature Cycling Test)

Samples were submitted to TCT per industry standard JESD22-A104 to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high- and low-temperature extremes on aged FGs. No electrical functionality failures or package cracks were seen after 168 cycles of TC. The test temperature ranged from -65℃~150℃.

5.14: Manual ATE Test

5.15: Temperature Cycling Chamber

g. Pressure Cooker Test (PCT)

Samples were submitted to pressure cooker testing per industry standard JESD22-A102 to evaluate moisture resistance and robustness testing on aged FGs. No electrical functionality failure or package cracks were observed after 96 hours of PCT.
Test condition: 121°C, 100% RH and 29.7Psia.

5.16: Manual ATE Test

5.17: PCT Chamber

h. H3TRB (High Humidity High Temp. Reverse Bias)

Samples were submitted to H3TRB testing to evaluate the product electrical functionality per industry standard JESD22-A101. The post 168h H3TRB test results showed all samples working normally with measured data being within datasheet specification limit.

5.18: Manual function test

5.19: H3TRB Board

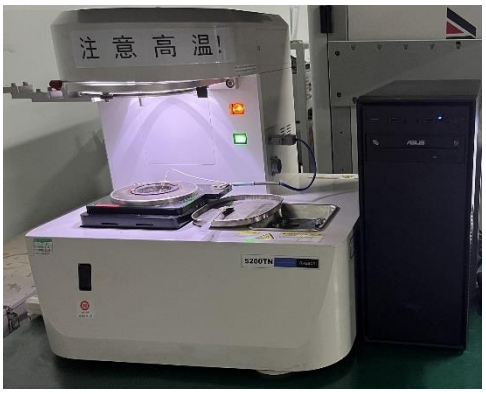
5.20: H3TRB Chamber

i. Solderability Test

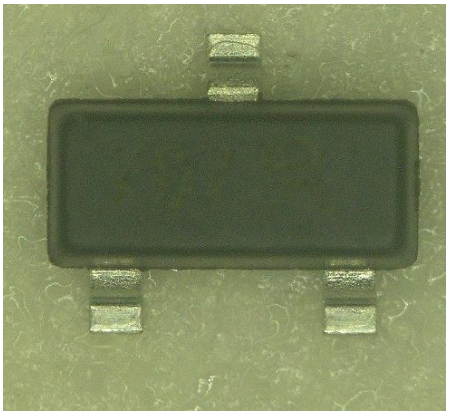
Samples were submitted for solderability testing per industry standard J-STD-002 to validate solderability performance of component leads and terminations on aged FGs. Initial check on lead pins did not reveal any anomalies; no lead finish oxidization or discoloration was seen. The post solderability tests showed good wettability of the lead finish on aging products.

j. Dip and Look Test

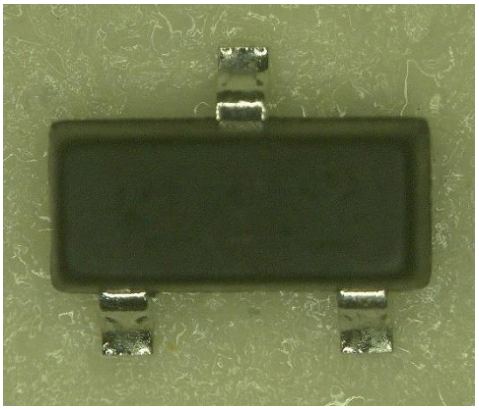
All leads exhibit a continuous solder coating free from defects for a minimum of 95% of the critical area of any individual lead.



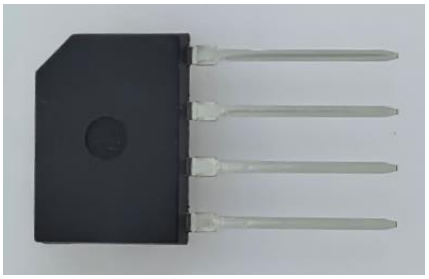
5.21: Solder dip test equipment



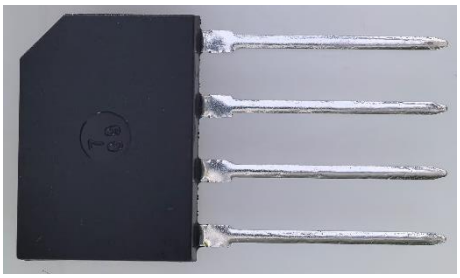
5.22: Sample before solder dip



5.23: Sample after solder dip



5.24: Through-hole sample before solder dip

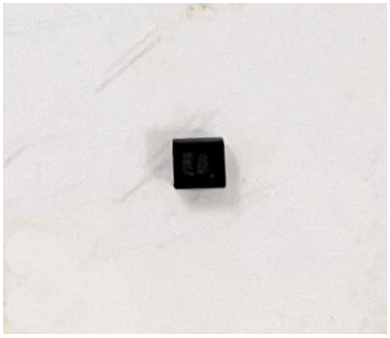


5.25: Through-hole sample after solder dip

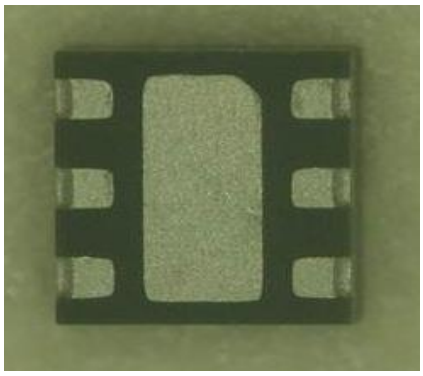
k. Surface Mount Process Simulation Test for lead-less packages

All leads exhibit a continuous solder coating free from defects for a minimum of 95% of the critical area of any individual lead.

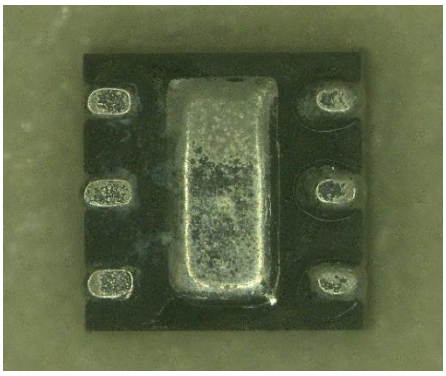
5.26: Solder printed by Stencil on ceramic board



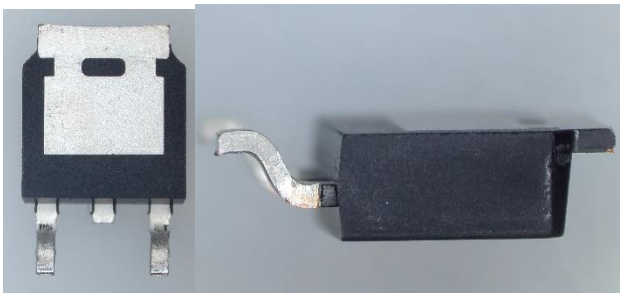
5.27: Device surface mounted on ceramic board



5.28: Sample before SMT soldering

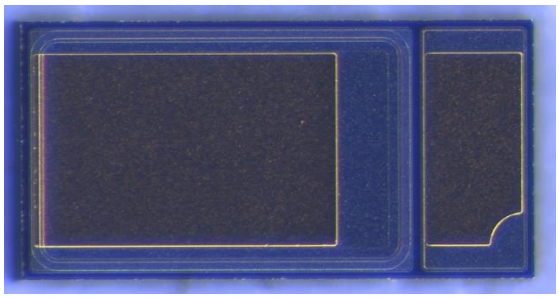


5.29: Sample after SMT Soldering

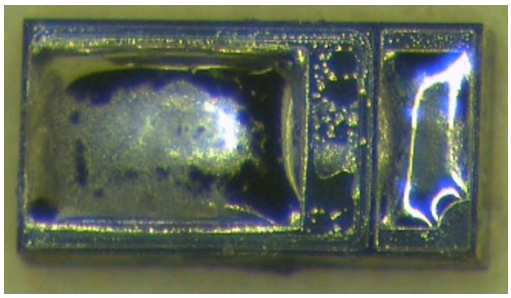


5.30: SMD Sample before soldering

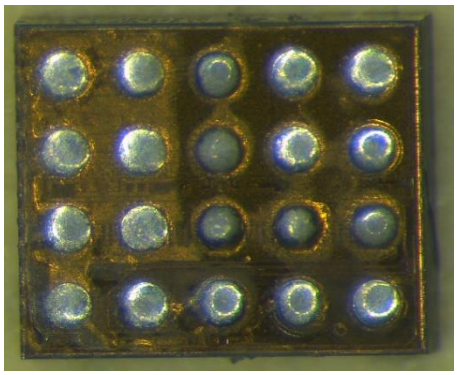
5.31: Sample after soldering on PCB



5.32: CSP Sample before soldering



5.33: CSP Sample after soldering



5.34: CSP Sample after soldering

Diodes also performed a detailed analysis of the customer return history from FG manufactured across external assembly & test houses, i.e. subcontractors, and aged up to 3 years since the date of manufacture. No indication of any quality or reliability issues was observed.

6. Conclusion

Diodes did not observe any quality or reliability related electrical or solderability (Sn or NiPdAu plating) failures of FG up to 3 years of age that could be solely attributed to the age of FG since the date of manufacture. Visual inspection of sampled FG, vacuum bags (MSL 3 products), HICs, labels, cover tape peel performance did not show any anomalies as well.

We can therefore assure that the product performance of Diodes products is not adversely impacted up to a shelf life of at least 3 years from the date of manufacture.

Diodes is committed to continue performing further age-related reliability testing and analysis in the future to pursue ensuring an even longer shelf life for our FG products. Results of these exercises will be published accordingly as they become available.

Alexander Moeller
Corporate Quality Director
Diodes Incorporated

References:

- JEP160, Revision A, August 2022: Long-Term Storage for Electronic Solid-State Wafers, Dice, and Devices
- JESD22-A101, Revision D, January 2021, Steady-State Temperature-Humidity Bias Life Test
- JESD22-A102, Revision E, January 2021, Accelerated Moisture Resistance - Unbiased Autoclave
- JESD22-A104, Revision F, April 2023, Temperature Cycling
- JESD22-A108, Revision G, November 2022, Temperature, Bias, and Operating Life
- JESD22-A110, Revision E, May 2021, Highly Accelerated Temperature and Humidity Stress Test (HAST)
- JESD22-A113, Revision I, April 2020: Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
- J-STD-020, Revision F, December 2022: JOINT IPC/JEDEC Standard Moisture/Reflow Sensitivity Classification for Non-hermetic Surface Mount Devices (SMDs)
- J-STD-002, Revision E, November 2017: Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
- J-STD-033 Revision D, April 2018: Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices